fido2100 3-Port Industrial Ethernet DLR Switch with IEEE 1588

Data Sheet

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1 Overview

The fido2100 is part of the Innovasic fido® family of real-time communication products. The fido2100 is a managed, 3-port Ethernet switch with support for IEEE-1588 and Device Level Ring (DLR) protocol. The fido2100 enhances the capabilities of Innovasic's line of Industrial Ethernet products by providing an infrastructure element with low latency, time synchronization and redundancy for any embedded Industrial Ethernet solution.

The fido2100 is an IEEE 802.3 standard compliant, Layer 2 switch that is compatible with the IEEE 802.1D standard. It has three ports: two are external ports that function as physical ports of a product and one is an internal port that connects to the host CPU. Each of the three ports has an IEEE 802.3 compliant MAC and the ports are interconnected with each other through full wire speed, non-blocking switching logic. Figure 1 illustrates the top-level blocks of the fido2100 architecture.

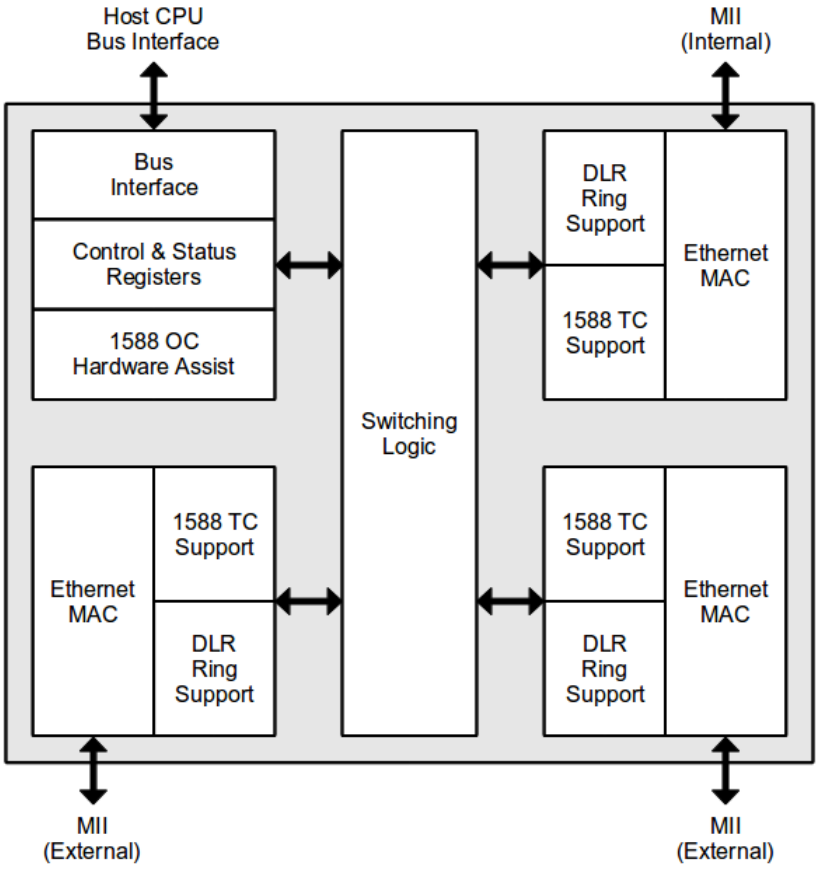

Figure 1 fido2100 Top Level Block Diagram

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The pass-through of traffic is handled swiftly by using cut through forwarding to pass traffic to the other external port. This is accomplished without host CPU intervention, which keeps throughput time host interaction to a minimum and keeps pass through delay to a minimum.

The fido2100 also has the ability to operate in a DLR configuration, which provides media redundancy amongst its members. Host CPU source code is available to provide the ability for the device to be a DLR participant or a DLR supervisor using the DLR support functions. The fido2100 will default to linear topology operation, and when inserted into a ring, will automatically change to DLR operation as a DLR participant.

1.1 Introduction to Device Level Ring Protocol

There are a variety of Industrial applications in which Ethernet ring topologies are preferable to the star topologies common in enterprise networks. Ring networks provide inherent single-point fault tolerance and reduced connectivity costs. Device Level Ring (DLR) protocol provides a means for detecting, managing and recovering from faults in a ring-based network.

DLR supports three classes of devices:

1 Ring Supervisor – Ring Supervisors are required to send and process DLR beacon frames at the default beacon interval.
2 Ring Node, Beacon-based – These devices are required to process beacon frames.
3 Ring Node, Announce-based – These devices are not required to process DLR beacon frames, but must be capable of processing announce frames.

A DLR network consists of a Ring Supervisor and any number of Ring Nodes. Ring nodes incorporate fido2100 technology with at least two external ports. The Ring Supervisor is responsible for generating a “beacon” at regular intervals. These beacons traverse the ring in each direction. The ring supervisor must be capable of blocking DLR frames to avoid infinite propagation of beacons. Faults are detected when beacon traffic is interrupted. There are obviously a number of failure mechanisms and associated recovery strategies. For a detailed explanation of DLR refer to ODVA documentation - Volume II: EtherNet/IP Adaptation of CIP, chapter 9, section 9-5. For definition of the DLR EtherNet/IP object, refer to Volume II: EtherNet/IP Adaptation of CIP, chapter 5, section 5-5.

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1.2 Introduction to IEEE-1588

The IEEE 1588 standard, also known as Precision Time Protocol (PTP), provides a means to synchronize participants in a network to a common time source. Each network participant has its own precision time source or "ordinary clock". A PTP system consists of some number of ordinary clocks connected to a network. A grandmaster is elected based upon the quality of available time sources and all other participants synchronize directly to it.

PTP systems can be expanded through the use of "boundary clocks". The boundary clock provides a means to bridge synchronization from one network segment to another. A synchronization master can then be elected for each network segment. The root timing reference remains the grandmaster.

PTP is a master-slave protocol. The master and network participants exchange synchronization messages. However, these messages will be delayed as they traverse the network due to the inherent latency of the network infrastructure. To compensate for this latency, PTP includes the concept of a transparent clock. The transparent clock automatically compensates for latency by modifying the timestamps in synchronization messages as they pass through a given device. The fido2100 provides hardware support for both transparent and ordinary clocks.

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2 Features

- IEEE 802.3
  - 10/100Mbps, Half / Full Duplex
  - Full Duplex Flow Control
  - Half Duplex Back Pressure Flow Control
  - Broadcast / Multicast Storm Prevention

- IEEE 1588 V2
  - Hardware Assist for Ordinary Clock
  - End-to-end Transparent Clock

- DLR Beacons
  - Capability to processes beacons from 100 ms down to 100 µs
  - Provides auto-generation of beacon frames for supervisor functions

- Cut through forwarding
  - Cut through forwarding minimizes latency for High Performance Control
  - Applications such as CIP Motion

- IP Differentiated Services Code Point (DSCP) based Quality of Service (QoS)
  - 4 Prioritized Queues per Port

- Incoming Filtering on Unicast / Multicast Traffic
  - 256-entry Dynamic Unicast MAC Learning and Filtering for 2 External Ports
  - 128 buffers of 128 bytes for each port

- Statistics Counters for 2 External Ports

- Supported Network topologies:
  - Hierarchical Star with either one of the external ports
  - Daisy Chain / Hybrid Daisy Chain Hierarchical Star
  - DLR Media Redundancy with Hardware Support for a Single Fault Tolerant Ring Protocol

- Software for Switch & DLR Protocol Management

- Full Industrial Temperature Range -40 to +85C
- Packages:
  - 128 pin Plastic Low Profile QFT (LQFP), RoHS Compliant
  - 128 Ball Grid Array (10x10mm BGA), RoHS Compliant

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2.1 IEEE 802.3 MAC Details

The fido2100 implements an IEEE 802.3 standard compliant MAC for each of the three ports. While beginning a transmission, the MAC will transmit 7 bytes of preamble pattern 0x55, followed by one byte of start of frame delimiter 0xD5, followed by the frame data and frame check sequence as per IEEE 802.3 specification.

While transmitting, the MAC will enforce an inter-frame gap period of 960 ns at 100Mbps speed and 9.6 ns at 10Mbps speed as per IEEE 802.3 specification. While receiving, the MAC can tolerate shrinkage of the inter-frame gap period down to 80 nanoseconds at 100Mbps speed and 800 nanoseconds at 10Mbps speed.

In full duplex mode the MAC will ignore carrier sense and collision detect signals from the PHY and is ready to transmit after satisfying the inter-frame gap period as per IEEE 802.3 specification. In half duplex mode, the MAC will wait for the current transmission to complete and the carrier sense signal to be de-asserted. Then it will monitor if the carrier sense signal gets asserted in the first 2/3 duration of the inter-frame gap period. If the carrier signal gets asserted within that period, the MAC will wait until the carrier sense signal gets de-asserted to restart inter-frame gap period again. If the carrier sense signal gets asserted in the last 1/3 duration of the inter-frame gap it will be ignored as per the IEEE 802.3 specification. The MAC is ready for transmission at the end of the inter-frame gap period. If a frame is not available for transmission at the end of the inter-frame gap, the carrier sense signal will be monitored for restarting inter-frame gap period.

If the frame transmission has commenced in half duplex mode and the collision signal gets asserted by the PHY, transmission of the current frame data will be truncated with a jam pattern of 4 bytes of 0xFF. At this point the collision back off and retransmission procedure will start using the truncated binary exponential back off algorithm as per IEEE 802.3 specification. At the end of enforcing a jamming pattern, the MAC will impose a delay before attempting to retransmit the frame. The delay is an integer multiple of a slot time, where one slot time is equal to 512 bits time. The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer r in the range:

$$0 \le r < 2^{k}; \text{ where } k = \min(n, 10)$$

If sixteen transmission attempts fail with collision for the same frame, the frame will be dropped as per IEEE 802.3 specification. The mechanism used to generate the uniformly distributed random number is a free running 10 bit wide linear feedback shift register (LFSR). The LFSR will cycle through all states in 1024 transmit clocks of the port under consideration. Depending on the retransmission attempt number *n*, the most significant *k* bits of LFSR are used as delay integer *r*. Due to the free running nature of the LFSR, lock step random number generation in two different devices should not occur. However, a facility is provided whereby the firmware can load a random seed value into the LFSR anytime during operation.

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The MAC will drop frames received with errors signaled by the PHY device and those with frame check sequence (CRC) errors. It will drop frames shorter than 64 bytes as per IEEE 802.3 specification. It will drop frames longer than maximum IEEE 802.3 tagged frame size of 1522 bytes. The MAC will also drop frames with alignment error, i.e. those having a non-integral number of bytes.

2.1.1 IEEE 802.3 Full Duplex Flow Control

The fido2100 implements IEEE 802.3 compliant full duplex flow control using PAUSE frames. In order to provide optimum performance, a special set of rules are followed for PAUSE frame generation and reception.

PAUSE frame reception is enabled on external ports operating in full duplex mode and transmission on the port through which the PAUSE frame was received will be suspended for specified pause duration in the PAUSE frame. PAUSE frame reception is always disabled on the internal port, since the host CPU will always have enough memory for its communications.

If speed and duplex modes of external ports are same and when buffer usage on either one of external ports reaches 95% of buffer capacity, a PAUSE frame will be generated from internal port to host CPU with maximum pause duration. If the buffer situation has not improved at the end of pause duration, additional PAUSE frames will be generated from internal port as needed. When buffer usage on both external ports reaches below 85% of buffer capacity, a PAUSE frame will be generated on internal port with zero pause duration to cancel pause. If speed and duplex modes of external ports are not same, PAUSE frames will not be generated.

For external ports, PAUSE frame generation on a port is enabled only for full duplex mode and when both external ports have same speed and duplex settings. When a first external port is operating in full duplex mode and buffer usage on internal port or second external port reaches 95% of buffer capacity a PAUSE frame will be generated on first external port with maximum pause duration. If the buffer situation has not improved at the end of pause duration, additional PAUSE frames will be generated from first external port as needed. When buffer usage on both internal and second external ports reaches below 85% of buffer capacity, a PAUSE frame will be generated on first external port with zero pause duration to cancel pause. If speed and duplex modes of external ports are not same, PAUSE frames will not be generated.

Obviously, for flow control on fido2100 to work properly, the integrated MAC on host CPU must support flow control as well. Most Ethernet microprocessors do support this capability and dual port product designer must ensure that the selected host CPU supports flow control.

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2.1.2 Half Duplex Flow Control and Broadcast/Multicast Storm Prevention

The fido2100 implements back pressure flow control in half duplex mode. When both external ports are operating in same speed and half duplex mode, and buffer usage on the internal port or other external port reaches 95% of buffer capacity, back pressure flow control is activated on the first external port. This continues until the buffer usage on both internal and second external ports reaches below 85% of buffer capacity. When back pressure flow control is activated on a port, the port will continue to transmit frames while it has any. If there is no frame to transmit, the frame will keep the carrier sense signal active by sending the preamble pattern periodically, causing the neighboring node to back off from transmitting any frames. If speed and duplex modes of external ports are not same, back pressure will not be activated.

Excessive broadcast frames can overload the CPU of all devices on network, especially IO adapters and IO blocks, leading to poor performance. To avoid this, the fido2100 implements a broadcast storm prevention mechanism. When received broadcast data within a 100 millisecond period (1 second at 10Mbps) reaches about 1% of network bandwidth in a port operating at 100Mbps speed, additional broadcast frames received on that port within that period will be dropped. This process is repeated for every 100 millisecond period. In well-engineered networks, broadcast storms do not occur during normal operation and a 1% broadcast storm limit will never be reached.

Similarly every port is also monitored for received non-redundancy (non-DLR/BRP) multicast frames. When received non-redundancy multicast data within a 10 millisecond period (100 milliseconds at 10Mbps) reaches about 50% of network bandwidth in a port operating at 100Mbps speed, additional nonredundancy multicast frames received on that port within that period will be dropped. This process is repeated for every 10 millisecond period. In well-engineered networks, multicast storms do not occur during normal operation.

2.2 IEEE 1588 V2

2.2.1 IEEE 1588 Hardware Assist for Ordinary Clock

Figure 2 below shows a block diagram of the IEEE 1588 V2 hardware assist that can be used to implement an IEEE 1588 ordinary master or slave clock on an end device. The MII traffic of the internal port between the host CPU and the fido2100 is monitored by two independent 1588 frame detection logic blocks, one for the transmit channel and the other for the receive channel.

Whenever the timestamp point of a passing transmit/receive frame is reached, a snapshot of the system time counter is saved in a temporary register. When the appropriate 1588 frame type is also detected in the frame, the snapshot is saved from the temporary register to the transmit/receive snapshot register. The receive snapshot register contains a sixteen entry FIFO, while the transmit snapshot register is a single entry register. With the transmit snapshot register, the snapshot will be locked to prevent

overwriting by subsequent frames. The firmware must later clear the lock after it has read the snapshot. With the receive snapshot register, the firmware should read all snapshots while the FIFO is not empty. If the FIFO becomes full because the firmware is slow to read it, additional snapshots will not be saved until the FIFO has a free entry. To distinguish saved snapshots, the received frame sequence identifier and source port identity are also locked in the FIFO and may be read through appropriate registers along with the snapshot.

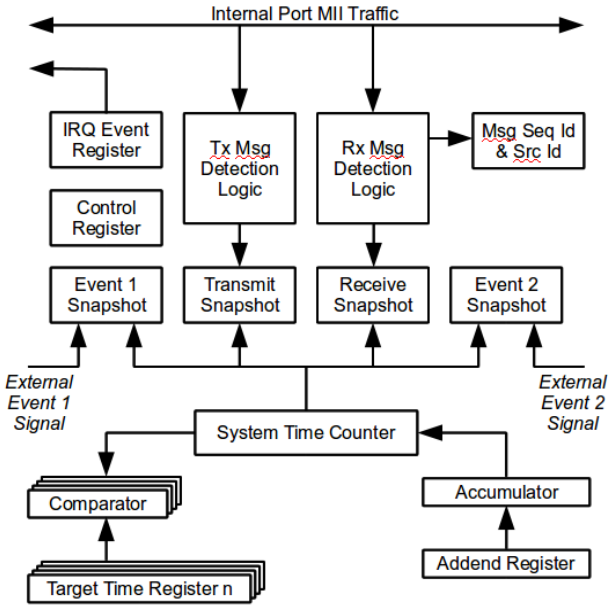

Figure 2 IEEE 1588 Hardware Assist Block Diagram

The supported frame mapping for frame detection logic is PTP over UDP over IPV4 over IEEE 802.3 tagged or untagged frames. The frames detected are based on the master mode bit setting in the time sync control register. In master mode, Sync frames are time stamped on transmit and Delay_Req frames are time stamped on receive. In slave mode, Delay_Req frames are time stamped on transmit and Sync frames are time stamped on receive. In addition, the sub-domain field of frames must match the subdomain configuration register for the snapshot to be saved.

The addend register, accumulator and system time counter comprise a frequency compensated clock under firmware control. The accumulator adds the addend register to itself on every incoming clock from the oscillator and the overflow signal of the accumulator causes the system time counter to increment. This provides a high precision tunable digital clock whose frequency of operation can be controlled by firmware through writing suitable values to the addend register.

While transmit and receive frame detection logic operate independently at 25MHz MII clock rates, the rest of the logic operates at 100MHz clock rate. The addend register and accumulator of frequency

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compensated clock are 32-bits wide, while the system time counter is 64-bits wide. The tunable precision for frequency compensation is better than 1 part per billion ($1x10^{-9}$). The procedure for realizing various nominal system time frequencies is described below.

- **FreqOscillator** is the clocking frequency of the time synchronization
- **FreqClock** is the nominal frequency at which the system time counter is to be incremented.
- **FreqDivisionRatio** = FreqOscillator / FreqClock (This must always be > 1)
- **FreqCompensationValue** = frequency compensation value is the number held in the addend register, which is added to the accumulator once every 1/FreqOscillator.

The equation for the FreqCompensationValue utilizes the precision of the accumulator and the FreqDivisionRatio. Since the accumulator is 32 bits, the following equation provides the value for the Addend register:

$$\textbf{FreqCompensationValue} = 2^{32} / \textbf{FreqDivisionRatio}$$

The hexadecimal representation of the FreqCompensationValue is the value that is written to the addend register. The following table gives examples of addend values based on a 100 MHz FreqOscillator.

Freq-oscillator	FreqClock	FreqDivisionRatio	FreqCompensationValue
100 MHz	83.33 MHz	1.2	0xD5555555
100 MHz	80 MHz	1.25	0xCCCCCCCD
100 MHz	66.66 MHz	1.5	0xAAAAAAAB

The synchronization accuracy between the time master and the slave depend on cumulative accuracy of individual components used in the system. When a time slave is connected directly to the time master, a synchronization accuracy of less than 50 ns from master is easily possible. This accuracy is achievable with low cost 50PPM crystal clock oscillators. Turbulent air flow over the crystal oscillator should be avoided to prevent rapid temperature changes resulting in short term stability errors. Some PHY devices introduce random delays in transmit and receive paths, which can increase time synchronization errors significantly. It is recommended that the PHY devices be investigated for such behavior. Any asymmetry in transmit and receive paths should be accounted properly by firmware to avoid accumulation of errors. In a cascaded transparent clock configuration between the time master and the slave, the errors will increase linearly with the number of transparent clocks.

There are two 64-bit target time registers and comparators that can be used to generate an interrupt to the host CPU when the system time counter reaches the target time. This feature can be used by firmware to schedule/coordinate control loops/activities. While both target time registers can be used by firmware for any purpose, the second target time register has a special capability to generate a pulse

per second signal. The pulse per second signal is required for internal IEEE 1588 compliance testing, but is not required on shipping products.

There are two additional snapshot registers for two external events. These snapshots can be used to synchronize system time with an external clock. For example, the event 1 can be used to synchronize internal IEEE 1588 system time as a slave with a global positioning system (GPS) signal as the master. Similarly, the event 2 can be used to synchronize internal IEEE 1588 system time as a master with an external clock in another module in the system as the slave. Both event snapshots have the same capability/behavior in implementation and they can be used interchangeably.

2.2.2 IEEE 1588 End to End Transparent Clock

The fido2100 implements an integrated IEEE 1588 V2 end to end transparent clock (E2E TC). This is a single step transparent clock in IEEE 1588 terminology. The supported frame mapping is PTP over UDP over IPV4 over IEEE 802.3 tagged or untagged frames. The E2E TC uses a non-syntonized free running timer as a time base. The free running timer runs at 100MHz, but the timestamp circuit uses both edges of the clock for sampling, and delay computation is suitably adjusted to make it effectively run at 200MHz, with 5 ns resolution.

In E2E TC mode, whenever an IEEE 1588 V2 Sync or Delay_Req frame is received, a receive timestamp is triggered on ingress at the timestamp point following the start of frame delimiter. The frame is parsed to extract the UDP checksum and correction field. When the received frame doesn't contain any errors and when the frame is transmitted through a port, a transmit timestamp is triggered on egress at the timestamp point. The residence time delay is then computed on the fly from the transmit and receive timestamps. The residence time delay is then added to the correction field in the frame with the UDP checksum and frame CRC adjusted on the fly.

Without transparent clocks, cascaded switches or boundary clocks will accumulate errors at exponential rate making time synchronization unstable. With transparent clocks the accumulation of errors is linear with the number of nodes. The implemented E2E TC has a theoretical worst case error of +/-15 ns per node assuming 50PPM source crystal oscillator stability.

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2.3 Device Level Ring (DLR) Protocol Support

The fido2100 provides hardware support for a single-fault tolerant ring protocol. The DLR protocol support for non-supervisor mode and support for supervisor mode can be enabled by setting appropriate bits in the redundancy control register.

In non-supervisor mode, received non-erroneous DLR beacon frames from the active ring supervisor through either port will be automatically dropped after extracting state information and restarting the DLR beacon timers. Received non-erroneous DLR beacon frames may optionally be configured to be delivered to the host CPU by setting appropriate bits in the redundancy control register. Irrespective of this bit setting, beacon messages received from a different supervisor than active supervisor are always forwarded to host CPU. The fido2100 can be configured to interrupt host CPU when ring beacon frames from active supervisor are received through either port or are not received through either port within ring beacon timeout period. The fido2100 can also be configured to interrupt host CPU when a change of state is observed in ring beacon frames from active ring supervisor received through either port. Neighbor check and multicast sign on frames received from either external port will be forwarded only to host CPU and those from host CPU will be forwarded only through port number matching source port number field in frame. Source identifier and sequence identifier fields of received neighbor check frames are captured to identify received port later. Unicast sign on frames are treated as any other unicast frame.

In supervisor mode, either one of the external ports can be placed in blocked mode by setting appropriate port transmit/receive blocked bits in redundancy control register. All frame reception and transmission will be blocked by the port in blocked mode with the exception of some special frames. These special frames are described under port transmit/receive blocked bits in redundancy control register. In supervisor mode, ring beacon frames can be automatically generated and transmitted through unblocked ports to reduce the CPU load and their arrival through both ports are monitored. The fido2100 can be configured to interrupt the host CPU when DLR beacon frames are received through either port or are not received through either port within DLR beacon timeout period. The fido2100 can also be configured to interrupt the host CPU when a change of state is observed in DLR beacon frames are received from the active ring supervisor through either port. Received non-erroneous DLR beacon frames may optionally be configured to be delivered to host CPU by setting appropriate bits in redundancy control register. Irrespective of this bit setting, beacon messages received from a different supervisor than self is always forwarded to host CPU.

In supervisor mode, neighbor check and multicast sign on frames received from either external port will be forwarded only to the host CPU, and those from the host CPU will be forwarded only through the port number matching the source port number field in the frame. The source identifier and sequence identifier fields of received neighbor check frames and sign on frames are captured to identify the received port later. Link/neighbor status frames received from either external port will be forwarded only to the host CPU. The source identifier and sequence identifier fields of received link/neighbor status frames are captured to identify the received port later.

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2.3.1 Network Loops

The fido2100 has a built in safety feature to detect network loops. Undetected, network loops can cause severe network problems. Network loops may be present when the user inadvertently misconnects the network in such a way as to create a loop or when the user intentionally creates a DLR topology, but fails to configure a DLR supervisor. When a frame is received through one of the external ports with the source MAC address the same as the MAC address of the host CPU, the fido2100 will drop that frame and will set a port-specific bit in the switch event register indicating that such a frame was received. These bits can be read and cleared by firmware and can be used to flag the network fault situation to the user. Alternatively, the fido2100 can be configured to interrupt the host CPU when those bits are set.

It should be noted that in a properly configured DLR with a DLR supervisor, network loops may be present for short durations when the network is being reconfigured. Hence firmware should not flag the user of this fault condition when operating in proper DLR mode. The firmware can detect the proper DLR mode by the presence of DLR beacons on the network, whereas in non-DLR mode or an improperly configured DLR mode, DLR beacons would be absent on network.

2.4 Cut Through Forwarding

The fido2100 implements cut through forwarding with store and forward on contention at the transmitting port. COTS switches and standard switching integrated circuits typically support only the store and forward approach. With the store and forward approach a frame has to be completely received before being transmitted. Hence every frame will encounter a delay equal to the length of the frame and additional internal switching delay. This can become an issue for high performance applications such as CIP motion when a long chain of cascaded switches are involved, such as in daisy chain or DLR topology networks.

With cut through forwarding, when frame reception begins and when a sufficient number of bytes of a frame have been buffered, the frame is queued for transmission, subject to the following forwarding rules:

1. If the transmitting port is idle and ready for transmission, it will immediately start frame transmission while the reception is in progress.
2. If the transmitting port is not free immediately, it will start transmitting as soon as the port becomes ready for transmission, while the reception is in progress.
3. If the transmitting port doesn't become available before the entire frame is received, the received frame will be buffered completely for store and forward.

Because of cut through forwarding, non-IP frames from all transmit queues and IP frames from transmit queues 2 and 3 will face a delay of 2.8 µs, other non-IEEE 1588 frames will face a delay of 4.9 µs and IEEE 1588 time synchronization frames will face a delay of 7.3 µs through the fido2100,

when the transmitting port is free of contention. Cut through forwarding is disabled for a transmit port when the receiving port is operating at 10Mbps speed and the transmitting port is operating at 100Mbps speed. In this case, store and forward is used.

2.5 Quality of Service

In order to support high performance applications such as CIP motion, the fido2100 enforces quality of service based on IP Differentiated Services Code Point (DSCP). The fido2100 implements four prioritized transmit queues per port. Frames received with DSCP 59 are queued in the highest priority transmit queue (queue #1). Frames received with DSCP 55 are queued in the second highest priority transmit queue (queue #2). Frames received with DSCP 47 and 43 are queued in the third highest priority transmit queue (queue #3). Frames received with other DSCP values are queued in the lowest priority transmit queue (queue #4). In addition, DLR protocol frames are queued in the highest priority queue 1. When a port is ready to transmit the next frame, the highest priority frame is chosen from the current set of queued frames for transmission based on strict priority ordering. Within a given priority queue frames are transmitted in FIFO order.

2.6 Unicast and Multicast Address Filtering

The fido2100 implements 256 entry dynamic unicast MAC address learning and filtering mechanism. The unicast MAC address learning table is implemented as 4-way learning/look up table of 64 rows. The 48-bit source MAC address from a frame received on any external port is hashed into 6-bits by XOR operation of every sixth bit. The hash index identifies the row where one of four locations that is free is used for MAC address learning along with associated external port. When none of them is free, the 4th way location is always overwritten. Learning is performed on source MAC address only from frames with a unicast or multicast destination MAC address. Automatic aging of learned entries will happen in 4- 6 minutes, unless learning is refreshed within that period.

When a frame with unicast destination address is received through any port, 4-way simultaneous lookup is performed from entries at hash index location of destination MAC address. If the address is found, the frame is forwarded only through associated external port. If the address is not found, then it is forwarded through all other external ports. When a frame with unicast destination address is received through one of the external ports and the destination address matches host CPU MAC address, then that frame is forwarded only to internal port.

The fido2100 implements multicast filtering on the internal port for frames received through external ports and no multicast filtering is implemented for the external ports. The multicast filter consists of a 2048 bin hash table. The received multicast destination address is passed through a 32-bit Ethernet CRC generator and the least significant 11 bits of the resulting CRC is used to index into the 2048 bin hash table. When the indexed bin in the hash table is set, the frame will be forwarded to the internal port and the other external port. If not set, the frame will be forwarded only to the other external port.

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By default, all 2048 bins of the multicast hash table are set to zero after power up or chip reset, and no multicast frames will be forwarded to the internal port. Since most devices such as I/O devices don't need to receive multicast frames, they don't need to change this default behavior. Note that the multicast filter table need not be set for receiving multicast ring frames.

2.7 Statistics Counters

The fido2100 implements statistics counters for the external ports. These counters can be used by firmware for the media and interface counters of the EtherNet/IP Ethernet Link object (Class Code: 0xF6). Most of these counters are 16 bits wide and to avoid roll over issues, firmware must read these registers at least once every 200 milliseconds or on demand, to calculate an increase in counter values. The firmware can then add the increase to firmware maintained 32 bit counters.

Counters are implemented for valid frames received with the group bit set in the destination address, valid frames received with a unicast destination address, total byte count of valid frames received, frames received with length greater than 1522 bytes, frames received with alignment error, frames received with a frame check sequence (CRC) error and frames received with other errors, including short runt frames less than 64 bytes in length.

Counters are also implemented for valid frames transmitted with the group bit set in the destination address, valid frames transmitted with a unicast destination address, total byte count of valid frames transmitted, frames transmitted after exactly one collision, frames transmitted after multiple collisions, frames dropped due to excessive collisions and frames truncated with error during transmission.

2.8 Buffer Management

The fido2100 implements an efficient packet buffering scheme using on board dual port SRAM memory. The buffers are 128 bytes in size to minimize memory wastage. Frames longer than 128 bytes are automatically fragmented to be stored in multiple buffers and reassembled during transmission.

Actual buffer usage depends on a number of factors such as network load, number of frames waiting to be transmitted at each node at the same time, the number of back to back frames arriving at the destination node through both external ports at the same time, etc. For some devices such as motion drives and I/O, buffer usage on any port may never exceed 10% of buffer capacity. For other devices such as network bridges, buffer usage on any port may be typically less than 50% of buffer capacity during normal operation. Irrespective of the type of end device, when buffer usage reaches 95% of buffer capacity on any port under heavily loaded network conditions, flow control will intervene to reduce buffer usage and will ensure frames are not being dropped.

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2.9 Supported Network Topologies

Dual port products designed with this toolkit can be used in a wide variety of network configurations. This single hardware design will support various network topologies. Irrespective of the network configuration used, a dual port end device will always have a single IP address and a single MAC address. This simplifies both configuration requirements and firmware changes required.

Figure 3 shows hierarchical star topology with commercial off the shelf (COTS) switches. Either port of a dual port end device may be used to connect to COTS switch to realize hierarchical star network topology.

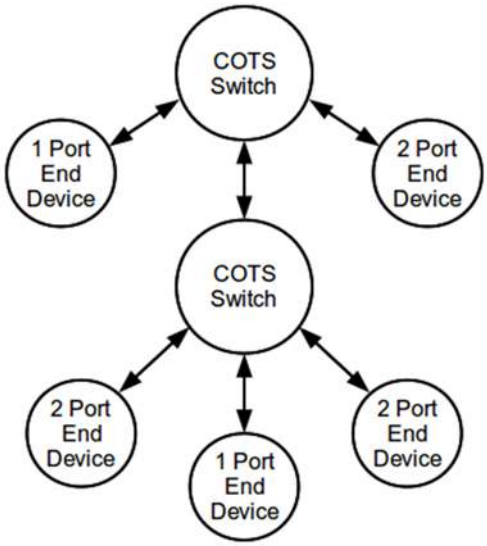

Figure 3 Hierarchical Start Topology

Figure 4 shows a hybrid daisy chain and hierarchical star topology. Single port end devices can be connected to a daisy chain at one of the ends of the chain, or through a standalone three port device that provides the daisy chain capability in the middle of chain. Figure 3 also shows a COTS switch in the middle of a daisy chain.

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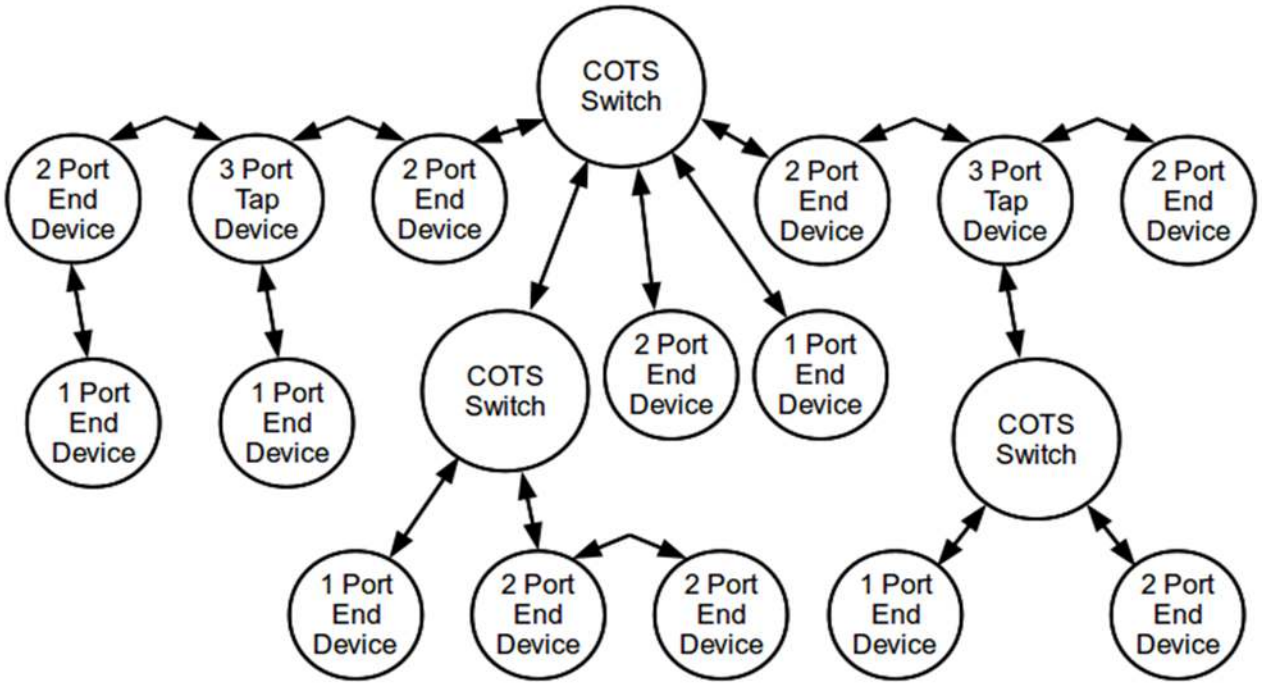

Figure 4 Hybrid Daisy Chain and Hierarchical Star Topology

It should be noted that a slower speed or half duplex link on main daisy chain will become a bottle neck, causing the entire network to operate at reduced capacity. Similarly, a single port device can be connected to either end of main daisy chain network, only if it operates at same/better speed and duplex mode as rest of the network. The recommended method for connecting slower speed/duplex devices is through a three port tap device to avoid performance issues.

Figure 5 shows a ring topology media redundancy that can tolerate single faults. One or more DLR supervisor(s) control the operation of ring. When multiple DLR supervisors are configured, one of them will be automatically chosen as active supervisor. Others will be in passive mode, until the active DLR supervisor fails or is removed from ring.

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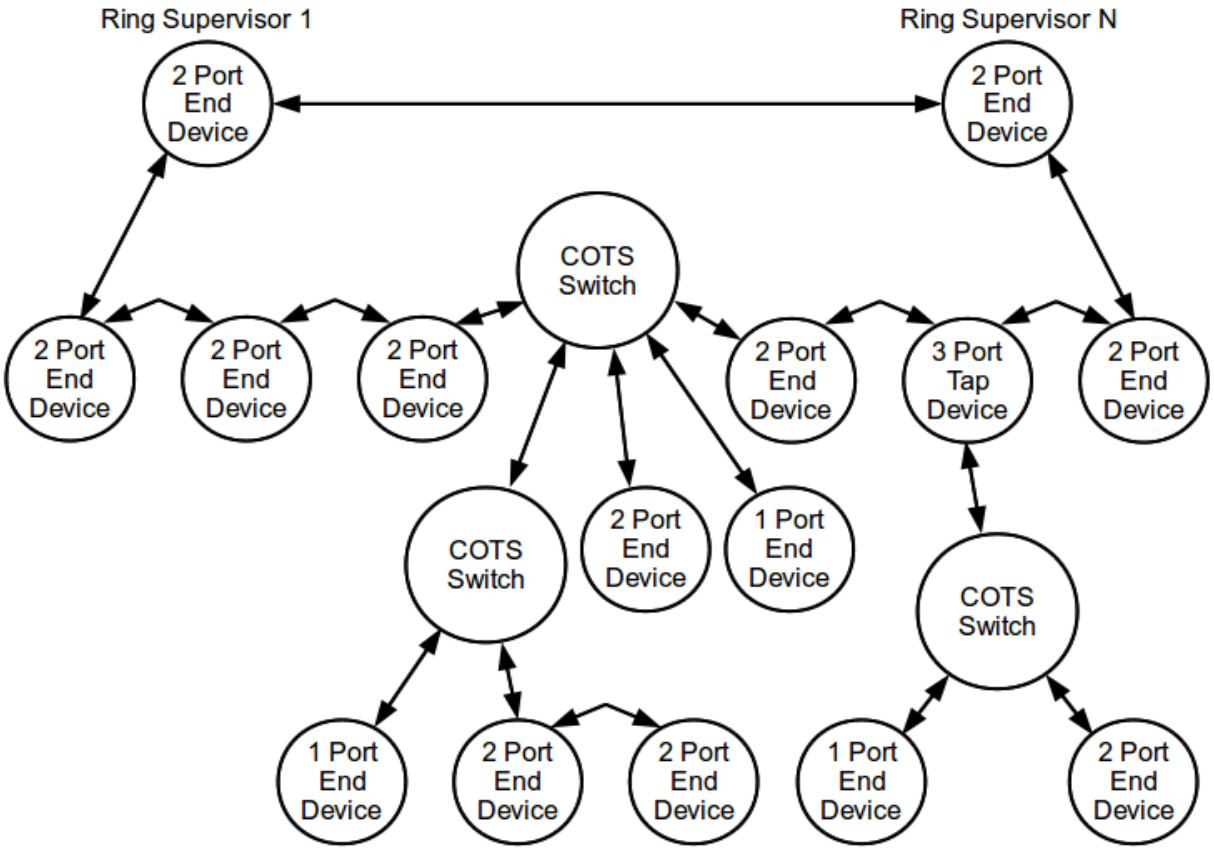

Figure 5 Ring Topology Media Redundancy

For IO applications, a COTS switch in the ring must support IEEE 802.3 tag based and IP DSCP based QoS with at least two prioritized queues, preferably four prioritized queues. The highest priority queue must be dedicated for ring protocol messages for predictable performance. For IEEE 1588 applications such as CIP motion, COTS switches directly on ring must support IEEE 1588 end-to-end transparent clock (or boundary clock) and IEEE 802.3 tag based and IP DSCP based QoS with four prioritized queues. The highest priority queue may be shared between IEEE 1588 and ring protocol messages. If not, COTS switches can be connected through three port tap device as shown in Figure 4.

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The COTS switch must be configured so that ring protocol messages are not forwarded to devices connected to it. IGMP snooping and multicast filtering must be disabled on 2 ports of the COTS switch directly connected to ring to facilitate rapid network reconfiguration. Since unicast filtering cannot be disabled in a COTS switch, it may take couple of CIP connection RPI's for some data packets to be delivered correctly on some nodes after a network reconfiguration. Ring timing parameters such as beacon period and timeout must account for the presence of a COTS switch directly in ring. Typical network recovery time for a ring containing 50 nodes will be less than 1 millisecond for most types of faults on a loaded network with mostly EtherNet/IP frames. Further details of ring topology and protocol are described in, "Device Level Ring Protocol"; see CIP Networks Library, Volume 2, Chapter 9, Edition 1.7 or later (see www.odva.org for details).

It is possible to create complex ring topologies. Some examples are: a backbone ring connecting multiple star topologies; a backbone star connecting multiple ring topologies; a backbone ring connecting multiple ring topologies; and other combinations.

Most dual/three port devices operate as simple ring nodes and require no special configuration. By default they will power up in daisy chain mode and transparently switch to ring mode upon receiving beacon frames from ring supervisor.

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3 LQFP Package

3.1 LQFP Package Pinout

The pinout for the fido2100 Industrial Ethernet Switch LQFP package is as shown in Figure 6. The corresponding pinout is provided in Table 1.

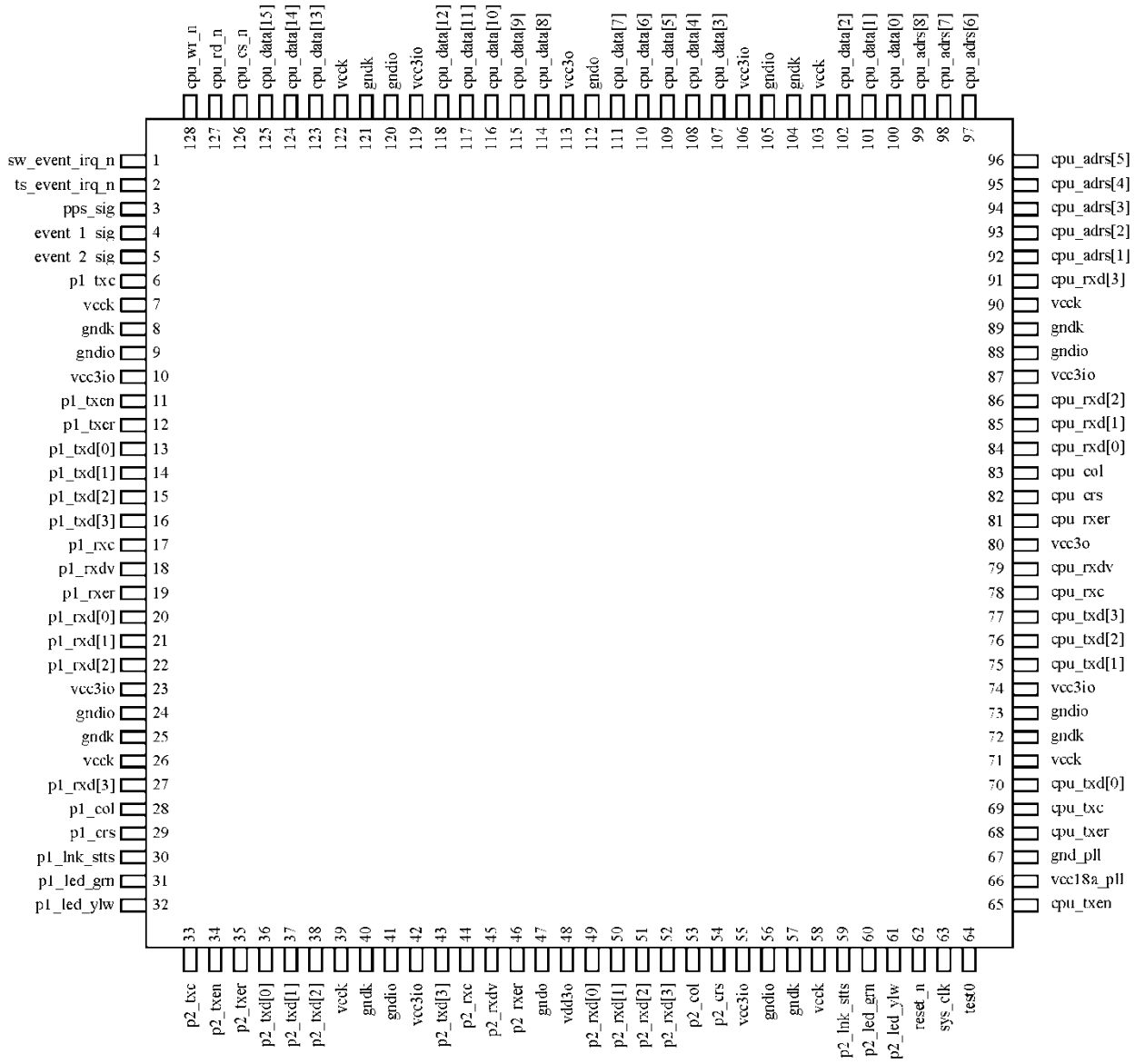

Figure 6 fido2100 LQFP Package Pinout

3.2 LQFP Pin Listing

Table 1 128-Pin LQFP Pin List

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Pin	Signal Name	Type	LQFP Pin Descriptions
1	sw_event_irq_n	output	switch event IRQ, must be connected to a high priority IRQ pin on cpu
2	ts_event_irq_n	output	time sync event IRQ. Optional for non-1588 devices.
3	pps_sig	output	pulse per second signal for 1588 compliance
4	event_1_sig	input	external event 1 snapshot trigger from CPU/others
5	event_2_sig	input	external event 2 snapshot trigger from CPU/others
6	p1_txc	input	port 1 mii, transmit clock from PHY
7	vcck	power	1.8 V digital core supply voltage
8	gndk	ground	digital core ground
9	gndio	ground	i/o ground
10	vcc3io	power	3.3 V i/o supply voltage
11	p1_txen	output	port 1 mii, transmit enable to PHY
12	p1_txer	output	port 1 mii, transmit error to PHY
13	p1_txd[0]	output	port 1 mii, transmit data bit 0 to PHY
14	p1_txd[1]	output	port 1 mii, transmit data bit 1 to PHY
15	p1_txd[2]	output	port 1 mii, transmit data bit 2 to PHY
16	p1_txd[3]	output	port 1 mii, transmit data bit 3 to PHY
17	p1_rxc	input	port 1 mii, receive clock from PHY
18	p1_rxdv	input	port 1 mii, receive data valid from PHY
19	p1_rxer	input	port 1 mii, receive data error from PHY
20	p1_rxd[0]	input	port 1 mii, receive data bit 0 from PHY
21	p1_rxd[1]	input	port 1 mii, receive data bit 1 from PHY
22	p1_rxd[2]	input	port 1 mii, receive data bit 2 from PHY
23	vcc3io	power	3.3 V i/o supply voltage
24	gndio	ground	i/o ground
25	gndk	ground	digital core ground
26	vcck	power	1.8 V digital core supply voltage
27	p1_rxd[3]	input	port 1 mii, receive data bit 3 from PHY
28	p1_col	input	port 1 mii, collision from PHY
29	p1_crs	input	port 1 mii, carrier sense from PHY
30	p1_lnk_stts	input	port 1 mii, link status from PHY (1:link pass, 0:link fail)
31	p1_led_grn	output	port 1 mii,, green led
32	p1_led_ylw	output	port 1 mii,, yellow led
33	p2_txc	input	port 2 mii, transmit clock from PHY
34	p2_txen	output	port 2 mii, transmit enable to PHY
35	p2_txer	output	port 2 mii, transmit error to PHY
36	p2_txd[0]	output	port 2 mii, transmit data bit 0 to PHY
37	p2_txd[1]	output	port 2 mii, transmit data bit 1 to PHY
38	p2_txd[2]	output	port 2 mii, transmit data bit 2 to PHY
39	vcck	power	1.8 V digital core supply voltage

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Pin	Signal Name	Type	LQFP Pin Descriptions
40	gndk	ground	digital core ground
41	gndio	ground	i/o ground
42	vcc3io	power	3.3 V i/o supply voltage
43	p2_txd[3]	output	port 2 mii, transmit data bit 3 to PHY
44	p2_rxc	input	port 2 mii, receive clock from PHY
45	p2_rxdv	input	port 2 mii, receive data valid from PHY
46	p2_rxer	input	port 2 mii, receive data error from PHY
47	gndo	ground	i/o ground
48	vdd3o	power	3.3 V i/o supply voltage
49	p2_rxd[0]	input	port 2 mii, receive data bit 0 from PHY
50	p2_rxd[1]	input	port 2 mii, receive data bit 1 from PHY
51	p2_rxd[2]	input	port 2 mii, receive data bit 2 from PHY
52	p2_rxd[3]	input	port 2 mii, receive data, bit 3 from PHY
53	p2_col	input	port 2 mii, collision from PHY
54	p2_crs	input	port 2 mii, carrier sense from PHY
55	vcc3io	power	3.3 V i/o supply voltage
56	gndio	ground	i/o ground
57	gndk	ground	digital core ground
58	vcck	power	1.8 V digital core supply voltage
59	p2_lnk_stts	input	port 2 mii, link status from PHY (1:link pass, 0:link fail)
60	p2_led_grn	output	port 2 mii,, green led
61	p2_led_ylw	output	port 2 mii,, yellow led
62	reset_n	input	chip reset, active low (internal pull-up)
63	sys_clk	input	25 MHz system clock
64	test	input	test, active high (internal pull-down)
65	cpu_txen	input	cpu mii, transmit enable from CPU
66	vcc18a_pll	power	1.8 V analog supply voltage
67	gnda_pll	ground	analog ground
68	cpu_txer	input	cpu mii, transmit error from CPU
69	cpu_txc	output	cpu mii, 25 MHz transmit clock to CPU
70	cpu_txd[0]	input	cpu mii, transmit data bit 0 from CPU
71	vcck	power	1.8 V digital core supply voltage
72	gndk	ground	digital core ground
73	gndio	ground	i/o ground
74	vcc3io	power	3.3 V i/o supply voltage
75	cpu_txd[1]	input	cpu mii, transmit data bit 1 from CPU
76	cpu_txd[2]	input	cpu mii, transmit data bit 2 from CPU
77	cpu_txd[3]	input	cpu mii, transmit data bit 3 from CPU
78	cpu_rxc	output	cpu mii, 25 MHz receive clock to CPU
79	cpu_rxdv	output	cpu_mii, receive data valid to CPU

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Pin	Signal Name	Type	LQFP Pin Descriptions
80	vcc3o	power	3.3 V i/o supply voltage
81	cpu_rxer	output	cpu mii, receive error
82	cpu_crs	output	cpu mii,
83	cpu_col	output	cpu mii, collision
84	cpu_rxd[0]	output	cpu mii, receive data bit 0 to CPU
85	cpu_rxd[1]	output	cpu mii, receive data bit 1 to CPU
86	cpu_rxd[2]	output	cpu mii, receive data bit 2 to CPU
87	vcc3io	power	3.3 V i/o supply voltage
88	gndio	ground	i/o ground
89	gndk	ground	digital core ground
90	vcck	power	1.8 V digital core supply voltage
91	cpu_rxd[3]	output	cpu mii, receive data bit 3 to CPU
92	cpu_adrs[1]	input	cpu host interface, address bit 1
93	cpu_adrs[2]	input	cpu host interface, address bit 2
94	cpu_adrs[3]	input	cpu host interface, address bit 3
95	cpu_adrs[4]	input	cpu host interface, address bit 4
96	cpu_adrs[5]	input	cpu host interface, address bit 5
97	cpu_adrs[6]	input	cpu host interface, address bit 6
98	cpu_adrs[7]	input	cpu host interface, address bit 7
99	cpu_adrs[8]	input	cpu host interface, address bit 8
100	cpu_data[0]	bidir	cpu host interface, data bit 0
101	cpu_data[1]	bidir	cpu host interface, data bit 1
102	cpu_data[2]	bidir	cpu host interface, data bit 2
103	vcck	power	1.8 V digital core supply voltage
104	gndk	ground	digital core ground
105	gndio	ground	i/o ground
106	vcc3io	power	3.3 V i/o supply voltage
107	cpu_data[3]	bidir	cpu host interface, data bit 3
108	cpu_data[4]	bidir	cpu host interface, data bit 4
109	cpu_data[5]	bidir	cpu host interface, data bit 5
110	cpu_data[6]	bidir	cpu host interface, data bit 6
111	cpu_data[7]	bidir	cpu host interface, data bit 7
112	gndo	ground	i/o ground
113	vcc3o	power	3.3 V i/o supply voltage
114	cpu_data[8]	bidir	cpu host interface, data bit 8
115	cpu_data[9]	bidir	cpu host interface, data bit 0
116	cpu_data[10]	bidir	cpu host interface, data bit 10
117	cpu_data[11]	bidir	cpu host interface, data bit 11
118	cpu_data[12]	bidir	cpu host interface, data bit 12
119	vcc3io	power	3.3 V i/o supply voltage

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Pin	Signal Name	Type	LQFP Pin Descriptions
120	gndio	ground	i/o ground
121	gndk	ground	digital core ground
122	vcck	power	1.8 V digital core supply voltage
123	cpu_data[13]	bidir	cpu host interface, data bit 13
124	cpu_data[14]	bidir	cpu host interface, data bit 14
125	cpu_data[15]	bidir	cpu host interface, data bit 15
126	cpu_cs_n	input	cpu host interface, chip select, active low (internal pull-up)
127	cpu_rd_n	input	cpu host interface, read enable, active low (internal pull-up)
128	cpu_wr_n	input	cpu host interface, write enable, active low (internal pull-up)

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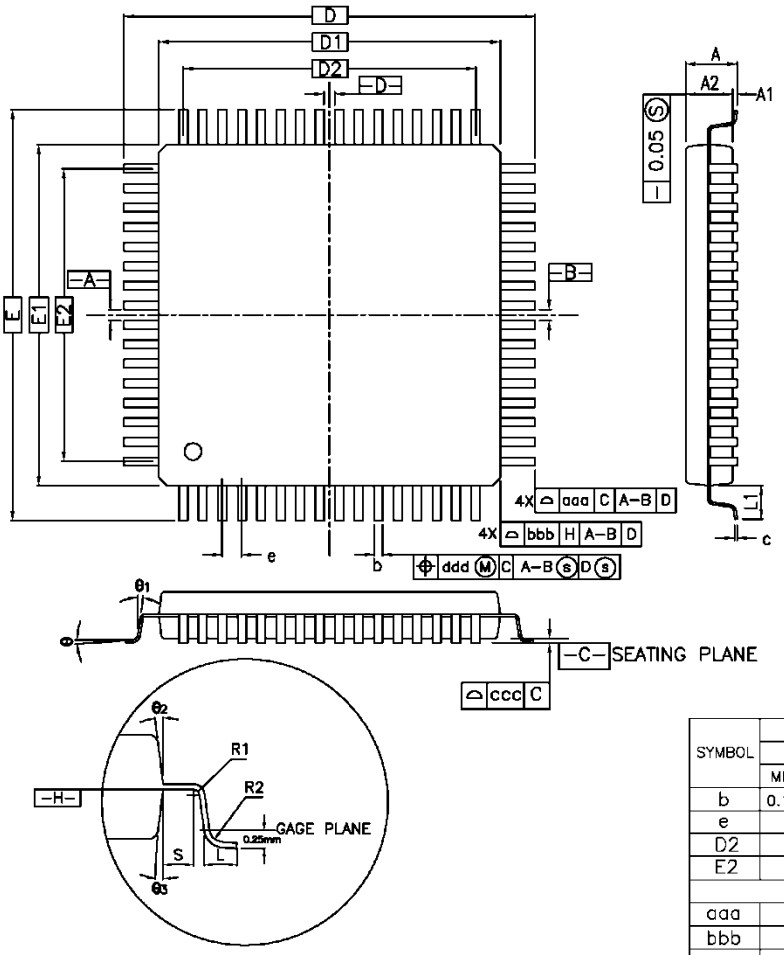
3.3 LQFP Package Physical Dimensions



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 128L WERE BASE ON THOSE OF 120L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

Figure 7 LQFP Package Physical Dimensions

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4 BGA Package

4.1 BGA Package Pinout

The pinout for the fido2100 Industrial Ethernet Switch BGA package is as shown in Figure 8. The corresponding pinout is provided in Table 2.

M	p1_lnk_stts	p2_txc	p2_txd[0]	p2_txd[2]	p2_rxc	p2_rxdv	p2_rxd[0]	p2_rxd[2]	p2_col	p2_lnk_stts	p2_led_grn	reset_n
L	p1_col	p1_led_grn	p2_txen	p2_txd[1]	p2_txd[3]	p2_rxer	p2_rxd[1]	p2_rxd[3]	p2_crs	p2_led_ylw	sys_clk	cpu_txen
K	p1_rxd[2]	p1_crs	p1_led_ylw	p2_txer	vcck	vcc3io	vcc3io	vcc3io	vcck	test	cpu_txer	cpu_txd[0]
J	p1_rxd[1]	p1_rxd[3]	vcck	vcck					gndio	vcc18a_pll	cpu_txc	cpu_txd[2]
H	p1_rxer	p1_rxd[0]	vcc3io		gndio	gndk	gndk	gndio		gnda_pll	cpu_txd[1]	cpu_txd[3]
G	p1_rxc	p1_rxdv	vcc3io		gndio	gndk	gndk	gndio		vcck	cpu_rxc	cpu_rxdv
F	p1_txd[3]	p1_txd[2]	vcc3io		gndio	gndk	gndk	gndio		vcc3io	cpu_rxer	cpu_crs
E	p1_txd[1]	p1_txd[0]	vcck		gndio	gndk	gndk	gndio		vcc3io	cpu_rxd[0]	cpu_col
D	p1_txer	p1_txc	vcck	gndio					vcck	vcc3io	cpu_rxd[2]	cpu_rxd[1]
C	p1_txen	event_1_sig	sw_event_irq_n	cpu_cs_n	vcc3io	cpu_data[9]	cpu_data[5]	vcc3io	cpu_adrs[8]	cpu_adrs[5]	cpu_adrs[2]	cpu_rxd[3]
B	event_2_sig	ts_event_irq_n	cpu_rd_n	cpu_data[14]	cpu_data[12]	cpu_data[10]	cpu_data[6]	cpu_data[3]	cpu_data[1]	cpu_adrs[7]	cpu_adrs[4]	cpu_adrs[1]
A	pps_sig	cpu_wr_n	cpu_data[15]	cpu_data[13]	cpu_data[11]	cpu_data[8]	cpu_data[7]	cpu_data[4]	cpu_data[2]	cpu_data[0]	cpu_adrs[6]	cpu_adrs[3]
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 8 fido2100 BGA Package Pinout

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4.2 BGA Pin Listing

Table 2 BGA Pin List

Pin	Signal Name	Type	BGA Pin Descriptions
C3	sw_event_irq_n	output	switch event IRQ, must be connected to a high priority IRQ pin on cpu
B2	ts_event_irq_n	output	time sync event IRQ. Optional for non-1588 devices.
A1	pps_sig	output	pulse per second signal for 1588 compliance
C2	event_1_sig	input	external event 1 snapshot trigger from CPU/others
B1	event_2_sig	input	external event 2 snapshot trigger from CPU/others
D2	p1_txc	input	port 1 mii, transmit clock from PHY
E3	vcck	power	1.8 V digital core supply voltage
E6	gndk	ground	digital core ground
F5	gndio	ground	i/o ground
F3	vcc3io	power	3.3 V i/o supply voltage
C1	p1_txen	output	port 1 mii, transmit enable to PHY
D1	p1_txer	output	port 1 mii, transmit error to PHY
E2	p1_txd[0]	output	port 1 mii, transmit data bit 0 to PHY
E1	p1_txd[1]	output	port 1 mii, transmit data bit 1 to PHY
F2	p1_txd[2]	output	port 1 mii, transmit data bit 2 to PHY
F1	p1_txd[3]	output	port 1 mii, transmit data bit 3 to PHY
G1	p1_rxc	input	port 1 mii, receive clock from PHY
G2	p1_rxdv	input	port 1 mii, receive data valid from PHY
H1	p1_rxer	input	port 1 mii, receive data error from PHY
H2	p1_rxd[0]	input	port 1 mii, receive data bit 0 from PHY
J1	p1_rxd[1]	input	port 1 mii, receive data bit 1 from PHY
K1	p1_rxd[2]	input	port 1 mii, receive data bit 2 from PHY
G3	vcc3io	power	3.3 V i/o supply voltage
G5	gndio	ground	i/o ground
F6	gndk	ground	digital core ground
J3	vcck	power	1.8 V digital core supply voltage
J2	p1_rxd[3]	input	port 1 mii, receive data bit 3 from PHY
L1	p1_col	input	port 1 mii, collision from PHY
K2	p1_crs	input	port 1 mii, carrier sense from PHY
M1	p1_lnk_stts	input	port 1 mii, link status from PHY (1:link pass, 0:link fail)
L2	p1_led_grn	output	port 1 mii,, green led
K3	p1_led_ylw	output	port 1 mii,, yellow led
M2	p2_txc	input	port 2 mii, transmit clock from PHY

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Pin	Signal Name	Type	BGA Pin Descriptions
L3	p2_txen	output	port 2 mii, transmit enable to PHY
K4	p2_txer	output	port 2 mii, transmit error to PHY
M3	p2_txd[0]	output	port 2 mii, transmit data bit 0 to PHY
L4	p2_txd[1]	output	port 2 mii, transmit data bit 1 to PHY
M4	p2_txd[2]	output	port 2 mii, transmit data bit 2 to PHY
J4	vcck	power	1.8 V digital core supply voltage
G6	gndk	ground	digital core ground
H5	gndio	ground	i/o ground
H3	vcc3io	power	3.3 V i/o supply voltage
L5	p2_txd[3]	output	port 2 mii, transmit data bit 3 to PHY
M5	p2_rxc	input	port 2 mii, receive clock from PHY
M6	p2_rxdv	input	port 2 mii, receive data valid from PHY
L6	p2_rxer	input	port 2 mii, receive data error from PHY
J9	gndio	ground	i/o ground
K6	vcc3io	power	3.3 V i/o supply voltage
M7	p2_rxd[0]	input	port 2 mii, receive data bit 0 from PHY
L7	p2_rxd[1]	input	port 2 mii, receive data bit 1 from PHY
M8	p2_rxd[2]	input	port 2 mii, receive data bit 2 from PHY
L8	p2_rxd[3]	input	port 2 mii, receive data, bit 3 from PHY
M9	p2_col	input	port 2 mii, collision from PHY
L9	p2_crs	input	port 2 mii, carrier sense from PHY
K7	vcc3io	power	3.3 V i/o supply voltage
H8	gndio	ground	i/o ground
H6	gndk	ground	digital core ground
K5	vcck	power	1.8 V digital core supply voltage
M10	p2_lnk_stts	input	port 2 mii, link status from PHY (1:link pass, 0:link fail)
M11	p2_led_grn	output	port 2 mii,, green led
L10	p2_led_ylw	output	port 2 mii,, yellow led
M12	reset_n	input	chip reset, active low (internal pull-up)
L11	sys_clk	input	25 MHz system clock
K10	test	input	test, active high (internal pull-down)
L12	cpu_txen	input	cpu mii, transmit enable from CPU
J10	vcc18a_pll	power	1.8 V analog supply voltage
H10	gnda_pll	ground	analog ground
K11	cpu_txer	input	cpu mii, transmit error from CPU
J11	cpu_txc	output	cpu mii, 25 MHz transmit clock to CPU
K12	cpu_txd[0]	input	cpu mii, transmit data bit 0 from CPU
K9	vcck	power	1.8 V digital core supply voltage

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Pin	Signal Name	Type	BGA Pin Descriptions
H7	gndk	ground	digital core ground
G8	gndio	ground	i/o ground
K8	vcc3io	power	3.3 V i/o supply voltage
H11	cpu_txd[1]	input	cpu mii, transmit data bit 1 from CPU
J12	cpu_txd[2]	input	cpu mii, transmit data bit 2 from CPU
H12	cpu_txd[3]	input	cpu mii, transmit data bit 3 from CPU
G11	cpu_rxc	output	cpu mii, 25 MHz receive clock to CPU
G12	cpu_rxdv	output	cpu_mii, receive data valid to CPU
F10	vcc3io	power	3.3 V i/o supply voltage
F11	cpu_rxer	output	cpu mii, receive error
F12	cpu_crs	output	cpu mii,
E12	cpu_col	output	cpu mii, collision
E11	cpu_rxd[0]	output	cpu mii, receive data bit 0 to CPU
D12	cpu_rxd[1]	output	cpu mii, receive data bit 1 to CPU
D11	cpu_rxd[2]	output	cpu mii, receive data bit 2 to CPU
E10	vcc3io	power	3.3 V i/o supply voltage
F8	gndio	ground	i/o ground
G7	gndk	ground	digital core ground
G10	vcck	power	1.8 V digital core supply voltage
C12	cpu_rxd[3]	output	cpu mii, receive data bit 3 to CPU
B12	cpu_adrs[1]	input	cpu host interface, address bit 1
C11	cpu_adrs[2]	input	cpu host interface, address bit 2
A12	cpu_adrs[3]	input	cpu host interface, address bit 3
B11	cpu_adrs[4]	input	cpu host interface, address bit 4
C10	cpu_adrs[5]	input	cpu host interface, address bit 5
A11	cpu_adrs[6]	input	cpu host interface, address bit 6
B10	cpu_adrs[7]	input	cpu host interface, address bit 7
C9	cpu_adrs[8]	input	cpu host interface, address bit 8
A10	cpu_data[0]	bidir	cpu host interface, data bit 0
B9	cpu_data[1]	bidir	cpu host interface, data bit 1
A9	cpu_data[2]	bidir	cpu host interface, data bit 2
D9	vcck	power	1.8 V digital core supply voltage
F7	gndk	ground	digital core ground
E8	gndio	ground	i/o ground
D10	vcc3io	power	3.3 V i/o supply voltage
B8	cpu_data[3]	bidir	cpu host interface, data bit 3
A8	cpu_data[4]	bidir	cpu host interface, data bit 4
C7	cpu_data[5]	bidir	cpu host interface, data bit 5

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Pin	Signal Name	Type	BGA Pin Descriptions
B7	cpu_data[6]	bidir	cpu host interface, data bit 6
A7	cpu_data[7]	bidir	cpu host interface, data bit 7
E5	gndio	ground	i/o ground
C8	vcc3io	power	3.3 V i/o supply voltage
A6	cpu_data[8]	bidir	cpu host interface, data bit 8
C6	cpu_data[9]	bidir	cpu host interface, data bit 0
B6	cpu_data[10]	bidir	cpu host interface, data bit 10
A5	cpu_data[11]	bidir	cpu host interface, data bit 11
B5	cpu_data[12]	bidir	cpu host interface, data bit 12
C5	vcc3io	power	3.3 V i/o supply voltage
D4	gndio	ground	i/o ground
E7	gndk	ground	digital core ground
D3	vcck	power	1.8 V digital core supply voltage
A4	cpu_data[13]	bidir	cpu host interface, data bit 13
B4	cpu_data[14]	bidir	cpu host interface, data bit 14
A3	cpu_data[15]	bidir	cpu host interface, data bit 15
C4	cpu_cs_n	input	cpu host interface, chip select, active low (internal pull-up)
B3	cpu_rd_n	input	cpu host interface, read enable, active low (internal pull-up)
A2	cpu_wr_n	input	cpu host interface, write enable, active low (internal pull-up)

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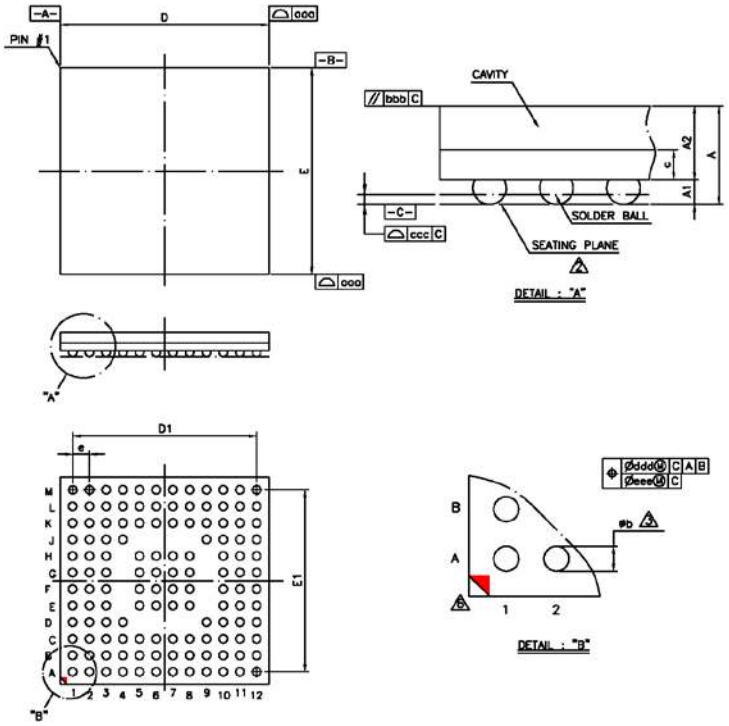
4.3 BGA Package Physical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	8.80	---	---	0.346	---
E1	---	8.80	---	---	0.346	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa						
bbb						
ccc						
ddd						
eee						
MD/ME						

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-205.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

Figure 9 BGA Package Physical Dimensions

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5 Electrical Characteristics

Tables 3 through 7 show the absolute maximum ratings, ESD and latch-up characteristics, recommended operating conditions, DC Characteristics of I/O cells and power consumption.

Table 3 Absolute Maximum Ratings

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
vcck	digital core supply voltage		-0.5	-	2.5	V
vcc18a_pll	pll analog supply voltage		-0.5	-	2.5	V
vcc3io	digital i/o supply voltage		-0.5	-	4.6	V
vcc3o	digital i/o supply voltage		-0.5	-	4.6	V
T_{STG}	Storage Temperature		-65	-	150	^oC
T_J	Operating Junction Temperature		-40	-	125	^oC

Table 4 ESD and Latch-Up Characteristics

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{HBM}	Human Body Model		2000			V
V_{MM}	Machine Model		200			V
I_{LATP}	Positive Latch-Up				50	µA
I_{LATN}	Negative Latch-Up				-50	µA

Table 5 Recommended Operating Conditions

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
vcck	digital core supply voltage		1.62	1.8	1.98	V
vcc18a_pll	pll analog supply voltage		1.62	1.8	1.98	V
vcc3io	digital i/o supply voltage		3.0	3.3	3.6	V
vcc3o	digital i/o supply voltage		3.0	3.3	3.6	V
T_A	Ambient Temperature		-40	-	85	^oC
sys_clk	system clock		-	25	-	MHz

Table 6 DC Characteristics of I/O Cells

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{IH}	input high voltage		2.0	-	-	V
V_{IL}	input low voltage		-	-	0.8	V
V_{OH}	output high voltage	I_{OH} = -12 mA	2.4	-	-	V
V_{OL}	output low voltage	I_{OL} = 12 mA	-	-	0.4	V
R_{PU}	Input pull-up resistance		40	75	190	kΩ
R_{PD}	Input pull-down resistance		40	75	190	kΩ
C_{IN}	Input Capacitance			2.4		pF

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Table 7 Power Consumption (Nominal)

I/O Voltage 3.3VDC		Core Voltage 1.8VDC		PLL Voltage 1.8VDC		Total
Current	Power	Current	Power	Current	Power	Power
5.27mA	17.39mW	60.0mA	108.0mW	.663mA	1.19mW	126.6mW

5.1 Thermal Characteristics

The thermal resistance characteristics for the LQFP and the BGA packages are provided in Table 8. All data is simulated based on the 2S2P board type. The board type is defined by JEDEC standard JESD51-7 for the PQFP package, and by JESD51-9 for the BGA package.

Table 8 Thermal Resistance Characteristics

Name	Description	Airflow (m/S)	BGA	LQFP
θ_{JC} (°C/W)	Junction to Case	0	8.03	17.5
θ_{JA} (°C/W)	Junction to Ambient	0	34.09	52.0

5.2 PLL Supply

The PLL for the fido2100 has dedicated supply and ground pins. For best performance of the PLL it is desirable to provide a quiet or separate 1.8 V supply. Decoupling capacitors of 0.1 uF and 10 uF should be placed on the board closely to the vdd18a_pll and gnda_pll pins. If the digital supply is to be used, it is best to also place a series ferrite bead before the decoupling capacitors and add additional decoupling capacitance of 0.1nF and 10nF.

5.3 System Clock Input

The system clock input (sys_clk) requires a rail-to-rail clock input at 25 MHz. This 25 MHz clock input is then used by the PLL the create the necessary internal clocks for the fido2100.

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5.4 RESET: Power-On-Reset, Hardware Reset and Software Reset

5.4.1 Power-On-Reset

The fido2100 has an internal power-on-reset (POR) circuit which will provide a reset of the PLL and the *rst* bit of the Switch Control Register when *vcck* power is applied. The POR circuit will keep the PLL and *rst* bit in reset until the *vcck* power has exceeded a 1.2 V threshold. Once the *vcck* voltage has exceeded the POR threshold the PLL will then need a minimum time of 60 ns to lock and provide a stable clock source.

5.4.2 Hardware Reset

There is also a reset input (reset_n) provided for a hardware reset of the fido2100. When *reset_n* is asserted low the POR circuit will reset the PLL and the *rst* bit of the Switch Control Register. The *reset_n* input must be asserted low for a minimum of 20 ns in order to assure a reset has occurred. On a reset, once the reset_n input has been de-asserted high, the PLL will then need a minimum time of 60 ns to lock and provide a stable clock source. The *reset_n* input has an internal pull-up which is intended to prevent a reset if the input is un-driven.

5.4.3 Software Reset

Software reset of the fido2100 is accomplished by writing a '1' to the *rst* bit of the Switch Control Register. The *rst* bit is self-clearing on the next clock. When this bit is set, the control and status registers return to their default conditions.

5.5 Test Input

The test input (test) should be tied low externally for normal operation. There are no user selectable tests. The *test* input has an internal pull-down which is intended to prevent a entering test mode if the input is un-driven.

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6 Host Bus Interface

The Host Bus Interface is used to read and/or write the various configuration and data registers within the fido2100. The Host Bus Interface consists of the following inputs, an 8-bit address bus (cpu_adrs[8:1]), a chip select (cpu_cs_n), a read select (cpu_rd_n) and a write select (cpu_wr_n), along with a 16-bit bidirectional data bus (cpu_data[15:0]).

6.1 READ, Host Bus Interface

A READ is accomplished by selecting a register address using input *cpu_adrs[8:1]*, then asserting both *cpu_cs_n* and *cpu_rd_n* inputs for a sufficient time. The contents of the register READ will be output on *cpu_data[15:0]*. The input *cpu_wr_n* must not be asserted during a READ operation. A typical READ operation, with necessary timing, can be seen below in Figure 10. During the READ operation the timing between *cpu_cs_n* and *cpu_rd_n* is not critical, however the actual READ cycle begins when both signals are asserted low with the last asserted signal determining the timing. The READ cycle will end when either *cpu_cs_n* or *cpu_rd_n* are de-asserted high. In the timing diagram of Figure 10, timing is shown only from *cpu_rd_n* for simplicity.

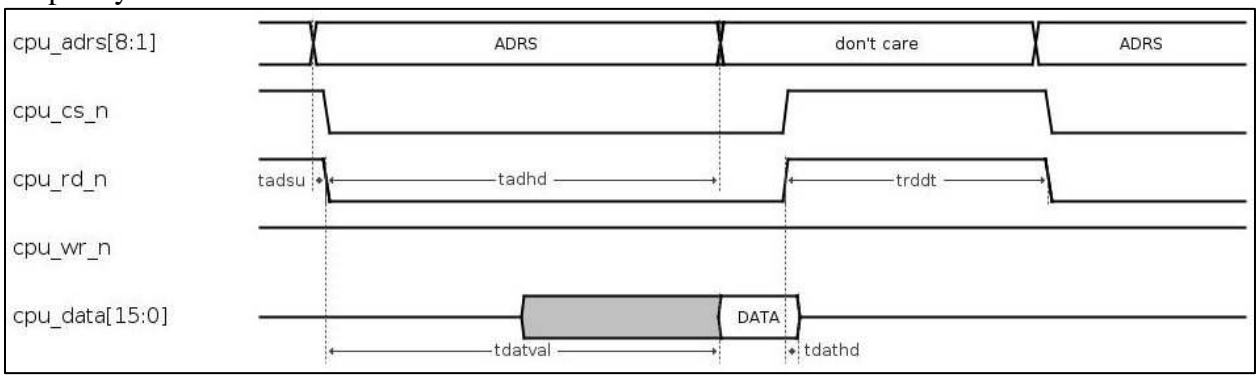

Figure 10 Host Interface, READ Timing

Table 9 Host Interface, READ Timing

Description	Symbol	min	max	unit
cpu_adrs SETUP time	tadsu	0		ns
cpu_adrs HOLD time	tadhd	60		ns
cpu_data VALID time	tdatval	60		ns
cpu_data HOLD time	tdathd		0	ns
cpu_rd_n DEAD time	trddt	40		ns

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6.2 WRITE, Host Bus Interface

A WRITE is accomplished by selecting a register address using input *cpu_adrs[8:1]*, placing data on *cpu_data[15:0]*, and then asserting both *cpu_cs_n* and *cpu_wr_n* inputs for a sufficient time. The data on the cpu_data[15:0] bus will then be written to the selected register. The input *cpu_rd_n* must not be asserted during a WRITE operation. A typical WRITE operation, with necessary timing, can be seen below in Figure 11. During the WRITE operation the timing between *cpu_cs_n* and *cpu_wr_n* is not critical, however the actual WRITE cycle begins when both signals are asserted low with the last asserted signal determining the timing. The WRITE cycle will end when either *cpu_cs_n* or *cpu_wr_n* are de-asserted high. In the timing diagram of Figure 11, timing is shown only from *cpu_wr_n* for simplicity.

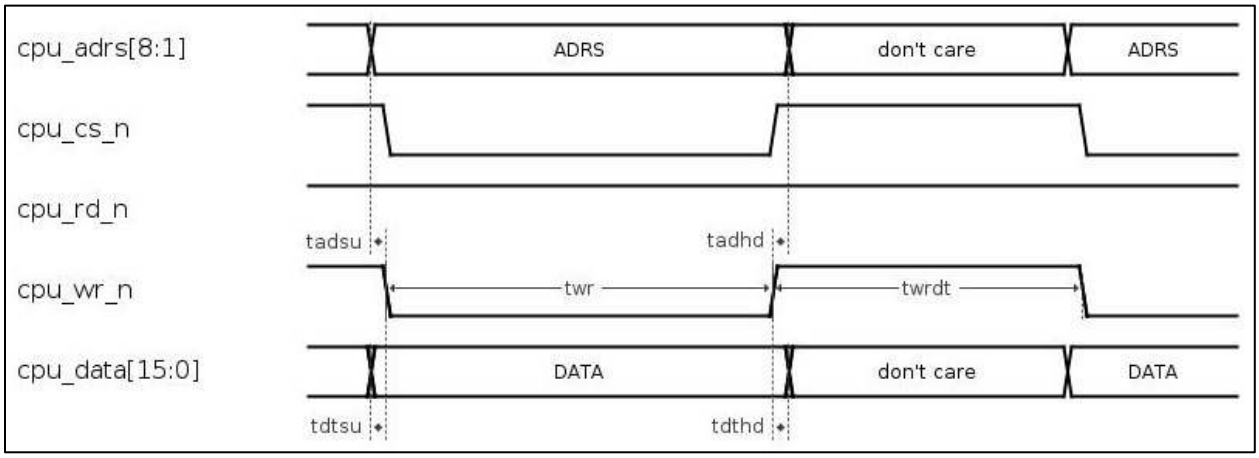

Figure 11 Host Interface, WRITE Timing

Table 10 Host Interface, WRITE Timing

Description	Symbol	min	max	unit
cpu_adrs SETUP time	tadsu	0		ns
cpu_adrs HOLD time	tadhd	0		ns
cpu_data SETUP time	tdtsu	0		ns
cpu_data HOLD time	tdthd	0		ns
cpu_wr_n WRITE time	twr	50		ns
cpu_wr_n DEAD time	twrdt	40		ns

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7 External MII Interface

The two external ports, port 1 and port 2, of the 3-Port Industrial Ethernet Switch are connected to their respective physical layer transceivers (PHY) through an IEEE 802.3 media independent interface (MII). The MII interface is comprised of 16 pins: transmit clock (px_txc), transmit enable (px_txen), transmit error (px_txer), transmit data (px_txd[3:0]), receive clock (px_rxc), receive data valid (px_rxdv), receive data error (px_rxer), receive data (px_rxd[3:0]), collision (px_col) and carrier sense (px_crs).

7.1 RECEIVE DATA, External MII Interface

An Ethernet packet received by the PHY will be transmitted to its respective port via an MII interface. The PHY will transmit this data using the MII inputs: *px_rxc*, *px_rxdv*, *px_rxer* and *px_rxd[3:0]*. Timing for the RECEIVE DATA is shown below in Figure 12.

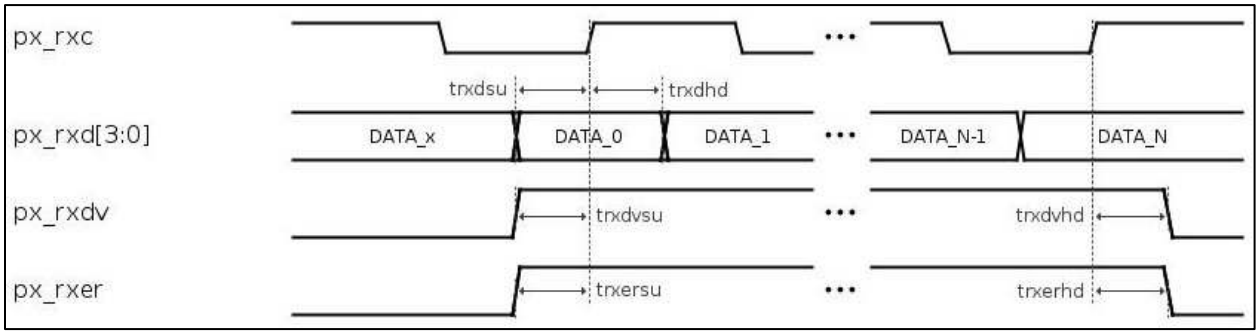

Figure 12 External MII Interface, RECEIVE DATA

Table 11 RECEIVE DATA, External MII Interface

Description	Symbol	min	max	unit
Receive Data SETUP time	trxdsu	10		ns
Receive Data HOLD time	trxdhd	10		ns
Receive Data Valid SETUP time	trxdvsu	10		ns
Receive Data Valid HOLD time	trxdvhd	10		ns
Receive Data Error SETUP time	trxersu	10		ns
Receive Data Error HOLD time	trxerhd	10		ns

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7.2 TRANSMIT DATA, External MII Interface

An Ethernet packet to be transmitted will be sent to its respective PHY via an MII interface. The PHY will transmit this data using the MII inputs: *px_txc*, *px_txen*, *px_txer* and *px_txd[3:0]*. Timing for the TRANSMIT DATA is shown below in Figure 13.

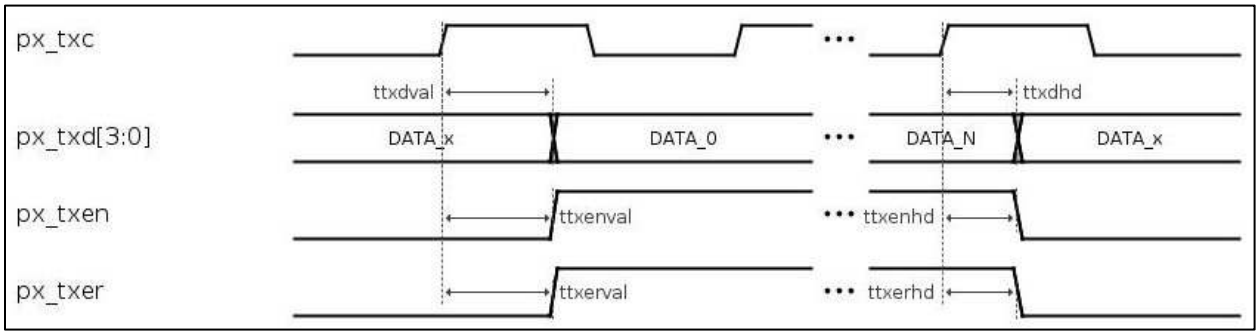

Figure 13 External MII Interface, TRANSMIT DATA

Table 12 TRANSMIT DATA, External MII Interface

Description	Symbol	min	max	unit
Transmit Data VALID time	ttxdval	15		ns
Transmit Data HOLD time	ttxdhd	0		ns
Transmit Data Enable VALID time	ttxenval	15		ns
Transmit Data Valid HOLD time	ttcenhd	0		ns
Transmit Data Error VALID time	ttxerval	15		ns
Transmit Data Error HOLD time	ttxerhd	0		ns

8 Internal MII Interface

The single internal port, port CPU, of the 3-Port Industrial Ethernet Switch acts as a physical layer transceivers (PHY) media independent interface (MII). This MII interface is comprised of 16 pins: transmit clock (cpu_txc), transmit enable (cpu_txen), transmit error (cpu_txer), transmit data (cpu_txd[3:0]), receive clock (cpu_rxc), receive data valid (cpu_rxdv), receive data error (cpu_rxer), receive data (cpu_rxd[3:0]), collision (cpu_col) and carrier sense (cpu_crs). However, as the Internal MII Interface always runs at 100MB and Full-Duplex, the output *cpu_col* is always low and the output *cpu_crs* is the same as *cpu_rxdv*.

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8.1 RECEIVE DATA, Internal MII Interface

An Ethernet packet received by the PHY will be transmitted to its respective port via an MII interface. The PHY will transmit this data using the MII inputs: *px_rxc*, *px_rxdv*, *px_rxer* and *px_rxd[3:0]*. Timing for the RECEIVE DATA is shown below in Figure 14.

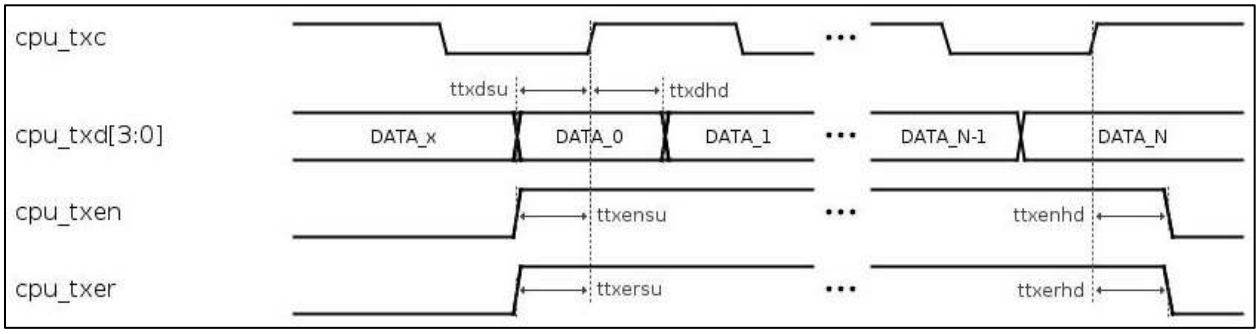

Figure 14 Internal MII Interface, RECEIVE DATA

Table 13 RECEIVE DATA, External MII Interface

Description	Symbol	min	max	unit
Receive Data SETUP time	ttxdsu	10		ns
Receive Data HOLD time	ttxdhd	10		ns
Receive Data Enable SETUP time	ttxensu	10		ns
Receive Data Enable HOLD time	ttxenhd	10		ns
Receive Data Error SETUP time	ttxersu	10		ns
Receive Data Error HOLD time	ttxerhd	10		ns

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8.2 TRANSMIT DATA, Internal MII Interface

An Ethernet packet to be transmitted will be sent to its respective PHY via an MII interface. The PHY will transmit this data using the MII inputs: *px_txc*, *px_txen*, *px_txer* and *px_txd[3:0]*. Timing for the TRANSMIT DATA is shown below in Figure 15.

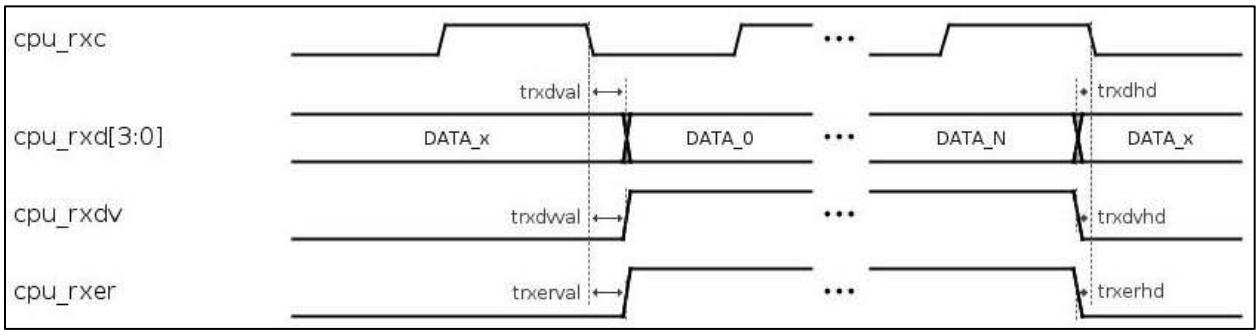

Figure 15 Internal MII Interface, TRANSMIT DATA

Table 14 TRANSMIT DATA, External MII Interface

Description	Symbol	min	max	unit
Transmit Data VALID time	trxdval	5		ns
Transmit Data HOLD time	trxdhd	0		ns
Transmit Data Valid VALID time	trxdvval	5		ns
Transmit Data Valid HOLD time	trxdvhd	0		ns
Transmit Data Error VALID time	trxerval	5		ns
Transmit Data Error HOLD time	trxerhd	0		ns

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9 Control and Status Registers

Table 13 below contains a listing of all Control & Status Registers accessible from the Host Bus Interface. The table includes the address, register name, a register mnemonic and the read/write status of the register. A detailed explanation of the registers is also included in this section following the table.

9.1 Register Map

Table 15 Register Map

Address Offset (cpu_adrs[8:0])	**Function**	**Mnemonic**	**R/W**
0x00	Time Sync Control	TS_Control	R/W
0x02	Time Sync IRQ Event	TS_Event	R/W
0x04	Addend_Low	Addend_Lo	R/W
0x06	Addend_High	Addend_Hi	R/W
0x08	Accumulator_Low	Accum_Lo	R/W
0x0A	Accumulator_High	Accum_Hi	R/W
0x0C	SystemTime_Low_Low	SysTime_Lo_Lo	R/W
0x0E	SystemTime_Low_High	SysTime_Lo_Hi	R/W
0x10	SystemTime_High_Low	SysTime_Hi_Lo	R/W
0x12	SystemTime_High_High	SysTime_Hi_Hi	R/W
0x14	TargetTime1_Low_Low	TgtTim1_Lo_Lo	R/W
0x16	TargetTime1_Low_High	TgtTim1_Lo_Hi	R/W
0x18	TargetTime1_High_Low	TgtTim1_Hi_Lo	R/W
0x1A	TargetTime1_High-High	TgtTim1_Hi_Hi	R/W
0x1C	TargetTime2_Low_Low	TgtTim2_Lo_Lo	R/W
0x1E	TargetTime2_Low_High	TgtTim2_Lo_Hi	R/W
0x20	TargetTime2_High_Low	TgtTim2_Hi_Lo	R/W
0x22	TargetTime2_High_High	TgtTim2_Hi_Hi	R/W
0x24	Event1Snap_Low_Low	Evnt1_Lo_Lo	R

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Address Offset (cpu_adrs[8:0])	**Function**	**Mnemonic**	**R/W**
0x26	Event1Snap_Low_High	Evnt1_Lo_Hi	R
0x28	Event1Snap_High_Low	Evnt1_Hi_Lo	R
0x2A	Event1Snap_High_High	Evnt1_Hi_Hi	R
0x2C	Event2Snap_Low_Low	Evnt2_Lo_Lo	R
0x2E	Event2Snap_Low_High	Evnt2_Lo_Hi	R
0x30	Event2Snap_High_Low	Evnt2_Hi_Lo	R
0x32	Event2Snap_High_High	Evnt2_Hi_Hi	R
0x34	Xmit_SnapShot_Low_Low	TxTS_Lo_Lo	R
0x36	Xmit_SnapShot_Low_High	TxTS_Lo_Hi	R
0x38	Xmit_SnapShot_High_Low	TxTS_Hi_Lo	R
0x3A	Xmit_SnapShot_High_High	TxTS_Hi_Hi	R
0x3C	Recv_Snapshot_Low_Low	RxTS_Lo_Lo	R
0x3E	Recv_Snapshot_Low_High	RxTS_Lo_Hi	R
0x40	Recv_Snapshot_High_Low	RxTS_Hi_Lo	R
0x42	Recv_Snapshot_High_High	RxTS_Hi_Hi	R
0x44	Recv_SourceID_Low_Low	RxID_Lo_Lo	R
0x46	Recv_SourceID_Low_High	RxID_Lo_Hi	R
0x48	Recv_SourceID_High_Low	RxID_Hi_Lo	R
0x4A	Recv_SourceID_High_High	RxID_Hi_Hi	R
0x4C	Recv_SequenceID	RxSeqID	R
0x4E	PTP Sub-domain	Subdomain	R/W
0x50	Switch Control	SW_Control	R/W
0x52	Switch IRQ Event	SW_Event	R/W
0x54	Switch IRQ Mask	SW_Mask	R/W
0x56	Port 1 Seed	Prt1Seed	R/W
0x58	Port 2 Seed	Prt2Seed	R/W
0x5A	MACAddress_Low_Low	MAC_Lo_Lo	R/W

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Address Offset (cpu_adrs[8:0])	**Function**	**Mnemonic**	**R/W**
0x5C	MACAddress_Low_High	MAC_Lo_Hi	R/W
0x5E	MACAddress_High_Low	MAC_Hi_Lo	R/W
0x60	Multicast_Hash_Filter_Index	MCHFI	R/W
0x62	Multicast_Hash_Filter_Value	MCHFV	R/W
0x64	Free_Running_Timer_Low	FreeTmr_Lo	R
0x66	Free_Running_Timer_High	FreeTmr_Hi	R
0x68	PIT_Timeout_Low	PITTmo_Lo	R
0x6A	PIT_Timeout_High	PITTmo_Hi	R
0x6C	Redundancy Control	Rdndnc_Control	R/W
0x6E	Ring Beacon State	Rng_BcnState	R
0x70	Beacon_Timeout_Low	BcnTmo_Lo	R/W
0x72	Beacon_Timeout_High	BcnTmo_Hi	R/W
0x74	Port1_Recv_Beacon_TS_Low	P1BcnTS_Lo	R
0x76	Port1_Recv_Beacon_TS_High	P1BcnTS_Hi	R
0x78	Port2_Recv_Beacon_TS_Low	P2BcnTS_Lo	R
0x7A	Port2_Recv_Beacon_TS_High	P2BcnTS_Hi	R
0x7C	Port1_Neighbor_Check_SrcId_Low_Low	P1NChkSId_Lo_Lo	R
0x7E	Port1_Neighbor_Check_SrcId_Low_High	P1NChkSId_Lo_Hi	R
0x80	Port1_Neighbor_Check_SrcId_High_Low	P1NChkSId_Hi_Lo	R
0x82	Port2_Neighbor_Check_SrcId_Low_Low	P2NChkSId_Lo_Lo	R
0x84	Port2_Neighbor_Check_SrcId_Low_High	P2NChkSId_Lo_Hi	R
0x86	Port2_Neighbor_Check_SrcId_High_Low	P2NChkSId_Hi_Lo	R
0x88	Port1_Neighbor_Status_SrcId_Low_Low	P1NStsSId_Lo_Lo	R
0x8A	Port1_Neighbor_Status_SrcId_Low_High	P1NStsSId_Lo_Hi	R
0x8C	Port1_Neighbor_Status_SrcId_High_Low	P1NStsSId_Hi_Lo	R
0x8E	Port2_Neighbor_Status_SrcId_Low_Low	P2NStsSId_Lo_Lo	R
0x90	Port2_Neighbor_Status_SrcId_Low_High	P2NStsSId_Lo_Hi	R

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Address Offset (cpu_adrs[8:0])	**Function**	**Mnemonic**	**R/W**
0x92	Port2_Neighbor_Status_SrcId_High_Low	P2NStsSId_Hi_Lo	R
0x94	Ring_Supervisor_MacId_Low_Low	RngSprvsrId_Lo_Lo	R/W
0x96	Ring_Supervisor_MacId_Low_High	RngSprvsrId_Lo_Hi	R/W
0x98	Ring_Supervisor_MacId_High_Low	RngSprvsrId_Hi_Lo	R/W
0x9A	Reserved		R
0x9C	Port1_Recv_Group_Frame_Count	P1RxGrpFrmCnt	R
0x9E	Port2_Recv_Group_Frame_Count	P2RxGrpFrmCnt	R
0xA0	Port1_Recv_Unicast_Frame_Count	P1RxUniFrmCnt	R
0xA2	Port2_Recv_Unicast_Frame_Count	P2RxUniFrmCnt	R
0xA4	Port1_Recv_Byte_Count_Low	P1RxBytCnt_Lo	R
0xA6	Port1_Recv_Byte_Count_High	P1RxBytCnt_Hi	R
0xA8	Port2_Recv_Byte_Count_Low	P2RxBytCnt_Lo	R
0xAA	Port2_Recv_Byte_Count_High	P2RxBytCnt_Hi	R
0xAC	Port1_Recv_Large_Error_Frame_Count	P1RxLrgFrmCnt	R
0xAE	Port2_Recv_Large_Error_Frame_Count	P2RxLrgFrmCnt	R
0xB0	Port1_Recv_Align_Error_Frame_Count	P1RxAlnFrmCnt	R
0xB2	Port2_Recv_Align_Error_Frame_Count	P2RxAlnFrmCnt	R
0xB4	Port1_Recv_FCS_Error_Frame_Count	P1RxFcsFrmCnt	R
0xB6	Port2_Recv_FCS_Error_Frame_Count	P2RxFcsFrmCnt	R
0xB8	Port1_Recv_Error_Frame_Count	P1RxErrFrmCnt	R
0xBA	Port2_Recv_Error_Frame_Count	P2RxErrFrmCnt	R
0xBC	Port1_Xmit_Group_Frame_Count	P1TxGrpFrmCnt	R
0xBE	Port2_Xmit_Group_Frame_Count	P2TxGrpFrmCnt	R
0xC0	Port1_Xmit_Unicast_Frame_Count	P1TxUniFrmCnt	R
0xC2	Port2_Xmit_Unicast_Frame_Count	P2TxUniFrmCnt	R
0xC4	Port1_Xmit_Byte_Count_Low	P1TxBytCnt_Lo	R
0xC6	Port1_Xmit_Byte_Count_High	P1TxBytCnt_Hi	R

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Address Offset (cpu_adrs[8:0])	**Function**	**Mnemonic**	**R/W**
0xC8	Port2_Xmit_Byte_Count_Low	P2TxBytCnt_Lo	R
0xCA	Port2_Xmit_Byte_Count_High	P2TxBytCnt_Hi	R
0xCC	Port1_Xmit_Single_Collision_Frame_Count	P1TxSClFrmCnt	R
0xCE	Port2_Xmit_Single_Collision_Frame_Count	P2TxSClFrmCnt	R
0xD0	Port1_Xmit_Multi_Collision_Frame_Count	P1TxMClFrmCnt	R
0xD2	Port2_Xmit_Multi_Collision_Frame_Count	P2TxMClFrmCnt	R
0xD4	Port1_Xmit_Excess_Collision_Frame_Count	P1TxXClFrmCnt	R
0xD6	Port2_Xmit_Excess_Collision_Frame_Count	P2TxXClFrmCnt	R
0xD8	Port1_Xmit_Error_Frame_Count	P1TxErrFrmCnt	R
0xDA	Port2_Xmit_Error_Frame_Count	P2TxErrFrmCnt	R
0xDC	Beacon_Generation_Control	BcnGenCntrl	R/W
0xDE	Beacon_Interval_Low	BcnIntrvl_Lo	R/W
0xE0	Beacon_Interval_High	BcnIntrvl_Hi	R/W
0xE2	Beacon_Data_Index	BcnDataIdx	R/W
0xE4	Beacon_Data_Value	BcnDataVal	R/W
0xE6	Embedded_Switch_Version	EmbSwtchVer	R

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9.2 Detailed Register Explanations

9.2.1 Time Sync Control Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_Control	R/W	0x00								rxm	txm	mm	ppse	tte2	tte1	evm2	evm1	ttm2	ttm1
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ttm1-2 **Target Time Interrupt Mask 1-2**. The Target Time interrupt mask 1-2 controls whether the corresponding Target Time interrupt is passed to the Host processor. When any of these bits are set, the corresponding interrupt to the Host is enabled. When any of these bits are cleared, the corresponding Target Time interrupt to the Host is disabled.

evm1 **Event 1 Interrupt Mask**. The interrupt for the Host is always disabled, regardless of the state of this bit.

evm2 **Event 2 Interrupt Mask**. The interrupt for the Host is always disabled, regardless of the state of this bit.

tte1-2 **Target Time Interrupt Enable 1-2**. The Target Time interrupt enable 1-2 controls whether the corresponding Target Time interrupt is enabled. When any of these bits are set, the corresponding Target Time Register is compared with System Time Register. When they match, the corresponding ttp1-2 bit in TS_Event register is set and the corresponding tte1-2 bit is reset. If the corresponding ttm1-2 bit is also set then an interrupt is delivered to the Host. To prevent spurious interrupts firmware should write to Target Time Registers 1-2, only when corresponding tte1-2 is not set.

ppse **Pulse Per Second Enable**. When this bit is set, the state of ttp2 bit in the TS_Event register is reflected on output pin pps_sig.

mm **Master Mode**. When this bit is set, the Time Sync logic implementing IEEE 1588 ordinary clock hardware assist on the local port connected to the host CPU MII interface, will operate in master mode. When this bit is reset the same logic will operate in slave mode.

txm **Transmit Snapshot Interrupt Mask**. The transmit snapshot interrupt mask controls whether the transmit snapshot txs bit in the TS_Event register, should interrupt the Host processor. When this bit is set, the interrupt to the Host is enabled. When cleared, the interrupt to the Host is disabled.

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rxm **Receive Snapshot Interrupt Mask**. The receive snapshot interrupt mask controls whether the receive snapshot rxs bit in the TS_Event register, should interrupt the Host processor. When this bit is set, the interrupt to the Host is enabled. When cleared, the interrupt to the Host is disabled.

9.2.2 Time Sync Interrupt Event Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_Event	R/W	0x02												rxs	txs	evs2	evs1	ttp2	ttp1
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

All interrupt requests from Time Sync Event register will be delivered to the host CPU through the *ts_event_irq_n* signal.

ttp1-2 **Target Time Interrupt Pending 1-2**. The Target Time interrupt pending 1-2 indicates if the corresponding Target Time register matched the System Time, as explained under tte1-2 in the Time Sync Control register. If corresponding ttm1-2 bit in the Time Sync Control register is also set, an interrupt will be delivered to the Host. ttp1-2 can be reset by writing a '1' to it.

evs1 **Event 1 Snapshot**. A rising edge on the input pin event_1_sig causes a snapshot of the System Time to be saved in the External Event 1 Snapshot register, and the evs1 bit to be set. After an event_1_sig, polling of this register should take place in order to determine that a snapshot has taken place when evs1 is set. Now the External Event 1 Snapshot register can be read. A subsequent rising edge will not cause the snapshot to be updated while the evs1 bit is set. This bit can be reset by writing a '1' to it.

evs2 **Event 2 Snapshot**. A rising edge on the input pin event_2_sig causes a snapshot of the System Time to be saved in the External Event 2 Snapshot register, and the evs2 bit to be set. After an event_2_sig, polling of this register should take place in order to determine that a snapshot has taken place when evs2 is set. Now the External Event 2 Snapshot register can be read. A subsequent rising edge will not cause the snapshot to be updated while the evs2 bit is set. This bit can be reset by writing a '1' to it.

txs **Transmit Snapshot**. A Sync frame in master mode or Delay_Req frame in slave mode will cause a snapshot of the System time to be saved in the Transmit Snapshot register and the txs bit to be set. Subsequent Sync/Delay_Req frames will not cause the snapshot to be updated while the

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txs bit is set. If this bit is set and the txm bit in TS_Control register is also set, an interrupt will be delivered to the Host. This bit can be reset by writing a '1' to it.

rxs **Receive Snapshot**. A Sync frame in slave mode or a Delay_Req frame in master mode will cause a snapshot of the System time to be saved in the Receive Snapshot register, the source ID/sequence ID of incoming frame to be saved in the Receive Source ID/Sequence ID registers and the rxs bit to be set. Up to 16 snapshots will be stored in the FIFO if firmware is slow to process them. If the FIFO is full, subsequent Sync/Delay_Req frames will not cause a snapshot/source ID/sequence ID to be stored. If this bit is set and the rxm bit in TS_Control register is also set, an interrupt will be delivered to the Host. This bit can be reset by writing a '1' to it. If the bit doesn't reset, it indicates additional snapshots are present. Firmware should repeatedly read and store all entries from the FIFO until this bit is reset.

9.2.3 Addend Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addend_Lo	R/W	0x04		Addend[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addend_Hi	R/W	0x06		Addend[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Addend register consists of two 16-bit registers. The Addend register contains the frequency scaling value used by a firmware algorithm to achieve time synchronization in the module. The value in this register is added to the value in the Accumulator. When the Accumulator rolls over, an overflow pulse is asserted and increments system time. Because the Addend register is cleared at reset, it must be written with a non-zero value to allow system time to increment. Reads of the two 16-bit registers can be performed in any order. When performing writes, Addend_Lo should be written first. When Addend_Hi is written later, an internal addend register will be updated with the full 32-bit value.

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9.2.4 Accumulator Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Accum_Lo	R/W	0x08		Accumulator[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Accum_Hi	R/W	0x0A		Accumulator[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Accumulator register consists of two 16-bit registers. The Accumulator register serves as a precision frequency divider in the time synchronization logic. Firmware calculates a frequency scaling value to be written to the Addend register. The data in the Accumulator register is added to the value in the Addend register once every period of the system clock. When the Accumulator rolls over, an overflow pulse is asserted which increments the value in the system timer. This register is not read or written to in normal operation. When performing reads, Accum_Lo should be read first, which will cause the higher 16 bits of the internal accumulator register to be latched and when Accum_Hi is read later, the latched value will be returned. When performing writes, Accum_Lo should be written first and when Accum _Hi is written later, the internal accumulator register will be updated with the full 32-bit value.

9.2.5 System Time Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SysTime_Lo_Lo	R/W	0x0C		Systime[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SysTime_Lo_Hi	R/W	0x0E		Systime[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SysTime_Hi_Lo	R/W	0x10		Systime[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SysTime_Hi_Hi	R/W	0x12		Systime[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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The System Time register consists of four 16-bit registers. The system timer is a loadable up-counter and reflects the local time in the module. The system timer is incremented when the Accumulator register rolls over. When performing reads, SysTime_Lo_Lo should be read first, which will cause the higher 48-bits of the internal system time register to be latched. When other SysTime_XX_XX registers are read later, the latched value will be returned. When performing writes, the lower three SysTime_XX_XX should be written first, and when SysTime_Hi_Hi is written later, the internal system time register will be updated with the full 64 bit value.

9.2.6 Target Time1 Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim1_Lo_Lo	R/W	0x14		Target1[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim1_Lo_Hi	R/W	0x16		Target1[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim1_Hi_Lo	R/W	0x18		Target1[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim1_Hi_Hi	R/W	0x1A		Target1[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Target Time1 register consists of four 16-bit registers. When the system time is equal to the target time value, the ttp1 bit in the Time Sync Event register is set and an interrupt is generated to the Host if the ttm1 bit in the Time Sync Control register is also set. Reads and writes of four 16-bit registers can be performed in any order. In order to prevent spurious interrupts during writes, the tte1 bit should be ‘0’ in the Time Sync Control register when writing to any of the four 16-bit registers.

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9.2.7 Target Time2 Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim2_Lo_Lo	R/W	0x1C		Target2[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim2_Lo_Hi	R/W	0x1E		Target2[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim2_Hi_Lo	R/W	0x20		Target2[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TgtTim2_Hi_Hi	R/W	0x22		Target2[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Target Time2 register consists of four 16-bit registers. When the system time is equal to the target time value, the ttp2 bit in the Time Sync Event register is set and an interrupt is generated to the Host if the ttm2 bit in the Time Sync Control register is also set. Reads and writes of four 16-bit registers can be performed in any order. In order to prevent spurious interrupts during writes, the tte2 bit should be '0' in the Time Sync Control register when writing to any of the four 16-bit registers. As explained under the ppse bit in Time Sync Control register, the Target Time2 register can also be used to generate a pulse per second output on the pps_sig pin.

9.2.8 External Event 1 Snapshot Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt1_Lo_Lo	R	0x24		Evnt1Snap[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt1_Lo_Hi	R	0x26		Evnt1Snap[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt1_Hi_Lo	R	0x28		Evnt1Snap[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt1_Hi_Hi	R	0x2A		Evnt1Snap[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The External Event 1 Snapshot register consists of four 16-bit registers. A rising edge on the input signal event_1_sig , triggers a snapshot of the System Time into Evnt1_XX_XX registers and the evs1 bit in Time Sync Event register is set. Polling of the Time Sync Event register for evs1 can be used to determine when this register is ready for a read. Reads of the four 16-bit registers can be performed in any order. The evs1 bit in the Time Sync Event register must be reset by writing a '1' to it in order to snapshot the system time at the next rising edge of event_1_sig .

9.2.9 External Event 2 Snapshot Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt2_Lo_Lo	R	0x2C		Evnt2Snap[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt2_Lo_Hi	R	0x2E		Evnt2Snap[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt2_Hi_Lo	R	0x30		Evnt2Snap[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Evnt2_Hi_Hi	R	0x32		Evnt2Snap[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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The External Event 2 Snapshot register consists of four 16-bit registers. A rising edge on the input signal event_2_sig , triggers a snapshot of the System Time into Evnt2_XX_XX registers and the evs2 bit in Time Sync Event register is set. Polling of the Time Sync Event register for evs2 can be used to determine when this register is ready for a read. Reads of the four 16-bit registers can be performed in any order. The evs2 bit in the Time Sync Event register must be reset by writing a '1' to it in order to snapshot the system time at the next rising edge of event_2_sig .

9.2.10 Transmit Snapshot Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxTS_Lo_Lo	R	0x34		TransmitSnap[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxTS_Lo_Hi	R	0x36		TransmitSnap[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxTS_Hi_Lo	R	0x38		TransmitSnap[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxTS_Hi_Hi	R	0x3A		TransmitSnap[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Transmit Snapshot register consists of four 16-bit registers. A Sync frame in master mode or Delay_Req frame in slave mode triggers a snapshot of the System Time into Xmit_XX_XX registers and the txs bit in Time Sync Event register is set. Reads of the four 16-bit registers can be performed in any order. The txs bit in the Time Sync Event register must be reset by writing a '1' to it in order to snapshot system time at the next Sync or Delay_Req frame.

9.2.11 Receive Snapshot Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxTS_Lo_Lo	R	0x3C		ReceiveSnap[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxTS_Lo_Hi	R	0x3E		ReceiveSnap[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxTS_Hi_Lo	R	0x40		ReceiveSnap[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxTS_Hi_Hi	R	0x42		ReceiveSnap[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Receive Snapshot register consists of four 16-bit registers. A Sync frame in slave mode or Delay_Req frame in master mode triggers a snapshot of the System Time into the Recv_XX_XX registers and the rxs bit in Time Sync Event register is set. Reads of four 16-bit registers can be performed in any order. Up to 16 snapshots will be stored in the FIFO if firmware is slow to process them. If the FIFO is full, subsequent Sync/Delay_Req frames will not cause the snapshot/source ID/sequence ID to be stored. The rxs bit in the Time Sync Event register must be reset by writing a '1' to it after reading a snapshot. If the bit doesn't reset, it indicates that additional snapshots are present. Firmware should repeatedly read and store all entries from the FIFO until this bit is reset.

9.2.12 Receive Source ID Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxID_Lo_Lo	R	0x44		SourceID[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxID_Lo_Hi	R	0x46		SourceID[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxID_Hi_Lo	R	0x48		SourceID[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxID_Hi_Hi	R	0x4A		SourceID[63:48]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Receive Source ID register consists of four 16-bit registers. The reception of a Sync frame in slave mode or Delay_Req frame in master mode triggers the capture of the source ID field in the received frame into the RxID_XX_XX registers. Reads of the four 16-bit registers can be performed in any order. See the Receive Snapshot register for additional description.

9.2.13 Receive Sequence ID Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxSeqID	R	0x4C		SequenceID[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The reception of a Sync frame in slave mode or Delay_Req frame in master mode triggers the capture of the sequence ID field in the received frame into the RxSeqID register. See the Receive Snapshot register for additional description.

9.2.14 PTP Sub-domain Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Subdomain	R/W	0x4E										Subdomain[7:0]							
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The PTP Sub-domain register is used to specify the sub-domain field of PTP event frames. Only the PTP event frames matching the value in this register will be time stamped. By default, this register will be 0, matching only the default sub-domain event frames.

9.2.15 Switch Control Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW_Control	R/W	0x50		ulfe	dms	dbs	dfc	dbg	p2ly	p1ly	p2lo	p1lo	p2s	p1s	p2h	p1h	p2r	p1r	rst
Power-up Defaults				1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0

rst **Chip Reset**. When a ‘1’ is written to this bit, all logic is returned to the same default state as when a power-on reset occurs. This bit is self-clearing.

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p1r **Port 1 Reset**. When this bit is set, port 1 is held in reset and no packets will be transmitted or received on port 1. This bit must be set for a minimum of 500 nanosecs for a proper reset.

p2r **Port 2 Reset**. When this bit is set, port 2 is held in reset and no packets will be transmitted or received on port 2. This bit must be set for a minimum of 500 nanosecs for a proper reset.

p1h **Port 1 Half Duplex**. When this bit is set, port 1 is in half duplex mode. When this bit is reset, port 1 is in full duplex mode. This bit should be set to the same duplex mode as negotiated/forced in the PHY. This bit should be changed only when p1r is set i.e. port 1 is held in reset.

p2h **Port 2 Half Duplex**. When this bit is set, port 2 is in half duplex mode. When this bit is reset, port 2 is in full duplex mode. This bit should be set to the same duplex mode as negotiated/forced in the PHY. This bit should be changed only when p2r is set i.e. port 2 is held in reset.

p1s **Port 1 Speed 10Mbps**. When this bit is set, the port 1 is operating at 10Mbps speed. When this bit is reset, port 1 is operating at 100Mbps speed. This bit should be set to the same speed as negotiated/forced in the PHY. This bit should be changed only when p1r is set i.e. port 1 is held in reset.

p2s **Port 2 Speed 10Mbps**. When this bit is set, the port 2 is operating at 10Mbps speed. When this bit is reset, port 2 is operating at 100Mbps speed. This bit should be set to the same speed as negotiated/forced in the PHY. This bit should be changed only when p2r is set i.e. port 2 is held in reset.

p1lo **Port 1 LED On**. When this bit is set, the port 1 LED is turned on. When there is no link activity on port 1 the LED will be solid indicating the link is up. When there is link activity on port 1 the LED will blink at a rate of 10Hz. Firmware can place port 1 in reset and set this bit to test the LED.

p2lo **Port 2 LED On**. When this bit is set, the port 2 LED is turned on. When there is no link activity on port 2, the LED will be solid indicating the link is up. When there is link activity on port 2 the LED will blink at a rate of 10Hz. Firmware can place port 2 in reset and set this bit to test the LED.

p1ly **Port 1 LED Yellow**. When this bit is set, the port 1 LED will be driven to the yellow color. If this bit is reset, the port 1 LED will be driven to the green color. Firmware can place port 1 in reset and set/reset this bit to test yellow/green color LEDs.

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p2ly **Port 2 LED Yellow**. When this bit is set, the port 2 LED will be driven to the yellow color. If this bit is reset, the port 2 LED will be driven to the green color. Firmware can place port 2 in reset and set/reset this bit to test yellow/green color LEDs.

dbg **Internal Port Debug Mode**. When this bit is set, the internal port connected to the host CPU will operate in promiscuous mode and will forward all traffic received on ports 1 and 2 to host CPU. When the combined traffic received on ports 1 and 2 exceed the bandwidth capacity of 100Mbps of the internal port, frames will be dropped on the internal port. Hence this setting must be used only for debug purposes and not during normal operation.

dfc **Disable Flow Control**. When this bit is set, flow control is disabled on all ports in both full and half duplex modes.

dbs **Disable Broadcast Storm Control**. When this bit is set, broadcast storm control will be disabled.

dms **Disable Multicast Storm Control**. When this bit is set multicast storm control will be disabled.

ulfe **Unicast MAC Address Learning and Filtering Enable**. When this bit is set, dynamic unicast MAC address learning and filtering is enabled. To flush unicast MAC address learning table reset this bit and then set it again.

9.2.16 Switch IRQ Event Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW_Event	R/W	0x52		lst2	lst1				pit	p2l	p1l	bto2	bto1	brx2	brx1	rbs2	rbs1	lirq2	lirq1
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

All interrupt requests from the Switch IRQ Event register will be delivered to the host CPU through the *sw_event_irq_n* signal.

lirq1 **Port 1 Link Status Change IRQ**. When a change of status occurs on the lst1 bit, then the lirq1 will be set. When the l1m bit in the Switch Mask register is also set, then an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

lirq2 **Port 2 Link Status Change IRQ**. When a change of status occurs on the lst2 bit, then the lirq2 will be set. When the l2m bit in the Switch Mask register is

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also set, then an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

rbs1 **Port 1 Ring Beacon State Change IRQ**. When a ring beacon is received through port 1 and a change of State field in the frame is detected when compared to the previous beacon, this bit is set. When the rbm1 bit in the Switch Mask register is also set, an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

rbs2 **Port 2 Ring Beacon State Change IRQ**. When a ring beacon is received through port 2 and a change of State field in frame is detected when compared to the previous beacon, this bit is set. When the rbm2 bit in the Switch Mask register is also set, an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

brx1 **Port 1 Beacon Received IRQ**. When a ring beacon is received through port 1, this bit is set. When the brm1 bit in the Switch Mask register is also set, an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

brx2 **Port 2 Beacon Received IRQ**. When a ring beacon is received through port 2, this bit is set. When the brm2 bit in the Switch Mask register is also set, an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

bto1 **Port 1 Beacon Timeout IRQ**. When a ring beacon is not received through port 1 within the beacon timeout period, this bit is set. When the btm1 bit in the Switch Mask register is also set, an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

bto2 **Port 2 Beacon Timeout IRQ**. When a ring beacon is not received through port 2 within the beacon timeout period, this bit is set. When the btm2 bit in the Switch Mask register is also set, an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

p1l **Port 1 Loop IRQ**. When a frame with the same source address field as the host CPU MAC address is received on port 1, this bit is set. When the p1lm bit in the Switch Control register is also set, an interrupt is delivered to the host CPU. This bit indicates a network misconnection resulting in a loop when not in ring redundancy mode. This should be flagged to the user, indicating a network fault condition. This bit can be cleared by writing a '1' to it.

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p2l **Port 2 Loop IRQ**. When a frame with the same source address field as the host CPU MAC address is received on port 2, this bit is set. When the p2lm bit in the Switch Control register is also set, an interrupt is delivered to the host CPU. This bit indicates a network misconnection resulting in a loop when not in ring redundancy mode. This should be flagged to the user, indicating a network fault condition. This bit can be cleared by writing a '1' to it.

pit **Periodic Interval Timer IRQ**. When the periodic interval timer expires (i.e. counts down to zero) this bit is set. When the pitm bit in the Switch Mask register is also set, an interrupt is delivered to the host CPU. This bit can be reset by writing a '1' to it.

lst1 **Port 1 Link Status**. This bit reflects the port 1 link status from the P1_LNKSTS input signal. A '1' indicates a valid link has been established (i.e. link pass status) and a '0' indicates link fail status. This is a read only bit, writes will be ignored.

lst2 **Port 2 Link Status**. This bit reflects the port 2 link status from the P2_LNKSTS input signal. A '1' indicates a valid link has been established (i.e. link pass status) and a '0' indicates link fail status. This is a read only bit, writes will be ignored.

9.2.17 Switch IRQ Mask Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW_Mask	R/W	0x54							pitm	p2lm	p1lm	btm2	btm1	brm2	brm1	rbm2	rbm1	l2m	l1m
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

l1m **Port 1 Link Status Change IRQ Mask**. When this bit is set and the lirq1 bit in the Switch Event register is also set, then an interrupt is delivered to the host CPU.

l2m **Port 2 Link Status Change IRQ Mask**. When this bit is set and the lirq2 bit in the Switch Event register is also set, then an interrupt is delivered to the host CPU.

rbm1 **Port 1 Ring Beacon State Change IRQ Mask**. When this bit is set and the rbs1 bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

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rbm2 **Port 2 Ring Beacon State Change IRQ Mask**. When this bit is set and the rbs2 bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

brm1 **Port 1 Beacon Received IRQ Mask**. When this bit is set and the brx1 bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

brm2 **Port 2 Beacon Received IRQ Mask**. When this bit is set and the brx2 bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

btm1 **Port 1 Beacon Timeout IRQ Mask**. When this bit is set and the bto1 bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

btm2 **Port 2 Beacon Timeout IRQ Mask**. When this bit is set and the bto2 bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

p1lm **Port 1 Loop IRQ Mask**. When this bit is set and the p1l bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

p2lm **Port 2 Loop IRQ Mask**. When this bit is set and the p2l bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

pitm **Periodic Interval Timer IRQ Mask**. When this bit is set and the pit bit in the Switch Event register is also set, an interrupt is delivered to the host CPU.

9.2.18 Port 1 Seed Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Prt1Seed	R/W	0x56								p1seed									
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

p1seed **Port 1 Seed**. When the port 1 is in half duplex mode, this field can be used to load a 10-bit seed value into the linear feedback shift register that is used for the truncated binary exponential back off algorithm.

9.2.19 Port 2 Seed Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Prt2Seed	R/W	0x58								p2seed									
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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p2seed **Port 2 Seed**. When the port 2 is in half duplex mode, this field can be used to load a 10-bit seed value into the linear feedback shift register that is used for the truncated binary exponential back off algorithm.

9.2.20 Host CPU MAC Address Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_Lo_Lo	R/W	0x5A		MACAddress[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_Lo_Hi	R/W	0x5C		MACAddress[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_Hi_Lo	R/W	0x5E		MACAddress[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Host CPU MAC Address register consists of three 16-bit registers. This register should be set to the same unicast MAC address as the host CPU MAC address. For example to load the MAC address 00-11-22-33-44-55, 0x0011 should be written to the MAC_Hi_Lo, 0x2233 should be written to the MAC_Lo_Hi, and 0x4455 should be written to the MAC_Lo_Lo. The content of this register is used to perform filtering inside the switch. Unicast frames cannot be received on the host until this register is set. The switch performs limited filtering of unicast frames. When a unicast frame is received on any port with a destination address equal to the host MAC address, then that frame is delivered to the host and is not forwarded to the other port. If a unicast frame is received on any port with a destination address not equal to the host MAC address, then it is only forwarded to the other port, but not to the host. Reads and writes of the three 16-bit registers can be performed in any order.

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9.2.21 Multicast Hash Filter Index and Value Registers

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCHFI	R/W	0x60											MulticastHashIndex[6:0]						
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCHFV	R/W	0x62		MulticastHashValue[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Multicast Hash Filter consists of one hundred and twenty eight (128) 16-bit registers. These 128 registers comprise a 2048 bin hash filter table, with bit 0 of register 0 corresponding to bin 0, and bit 15 of register 127 corresponding to bin 2047. In order to access a filter register, the register number should first be written to the Multicast Hash Filter Index register. The register value can then be read from/written to through the Multicast Hash Filter Value register. When a multicast frame is received on an external port, the CRC is computed on the received multicast address, and the bottom 11 bits of the CRC are used to select the bin in the multicast hash filter table. If the selected bin is set, then the frame will be delivered to the host CPU. The algorithm used to compute the CRC is the same as the Ethernet CRC. One version of the CRC code is enclosed for reference. A table driven version of the Ethernet CRC code can also be used for speed. For example, to receive multicast address 01-00-5E-00-01-81 (CRC=0xD2E88860), register 6, bit 0 must be set. Note that the filter table need not be set for receiving multicast ring frames.

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```
//-------------------------------------------------------------------
const unsigned  Poly = 0xedb88320; // bit reverse of 0x04c11db7
//-------------------------------------------------------------------
unsigned  ComputeCrc32 (unsigned char  *buf, int  len)
{
        unsigned  crc = 0xffffffff;
        while  (--len >= 0)
        {
                unsigned char  data = *buf++;
                for  (int  i = 0; i < 8; i++)
                {
                        if  ((crc ^ data) & 1)
                        {
                                crc >>= 1;
                                crc ^= Poly;
                        }
                        else  crc >>= 1;
                        data >>= 1;
                }
        }
        return  (crc ^ 0xffffffff);
}
//-------------------------------------------------------------------
unsigned  GetMCHashBin (unsigned char  mcadrs[6])
{
        unsigned  crc = ComputeCrc32 ((unsigned char  *)mcadrs, 6);
        return  (crc & 0x7ff);
}
//-------------------------------------------------------------------
```

9.2.22 Free Running Timer Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FreeTmr_Lo	R	0x64		FreeTimer[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FreeTmr_Hi	R	0x66		FreeTimer[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Free Running Timer register consists of two 16-bit registers. It is a 32-bit free running up counter that counts at 100MHz and is used for transparent clock timestamps, delay measurements, and redundancy timestamps. It can be used to compare how recent a

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timestamp is using 32-bit unsigned arithmetic. At 100MHz the counter will reach the same value from the starting point in about 42 seconds, and so comparisons are not valid beyond that. When performing reads, FreeTmr_Lo should be read first, which will cause the higher 16 bits of the internal Free Timer register to be latched. When FreeTmr_Hi is read later, the latched value will be returned.

9.2.23 Periodic Interval Timer Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PITTmo_Lo	R/W	0x68		PITTimeout[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PITTmo_Hi	R/W	0x6A		PITTimeout[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Periodic Interval Timer register consists of two 16-bit registers. It is a 32-bit down counter that counts at 50MHz. When the PIT timer is enabled through the pite bit in the Redundancy Control register, the value from this register is loaded into the timer and countdown begins. When the timer reaches zero the pit bit in the Switch Event register is set, and the timer is loaded with value from this register again for the next count down. To prevent spurious interrupts, this register should be changed only when the pite bit is reset in the Redundancy Control register. The periodic interval timer can be used to provide an interrupt to generate ring beacons.

9.2.24 Redundancy Control Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rdndnc_Control	R/W	0x6C			raf	drm	cns	pite	p2bte	p1bte	p2br	p1br	p2tb	p2rb	p1tb	p1rb	rspr	dlre	resv
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

resv **Reserved**, must be reset (0)

dlre **Device Level Ring Protocol Enable**. When this bit is set, fido2100 will support DLR protocol redundancy. If it is reset, fido2100 will not support ring redundancy.

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rspr **Ring Supervisor Enable**. When this bit is set, fido2100 will support Ring protocol redundancy as a ring supervisor. If it is reset, fido2100 will support Ring protocol redundancy as a nonsupervisory device. Depending on the setting of this bit, some logic will be enabled, some disabled and some function differently. Details are described under appropriate sections.

p1rb **Port 1 Receive Blocked**. When this bit is set all frames received on port 1 will be dropped with the exception of following special frames. Ring beacon frames will be forwarded to host CPU if p1br bit is set. Ring beacon frames with source MAC address different from Ring Supervisor MAC ID register will always be forwarded to host CPU. Ring Neighbor Check/Sign On (multicast) frames will be forwarded to host CPU. Ring Link/Neighbor Status frames or beacon Failure Notify frames with destination MAC address same as host CPU MAC address will be forwarded to host CPU. Ring beacon frames will be forwarded to port 2 if rspr bit is not set.

p1tb **Port 1 Transmit Blocked**. When this bit is set no frames will be transmitted on port 1 with the exception of following special frames. Ring beacon frames from host CPU will be transmitted if rspr bit is set (i.e. ring beacon will be transmitted on both ports). Ring Neighbor Check/Sign On (multicast) frames from host CPU will be transmitted if source port in frame matches port 1. Ring beacon frames from port 2 will be transmitted if rspr bit is not set.

p2rb **Port 2 Receive Blocked**. When this bit is set all frames received on port 2 will be dropped with the exception of following special frames. Ring beacon frames will be forwarded to host CPU if p2br bit is set. Ring beacon frames with source MAC address different from Ring Supervisor MAC ID register will always be forwarded to host CPU. Ring Neighbor Check/Sign On (multicast) frames will be forwarded to host CPU. Ring Link/Neighbor Status frames or beacon Failure Notify frames with destination MAC address same as host CPU MAC address will be forwarded to host CPU. Ring beacon frames will be forwarded to port 1 if rspr bit is not set.

p2tb **Port 2 Transmit Blocked**. When this bit is set no frames will be transmitted on port 2 with the exception of following special frames. Ring beacon frames from host CPU will be transmitted if rspr bit is set (i.e. ring beacon will be transmitted on both ports). Ring Neighbor Check/Sign On (multicast) frames from host CPU will be transmitted if source port in frame matches port 2. Ring beacon frames from port 1 will be transmitted if rspr bit is not set.

p1br **Port 1 Beacon Receive**. When this bit is set, Ring beacon frames received on port 1 will be forwarded to host CPU. If this bit is reset, Ring beacons received

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on port 1 will be dropped with following exception. Ring beacon frames with source MAC address different from Ring Supervisor MAC ID register will always be forwarded to host CPU.

p2br **Port 2 Beacon Receive**. When this bit is set, Ring beacon frames received on port 2 will be forwarded to host CPU. If this bit is reset, Ring beacons received on port 2 will be dropped with following exception. Ring beacon frames with source MAC address different from Ring Supervisor MAC ID register will always be forwarded to host CPU.

p1bte **Port 1 Beacon Timeout Enable**. When this bit is set, port 1 beacon timeout timer is enabled. See Beacon Timeout register for details.

p2bte **Port 2 Beacon Timeout Enable**. When this bit is set, port 2 beacon timeout timer is enabled. See Beacon Timeout register for details.

pite **Periodic Interval Timer Enable**. When this bit is set, periodic interval timer is enabled. See Periodic Interval Timer register for details.

cns **Clear Neighbor Check Request/Sign On and Link/Neighbor Status Receive Source ID Registers**. When this bit is set, Neighbor Check Request/Sign On and Link/Neighbor Status Receive Source ID registers for both port 1 and port 2 will be cleared. This bit is self-clearing.

drm **Drop Reserved MAC addresses**. When this bit is set, IEEE 802.1D reserved MAC address 01-80-C2-00- 00-00 and Cisco PVST+ MAC address 01-00-0C-CC-CC-CD will not be forwarded from any port to other ports.

raf **Receive Announce Frames**. When this bit is set, ring Announce frames will be forwarded to host CPU.

9.2.25 Ring Beacon State Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rng_BcnState	R	0x6E		RingBeaconState2[7:0]								RingBeaconState1[7:0]							
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Ring Beacon State register contains the State Flags field captured from the last beacon frame with the Ring Supervisor MAC ID register source address through ports 1 and 2. RingBeaconState1 contains the State field captured from the last beacon frame through port 1 and RingBeaconState2 contains the State field captured from the last

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beacon frame through port 2. A change of state in RingBeaconState1 causes the rbs1 IRQ in the Switch Event register and a change of state in RingBeaconState2 causes the rbs2 IRQ in the Switch Event register.

9.2.26 Beacon Timeout Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BcnTmo_Lo	R/W	0x70		BeaconTimeout[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BcnTmo_Hi	R/W	0x72		BeaconTimeout[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Beacon Timeout register consists of two 16-bit registers. The timeout value is used by both the port 1 beacon timeout timer and the port 2 beacon timeout timer. The beacon timeout timers are 32-bit down counters that count at 50MHz. When the port 1 (or port 2) beacon timeout timer is enabled through the p1bte (or p2bte) bit in the Redundancy Control register, the value from this register is loaded into respective timer and countdown begins. When a Ring beacon is received on port 1 (or port 2) with the Ring Supervisor MAC ID register source address, without a CRC error, the respective port's beacon timer is reloaded with the beacon timeout value and the countdown is started again. If the timer reaches zero the bto1 (or bto2) bit in the Switch Event register is set and the timer is loaded with the value from this register again for next count down. To prevent spurious interrupts, this register should be changed only when the p1bte and p2bte bits are reset in the Redundancy Control register.

9.2.27 Port 1 Beacon Receive Timestamp Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1BcnTS_Lo	R	0x74		BeaconTimestamp1[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1BcnTS_Hi	R	0x76		BeaconTimestamp1[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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The Port 1 Beacon Receive Timestamp register is comprised of two 16- bit registers. It contains a snapshot of the Free Running Timer when last Ring beacon was received on Port 1 with the Ring Supervisor MAC ID register source address. The two registers may be read in any order. However, since the registers may be updated between two reads when a new beacon is received, care should be taken to read the registers multiple times and only consider it as valid when two successive reads produce the same result.

9.2.28 Port 2 Beacon Receive Timestamp Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2BcnTS_Lo	R	0x78		BeaconTimestamp2[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2BcnTS_Hi	R	0x7A		BeaconTimestamp2[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Port 2 Beacon Receive Timestamp register is comprised of two 16- bit registers. It contains a snapshot of the Free Running Timer when the last ring beacon was received on Port 2 with the Ring Supervisor MAC ID register source address. The two registers may be read in any order. However, since the registers may be updated between two reads when a new beacon is received, care should be taken to read the registers multiple times and only consider it as valid when two successive reads produce the same result.

9.2.29 Port 1 Neighbor Check Request/Sign On Receive Source ID Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1NChkSId_Lo_Lo	R	0x7C		Port1_Neighbor_Check_Req_Recv_SrcID[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1NChkSId_Lo_Hi	R	0x7E		Port1_Neighbor_Check_Req_Recv_SrcID[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1NChkSId_Hi_Lo	R	0x80		Port1_Neighbor_Check_Req_Recv_SrcID[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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The Port 1 Neighbor Check Request/Sign On Receive Source ID register is comprised of three 16- bit registers. It contains the source MAC address of last Neighbor Check Request/Sign On (multicast) frame that was received on port 1. Reads may be performed in any order.

9.2.30 Port 2 Neighbor Check Request/Sign On Receive Source ID Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2NChkSId_Lo_Lo	R	0x82		Port2_Neighbor_Check_Req_Recv_SrcID[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2NChkSId_Lo_Hi	R	0x84		Port2_Neighbor_Check_Req_Recv_SrcID[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2NChkSId_Hi_Lo	R	0x86		Port2_Neighbor_Check_Req_Recv_SrcID[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Port 2 Neighbor Check Request/Sign On Receive Source ID register is comprised of three 16- bit registers. It contains the source MAC address of last Neighbor Check Request/Sign On (multicast) frame that was received on port 2. Reads may be performed in any order.

9.2.31 Port 1 Link/Neighbor Status Receive Source ID Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1NStsSId_Lo_Lo	R	0x88		Port1_Neighbor_Status_Recv_SrcID[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1NStsSId_Lo_Hi	R	0x8A		Port1_Neighbor_Status_Recv_SrcID[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1NStsSId_Hi_Lo	R	0x8C		Port1_Neighbor_Status_Recv_SrcID[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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The Port 1 Link/Neighbor Status Receive Source ID register is comprised of three 16- bit registers. It contains the source MAC address of the last Link/Neighbor Status frame that was received on port 1. Reads may be performed in any order.

9.2.32 Port 2 Link/Neighbor Status Receive Source ID Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2NStsSId_Lo_Lo	R	0x8E		Port2_Neighbor_Status_Recv_SrcID[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2NStsSId_Lo_Hi	R	0x90		Port2_Neighbor_Status_Recv_SrcID[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2NStsSId_Hi_Lo	R	0x92		Port2_Neighbor_Status_Recv_SrcID[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Port 2 Link/Neighbor Status Receive Source ID register is comprised of three 16- bit registers. It contains the source MAC address of the last Link/Neighbor Status frame that was received on port 2. Reads may be performed in any order.

9.2.33 Ring Supervisor MAC ID Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RngSprvsrId_Lo_Lo	R	0x94		Ring_Supervisor_MacId[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RngSprvsrId_Lo_Hi	R	0x96		Ring_Supervisor_MacId[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RngSprvsrId_Hi_Lo	R	0x98		Ring_Supervisor_MacId[47:32]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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The Ring Supervisor MAC ID register is comprised of three 16- bit registers. It contains the source MAC address of active ring supervisor. This register must be set to the proper value in both ring supervisor and non-supervisor modes of operation, for the ring logic to function correctly. For example to load MAC address 00-11-22-33-44-55, 0x0011 should be written to RngSprvsrId_Hi_Lo, 0x2233 should be written to RngSprvsrId _Lo_Hi, and 0x4455 should be written to RngSprvsrId _Lo_Lo. Reads and writes may be performed in any order.

9.2.34 Interface and Media Counters Registers

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxGrpFrmCnt	R	0x9C		Port1_Group_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxGrpFrmCnt	R	0x9E		Port2_Group_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxUniFrmCnt	R	0xA0		Port1_Unicast_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxUniFrmCnt	R	0xA2		Port1_Unicast_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxBytCnt_Lo	R	0xA4		Port1_Recv_Byte_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxBytCnt_Hi	R	0xA6		Port1_Recv_Byte_Count[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxBytCnt_Lo	R	0xA8		Port2_Recv_Byte_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxBytCnt_Hi	R	0xAA		Port2_Recv_Byte_Count[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxLrgFrmCnt	R	0xAC		Port1_Large_Error_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxLrgFrmCnt	R	0xAE		Port2_Large_Error_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxAlnFrmCnt	R	0xB0		Port1_Align_Error_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxAlnFrmCnt	R	0xB2		Port2_Align_Error_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxFcsFrmCnt	R	0xB4		Port1_FCS_Error_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxFcsFrmCnt	R	0xB6		Port2_FCS_Error_Frame_Recv_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1RxErrFrmCnt	R	0xB8		Port1_Recv_Error_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2RxErrFrmCnt	R	0xBA		Port2_Recv_Error_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxGrpFrmCnt	R	0xBC		Port1_Group_Frame_Xmit_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxGrpFrmCnt	R	0xBE		Port2_Group_Frame_Xmit_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxUniFrmCnt	R	0xC0		Port1_Unicast_Frame_Xmit_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxUniFrmCnt	R	0xC2		Port2_Unicast_Frame_Xmit_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxBytCnt_Lo	R	0xC4		Port1_Xmit_Byte_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxBytCnt_Hi	R	0xC6		Port1_Xmit_Byte_Count[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxBytCnt_Lo	R	0xC8		Port2_Xmit_Byte_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxBytCnt_Hi	R	0xCA		Port2_Xmit_Byte_Count[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxSCIFrmCnt	R	0xCC		Port1_Xmit_Single_Collision_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxSClFrmCnt	R	0xCE		Port2_Xmit_Single_Collision_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxMClFrmCnt	R	0xD0		Port1_Xmit_Multiple_Collision_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxMClFrmCnt	R	0xD2		Port2_Xmit_Multiple_Collision_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxXClFrmCnt	R	0xD4		Port1_Xmit_Excessive_Collision_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxXClFrmCnt	R	0xD6		Port2_Xmit_Excessive_Collision_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1TxErrFrmCnt	R	0xD8		Port1_Xmit_Error_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2TxErrFrmCnt	R	0xDA		Port2_Xmit_Error_Frame_Count[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Interface and Media counters registers can be used to implement EtherNet/IP link object. To avoid a rollover issue with these registers, the firmware should scan these registers at least once every 200 milliseconds or on demand, and calculate the increase in counters using unsigned 16-bit arithmetic. The computed increase must be added to firmware maintained 32-bit counters of the EtherNet/IP link object. The counters can be reset by resetting the respective port.

- **P1RxGrpFrmCnt** : This 16-bit counter reflects multicast and broadcast frames received without errors on port 1.

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- **P2RxGrpFrmCnt**: This 16-bit counter reflects multicast and broadcast frames received without errors on port 2.
- **P1RxUniFrmCnt**: This 16-bit counter reflects unicast frames received without errors on port 1.
- **P2RxUniFrmCnt**: This 16-bit counter reflects unicast frames received without errors on port 2.
- **P1RxBytCnt**: This 32-bit counter reflects byte count of unicast, multicast and broadcast frames received without errors on port 1. Since this register may be updated while the reads are under progress, this counter must be read twice. Only when two successive reads produce same result should the value be used.
- **P2RxBytCnt**: This 32-bit counter reflects byte count of unicast, multicast and broadcast frames received without errors on port 2. Since this register may be updated while the reads are under progress, this counter must be read twice. Only when two successive reads produce same result should the value be used.
- **P1RxLrgFrmCnt**: This 16-bit counter reflects frames larger than 1522 bytes including CRC received on port 1. Such frames are not IEEE 802.3 compliant.
- **P2RxLrgFrmCnt**: This 16-bit counter reflects frames larger than 1522 bytes including CRC received on port 2. Such frames are not IEEE 802.3 compliant.
- **P1RxAlnFrmCnt**: This 16-bit counter reflects frames with alignment error i.e. non-integral number of bytes received on port 1.
- **P2RxAlnFrmCnt**: This 16-bit counter reflects frames with alignment error i.e. non-integral number of bytes received on port 2.
- **P1RxFcsFrmCnt**: This 16-bit counter reflects frames with frame check sequence (CRC) error received on port 1.
- **P2RxFcsFrmCnt**: This 16-bit counter reflects frames with frame check sequence (CRC) error received on port 2.
- **P1RxErrFrmCnt**: This 16-bit counter reflects frames with other errors including frames shorter than 64 bytes received on port 1.
- **P2RxErrFrmCnt**: This 16-bit counter reflects frames with other errors including frames shorter than 64 bytes received on port 2.

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- **P1TxGrpFrmCnt**: This 16-bit counter reflects multicast and broadcast frames transmitted without errors on port 1.
- **P2TxGrpFrmCnt**: This 16-bit counter reflects multicast and broadcast frames transmitted without errors on port 2.
- **P1TxUniFrmCnt**: This 16-bit counter reflects unicast frames transmitted without errors on port 1.
- **P2TxUniFrmCnt**: This 16-bit counter reflects unicast frames transmitted without errors on port 2.
- **P1TxBytCnt**: This 32-bit counter reflects byte count of unicast, multicast and broadcast frames transmitted without errors on port 1. Since this register may be updated while the reads are under progress, this counter must be read twice and only when two successive reads produce same result should the value be used.
- **P2TxBytCnt**: This 32 bit counter reflects byte count of unicast, multicast and broadcast frames transmitted without errors on port 2. Since this register may be updated while the reads are under progress, this counter must be read twice and only when two successive reads produce same result should the value be used.
- **P1TxSClFrmCnt**: This 16-bit counter reflects frames transmitted after exactly one collision in half duplex mode on port 1.
- **P2TxSClFrmCnt**: This 16-bit counter reflects frames transmitted after exactly one collision in half duplex mode on port 2.
- **P1TxMClFrmCnt**: This 16-bit counter reflects frames transmitted after more than one collision in half duplex mode on port 1.
- **P2TxMClFrmCnt**: This 16-bit counter reflects frames transmitted after more than one collision in half duplex mode on port 2.
- **P1TxXClFrmCnt**: This 16-bit counter reflects frames dropped after excessive (16) collisions in half duplex mode on port 1.
- **P2TxXClFrmCnt**: This 16-bit counter reflects frames dropped after excessive (16) collisions in half duplex mode on port 2.
- **P1TxErrFrmCnt**: This 16-bit counter reflects frames truncated with error during transmission on port 1.

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- **P2TxErrFrmCnt**: This 16-bit counter reflects frames truncated with error during transmission on port 2.

9.2.35 Beacon Generation Control Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BcnGenCntrl	R/W	0xDC														bgrst	bge2	bge1	bite
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

bite **Beacon Interval Timer Enable**. When this bit is set, beacon interval timer is enabled. It's a periodic timer and when the interval expires, beacon generation is triggered if bge1/bge2 are set and the timer is restarted. In order to immediately trigger a beacon frame on ports, this bit should be reset and set.

bge1 **Beacon Generation Enable for Port 1**. When this bit is set, DLR beacon frame generation is enabled on port 1. Frame sequence ID will be automatically generated.

bge2 **Beacon Generation Enable for Port 2**. When this bit is set, DLR beacon frame generation is enabled on port 2. Frame sequence ID will be automatically generated.

bgrst **Beacon Generation Reset**. When this bit is set, all beacon frame generation logic will be held in reset.

9.2.36 Beacon Interval Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BcnIntrvl_Lo	R/W	0xDE		BeaconInterval[15:0]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BcnIntrvl_Hi	R/W	0xE0		BeaconInterval[31:16]															
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Beacon Interval register consists of two 16-bit registers. It is a 32-bit counter that counts at 50MHz and is used to trigger beacon frame generation on port(s) when it is enabled and expires. See bite bit in Beacon Generation Control register for more details.

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9.2.37 Beacon Frame Data Index and Value Registers

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BcnDataIdx	R/W	0xE2												BeaconDataIndex[5:0]					
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BcnDataVal	R/W	0xE4										BeaconDataValue[7:0]							
Power-up Defaults				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Beacon Frame Data Index and Value registers provide the means to define appropriate contents for the DLR beacon frame. For DLR beacon frames, bytes 0 to 39 must be defined. The sequence Id for beacon frame will be automatically generated and will be inserted at correct position. Note that byte index greater than or equal to 40 should not be defined.

9.2.38 fido2100 Version Register

Mnemonic	type	offset	bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EmbSwtchVer	R	0xE6		MajorVersion[7:0]								MinorVersion[7:0]							
Power-up Defaults				0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	1

The fido2100 Version Register is a read only register that provides major and minor version information.

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10 Revision History

Table 16 Document Revision History

Date	Revision	Description	Page(s)
September 10, 2012	00	First edition released.	NA
October 1, 2012	01	Updated Section 5.1 PLL Supply.	37
December 3, 2012	02	Added Thermal Characteristics and Power Consumption Information.	37, 38
February 12, 2013	03	Corrected cut-through times (changed ns to µs)	19
April 10, 2013	04	Clarified junction temperature parameter name	37

11 For Additional Information

The Innovasic Support Team is continually planning and creating tools for your use. Visit http://www.innovasic.com for up-to-date documentation and software. Our goal is to provide timely, complete, accurate, useful, and easy-to-understand information. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

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