Class-AB Speaker Amplifier Series

2.8 W High Power Monaural Speaker Amplifier for Automotive

BD783xxEFJ-M BD783xxUEFJ-M Series

General Description

BD783xxEFJ-M, BD783xxUEFJ-M Series are Class-AB monaural speaker amplifiers designed for automotive. Class-AB amplifiers have no requirements for care about EMI noise. Adopting power package HTSOP-J8 achieves high output power. Low quiescent current can reduce battery consumption. Shutdown current is also very low (0.1 µA Typ) and pop noise level when switching to shutdown is very small, so this device is suitable for applications in which the mode often changes between “shutdown state” and “active state”.

Features

- AEC-Q100 Qualified*(Note 1)*
- Pop Noise Reduction Function
- Shutdown Function
- Protection Functions
  - Over Current Protection
  - Thermal Shutdown
  - Under Voltage Lock Out (UVLO)
- Power Package with Thermal Pad HTSOP-J8

(Note 1) Grade2

Applications

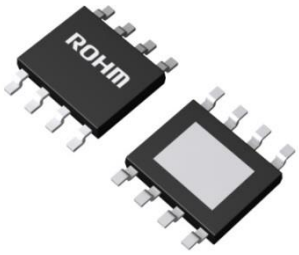
- Automotive Instruments

Key Specifications

- Output Power 1.2 W (Typ)
  (VDD = 5 V, R_L = 8 Ω, THD+N = 1 %)
  Output Power 2.8 W (Typ)
  (VDD = 5 V, R_L = 4 Ω, THD+N = 10 %)
- Quiescent Current 2.5 mA (Typ)
- Shutdown Current 0.1 µA (Typ)
- Total Harmonic Distortion + Noise
  (R_L = 8 Ω, f = 1 kHz) 0.05 % (Typ)*(Note 2)*
- Output Noise Voltage 15 μV_{RMS} (Typ)*(Note 2)*
- Voltage Gain 6.0 dB to 26.0 dB (Typ)
- Operating Temperature Range -40 ºC to +105 ºC

(Note 2) Characteristic of BD78306EFJ-M

Package	**W (Typ) x D (Typ) x H (Max)**
HTSOP-J8	4.90 mm x 6.00 mm x 1.00 mm



HTSOP-J8

Typical Application Circuit

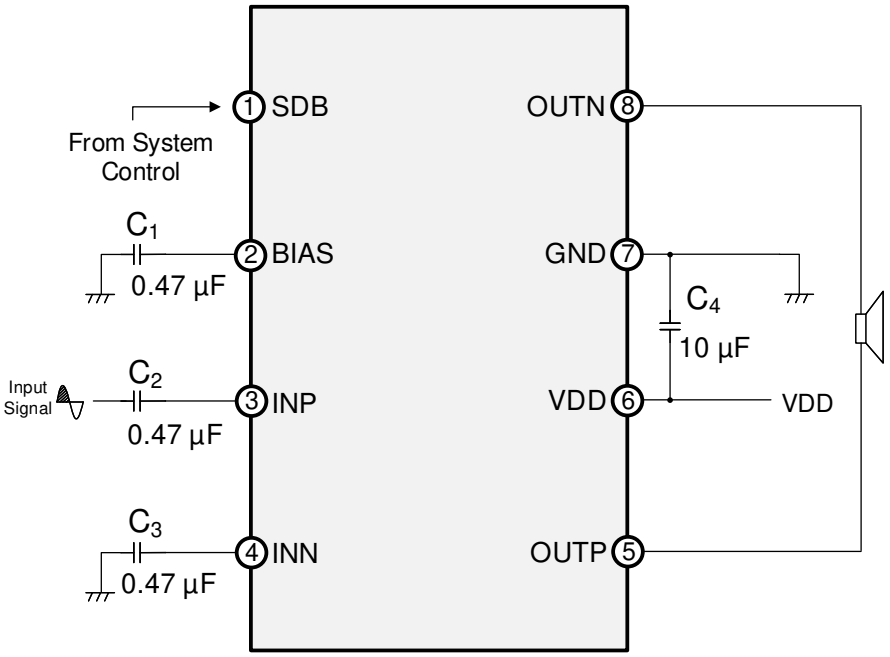
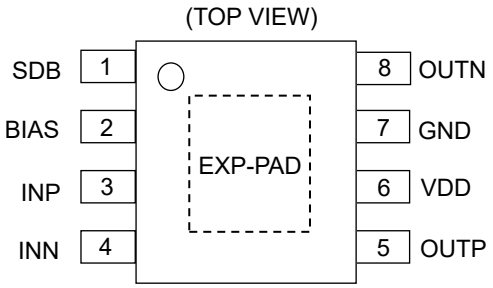


Figure 1

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration



Caution:
VDD and GND pins adjoin each other. In case that these pins are shorted each other, it may make characteristics of power supply device worse, or it may damage power supply device.
Considering this point, select power supply device which has protection functions as over current protection.

Pin Description

Pin No.	Pin Name	Function
1	SDB	Shutdown
2	BIAS	Bias
3	INP	Positive differential input
4	INN	Negative differential input
5	OUTP	Positive output
6	VDD	Power supply
7	GND	Ground
8	OUTN	Negative output
-	EXP-PAD	Connect the EXP-PAD to Ground

Control Pin's Setting

SDB pin	Operating Mode
High	Active
Low	Shutdown

Block Diagram

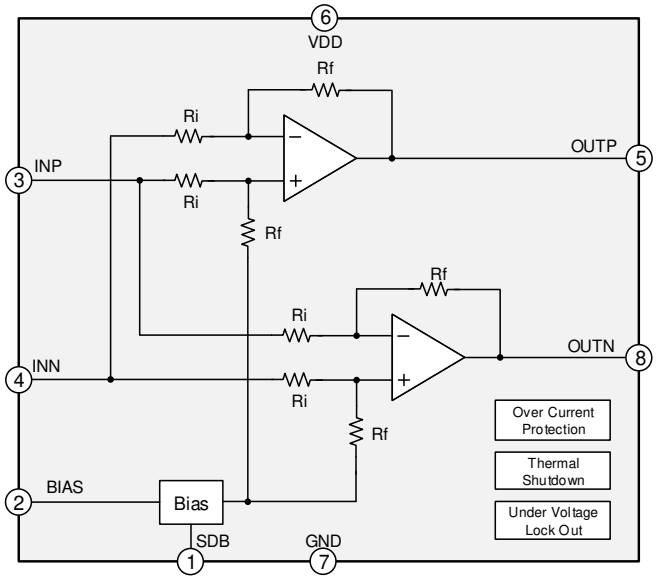


Figure 2

Part Number	Ri[kΩ] (Typ)	Rf[kΩ] (Typ)
BD78306EFJ-M	90	90
BD78306UEFJ-M		
BD78310EFJ-M	70	110
BD78310UEFJ-M		
BD78326EFJ-M	16	164
BD78326UEFJ-M		

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	VDDmax	7.0	V
Input Voltage	Vin	-0.3 to VDD+0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
HTSOP-J8				
Junction to Ambient	θ_{JA}	149.4	39.8	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	11.0	9.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD78326EFJ-M Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Use a thermal design that has sufficient margin in consideration of power dissipation under actual operating conditions. This IC exposes its frame at the backside of package. Note that this part is assumed to be used after providing heat dissipation treatment to improve heat dissipation efficiency. Try to put heat dissipation pattern as wide as possible not only on the board surface but also on the backside.

Under the insufficient heat dissipation and excessive large signal input condition, power dissipation (Pdiss) exceeds maximum power dissipation (Pd) and thermal shutdown function may operate. Thermal design should be considered so that Pdiss is lower than Pd. Reference data of Pdiss is listed on P.7.

(Tjmax : Maximum Junction Temperature = 150 °C, Ta : Operating Ambient Temperature[°C], θja : Package Thermal Resistance[°C/W])

Power dissipation:

$$Pd = (Tjmax - Ta) / \theta ja \quad [W]$$

This IC has thermal shutdown function. Thermal shutdown operates when Tj (junction temperature, which is assumed to be same as chip temperature) rises over about 180 °C (Typ) and be released when Tj fall about 160 °C (Typ) or less.

Thermal shutdown is designed to protect the IC from temperature condition that exceeds Tjmax = 150 °C, not to protect or warrant application set.

Note that device reliability is affected if it is used under temperature thermal shutdown operates.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	VDD	4.0	5.0	5.5	V
Operating Temperature	Topr	-40	+25	+105	°C
Load Resistance	R_L	3.2	8.0	38.4	Ω

Caution: *Operating supply voltage and operating temperature are the ranges in which the IC is available for basic operation. (Basic operation means that the IC operates without emitting unexpected noise or stopping signal.) Characteristics and rating are not warranted in the whole operating supply voltage and operating temperature.*

Electrical Characteristics 1
(Unless otherwise specified Ta = -40 °C to +105 °C, VDD = 5.0 V, f = 1 kHz, R_L = 8 Ω, BTL*(Note 1)*, Active)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
Quiescent Current		I_{CC}	-	2.5	6.0	mA	No load
Shutdown Current		I_{SD}	-	0.1	25.0	μA	Shutdown SDB = Low
Input Impedance		Z_{IN}	Z_{IN} x0.4	Z_{IN}	Z_{IN} x1.6	kΩ	Refer to the table below
Output Offset Voltage		V_{OFS}	-30	0	+30	mV	OUTP-OUTN
Control Pin (SDB)							
Input Voltage	High Level	V_{IH}	2.0	-	VDD	V	
	Low Level	V_{IL}	0	-	0.3	V	
Under Voltage Lock Out (UVLO)							
Threshold Supply Voltage	Detection	V_{UVLO_DET}	-	3.43	3.80	V	
	Release	V_{UVLO_REL}	-	3.58	3.95	V	

(Note 1) "BTL" means the state that R_L is connected between the OUTP pin (pin5) and the OUTN pin (pin8).

Part Number	Z_{IN}[kΩ] (Typ)
BD78306EFJ-M	45
BD78306UEFJ-M	
BD78310EFJ-M	35
BD78310UEFJ-M	
BD78326EFJ-M	8
BD78326UEFJ-M	

Electrical Characteristics 2
(Unless otherwise specified Ta = 25 °C, VDD = 5.0 V, f = 1 kHz, R_L = 8 Ω, BTL, Active)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Rated Output Power*(Note 2)*	P_O	0.9	1.2	1.6	W	THD+N = 1 %, BW = 400 Hz to 30 kHz Continuous output time 60 s
Maximum Output Power	P_{OMAX}	-	1.6	-	W	THD+N = 10 %, BW = 400 Hz to 30 kHz Continuous output time 90 s
Total Harmonic Distortion + Noise	THD+N	-	-	0.5	%	P_O = 1 W BW = 400 Hz to 30 kHz
Voltage Gain*(Note 2)*	G_V	G_V - 1	G_V	G_V + 1	dB	P_O = 0.5 W G_V = 6 dB to 26 dB
Shutdown Attenuation	ATT_{SD}	-	-90	-80	dB	Vin = 0.1 V_{RMS} BW = 400 Hz to 30 kHz
Power Supply Rejection Ratio	PSRR	-	-60	-40	dB	Vripple = 0.2 V_{P-P}, C_1 = 0.47 μF BW = A-Weight
Output Noise Voltage	V_{NO}	-	-	100	μV_{RMS}	C_1 = 0.47 μF BW = A-Weight

(Note 2) The typical performance of device is shown Output Power and Voltage Gain. It largely depends on the board layout, parts, and power supply. The typical values are measured with the device and parts mounting on surface of ROHM's board directly and soldering thermal pad backside of package to top layer cupper pattern of the board.

This IC is applicable to only dynamic speaker, not to other loads.

Typical Performance Curves

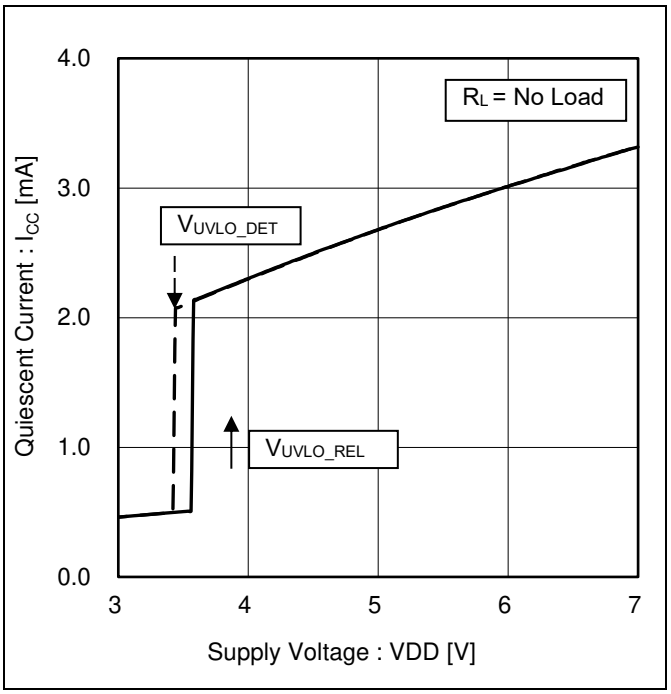


Figure 3. Quiescent Current vs Supply Voltage

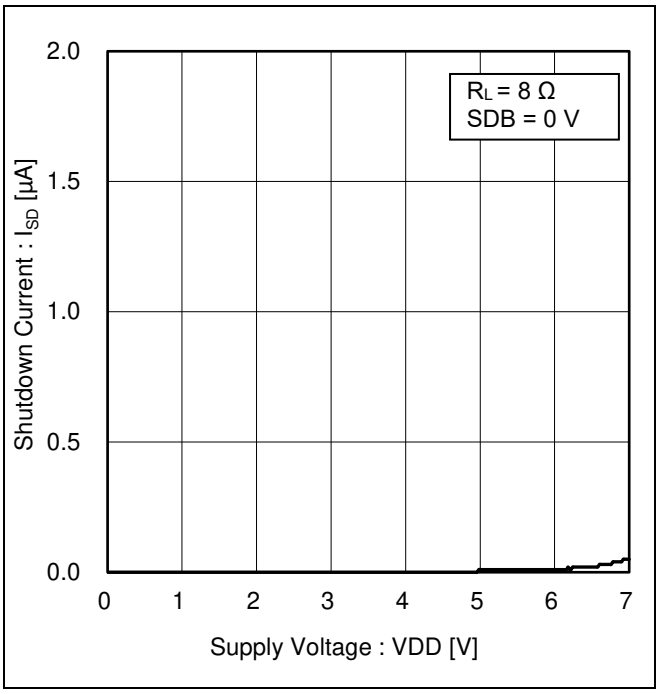


Figure 4. Shutdown Current vs Supply Voltage

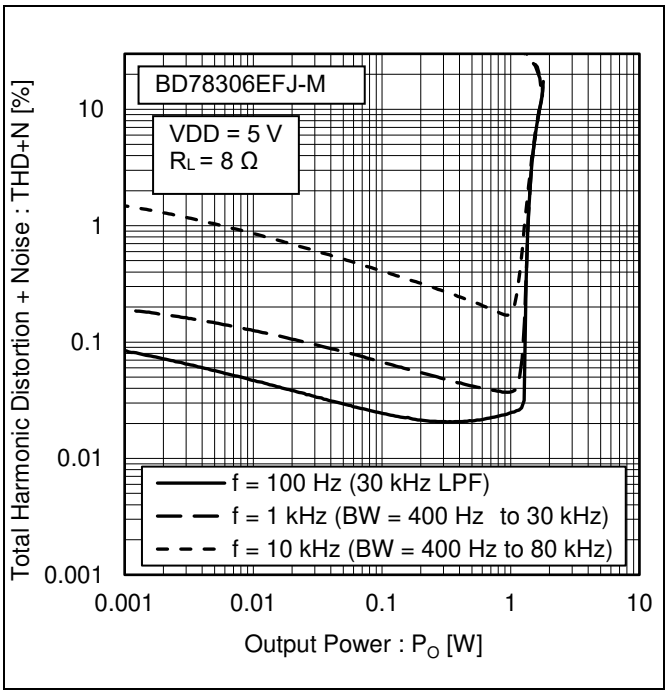


Figure 5. Total Harmonic Distortion + Noise vs Output Power

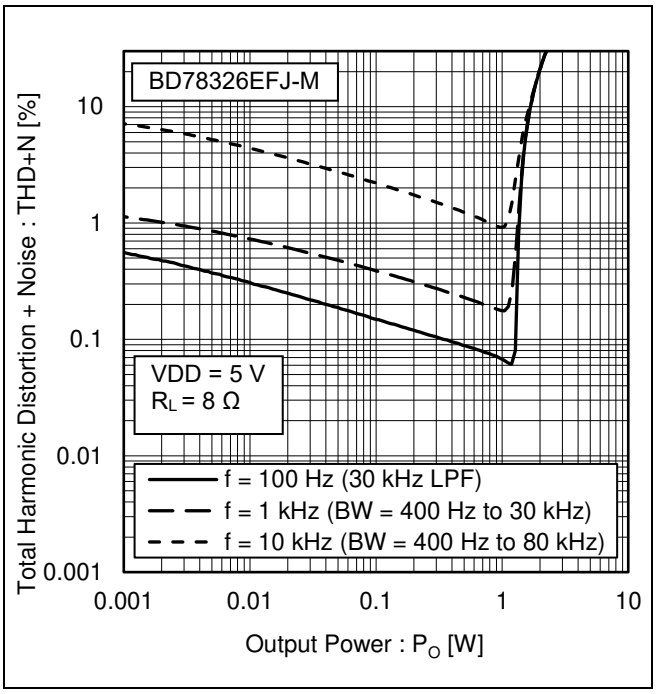


Figure 6. Total Harmonic Distortion + Noise vs Output Power

Typical Performance Curves – continued

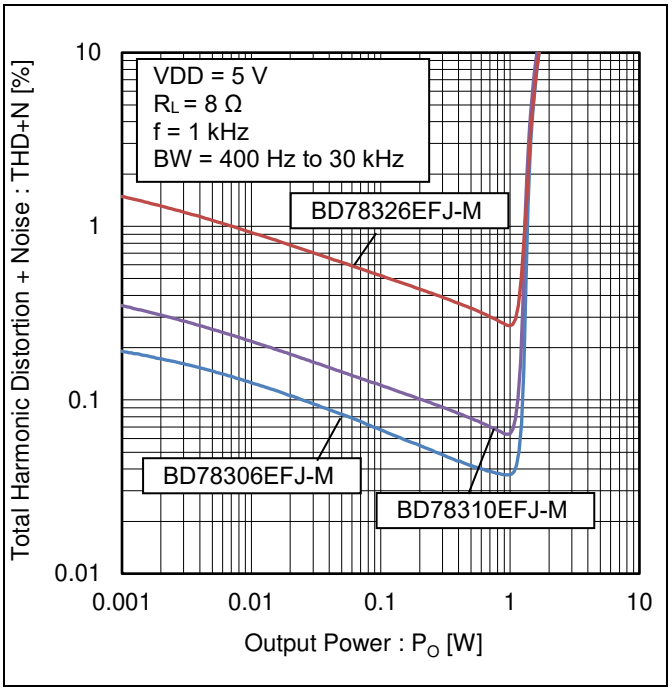


Figure 7. Total Harmonic Distortion + Noise vs Output Power

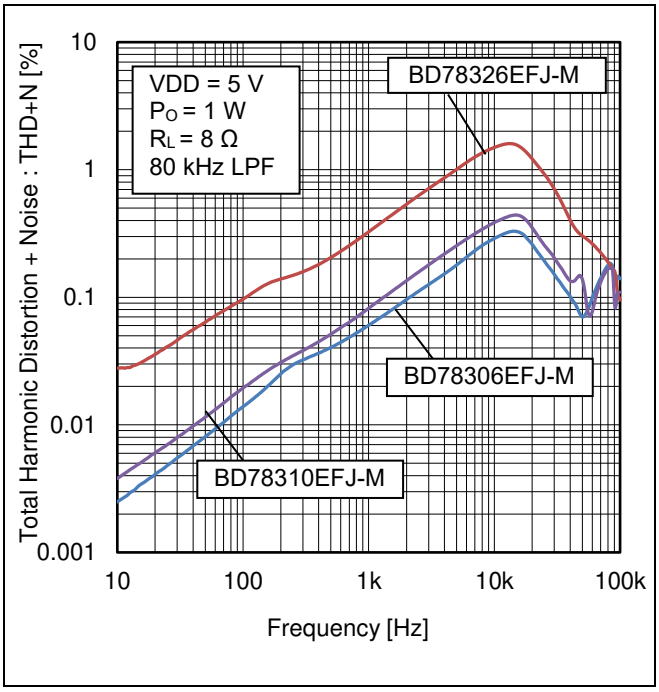


Figure 8. Total Harmonic Distortion + Noise vs Frequency

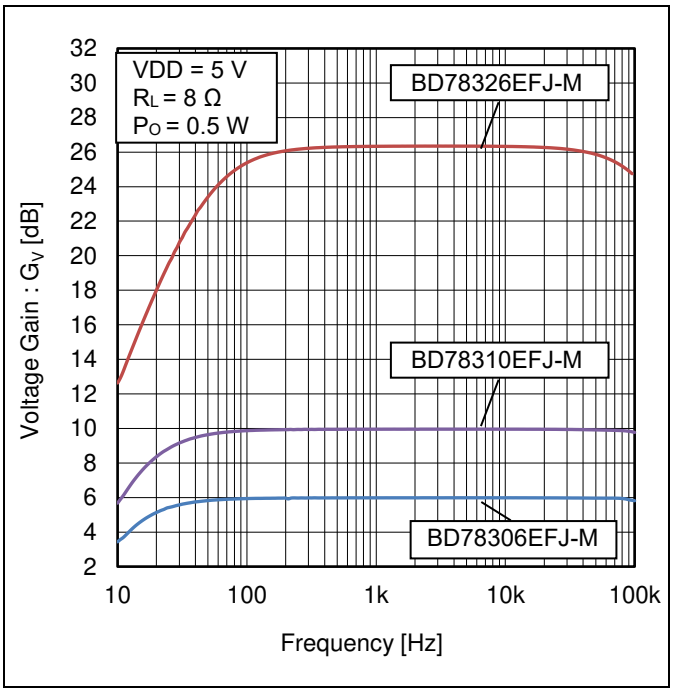


Figure 9. Voltage Gain vs Frequency

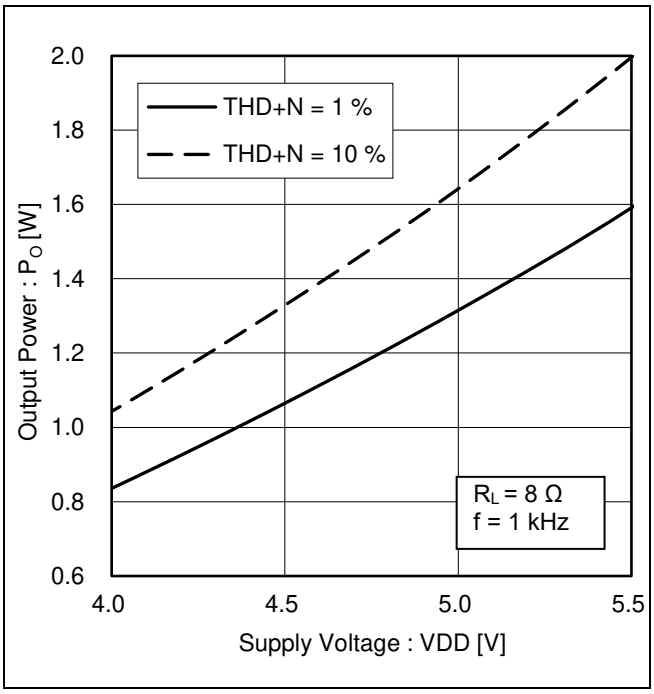


Figure 10. Output Power vs Supply Voltage

Typical Performance Curves - continued

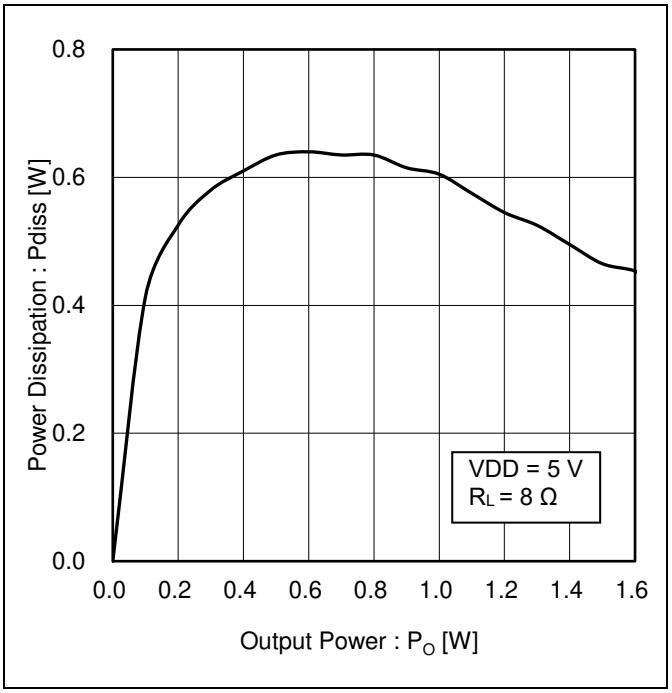


Figure 11. Power Dissipation vs Output Power

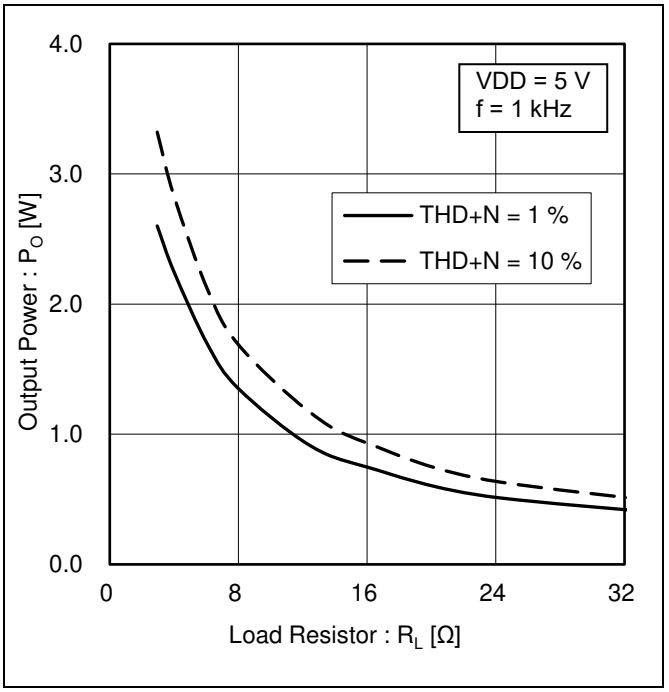


Figure 12. Output Power vs Load Resistor

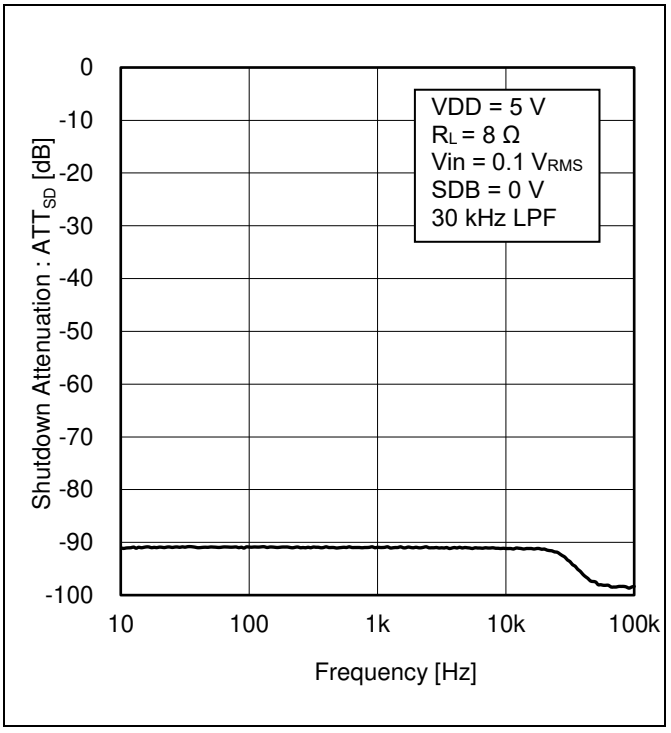


Figure 13. Shutdown Attenuation vs Frequency

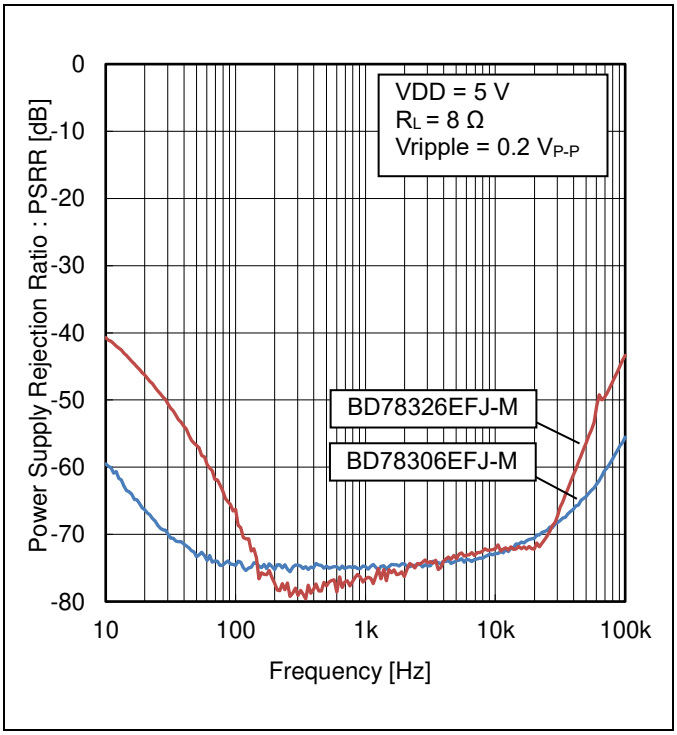


Figure 14. Power Supply Rejection Ratio vs Frequency

Timing Chart

Power on/power down sequences of the VDD pin and the SDB pin are shown.
Follow the sequences below when power on and power down.

1. Power on sequence
   (1) Start up voltage of the VDD pin and the SDB pin in order

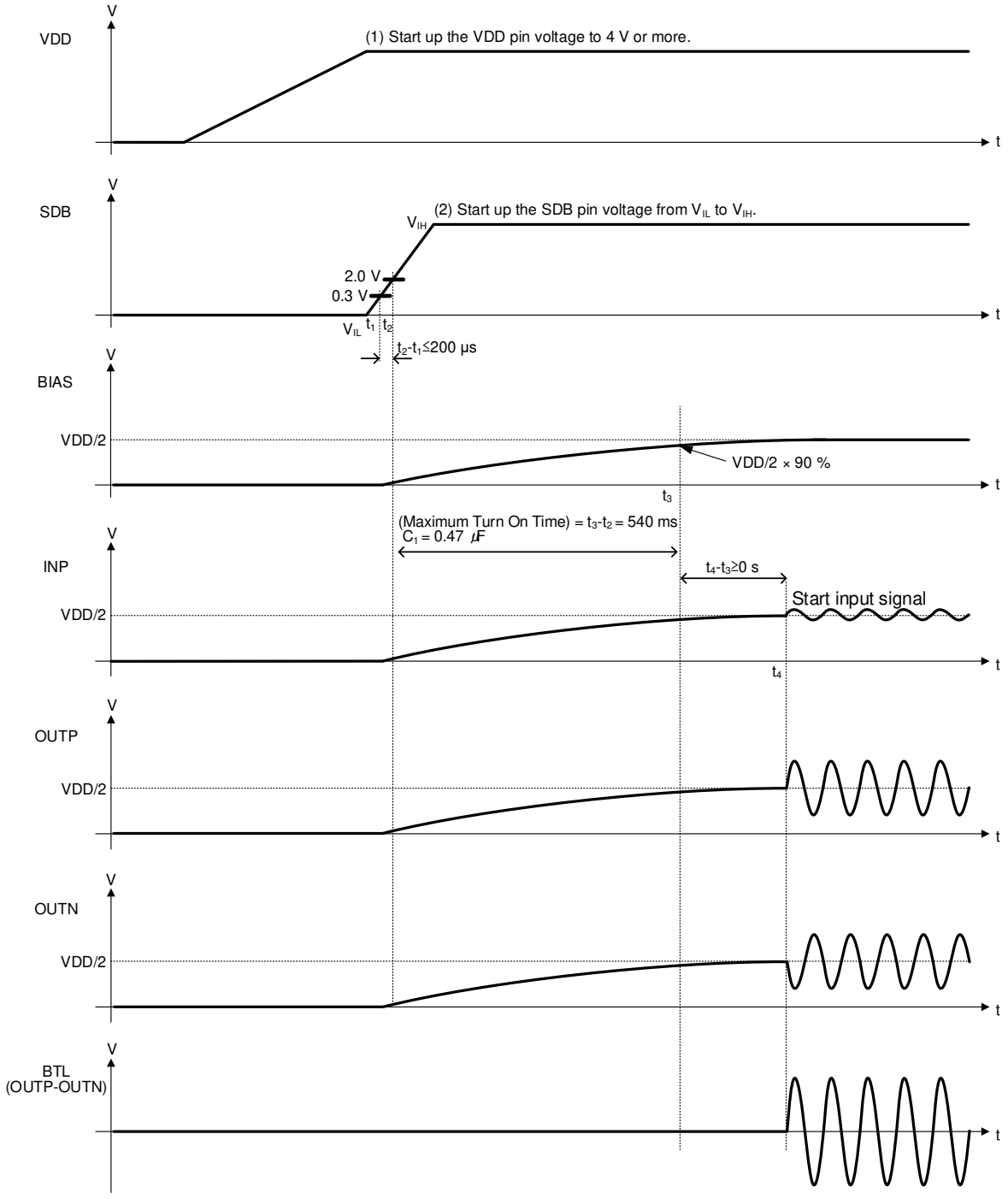
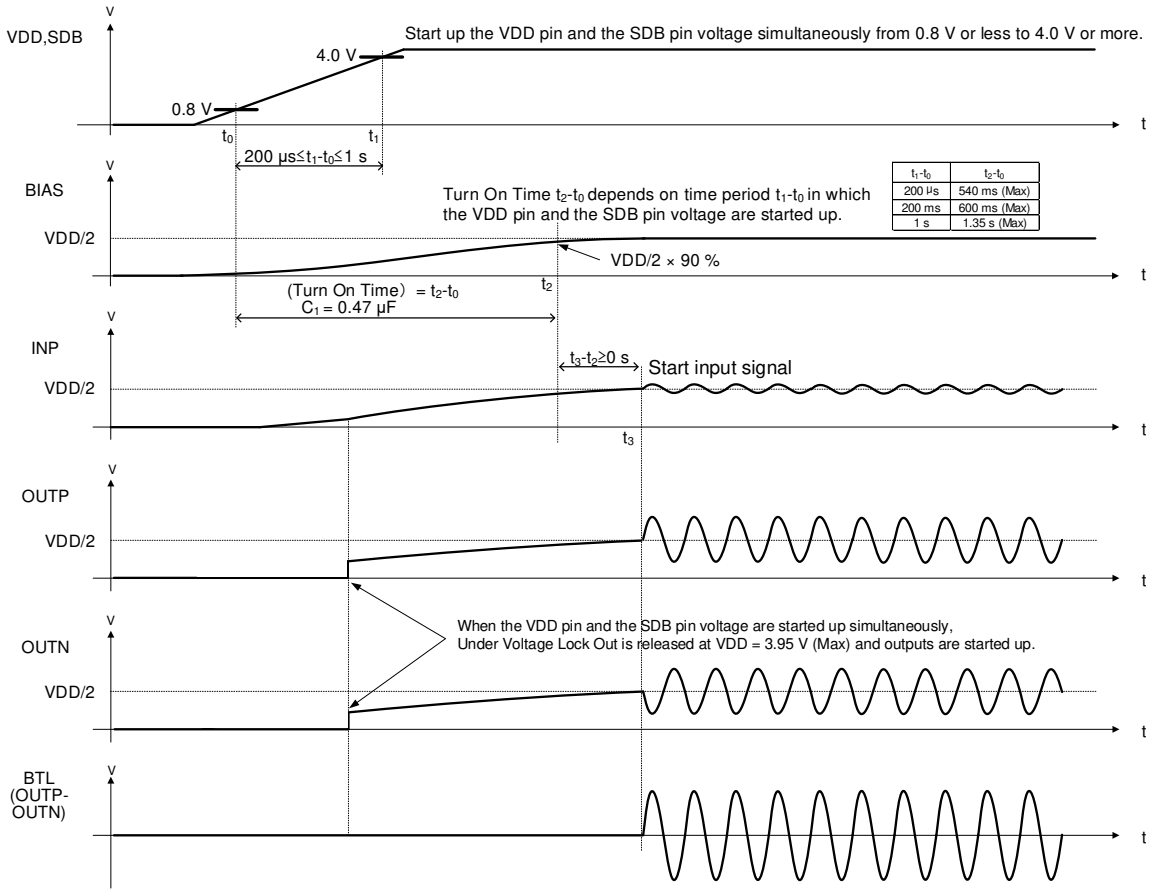


Figure 15. Power On Sequence

Caution:
Start to input signal after waiting maximum Turn On Time 540 ms (C_1 = 0.47 µF) after setting the SDB pin voltage high.

Timing Chart – continued

(2) Start up voltage of the VDD pin and the SDB pin simultaneously



Caution:
Start up waveforms in the figure above, are described in case the VDD pin and the SDB pin voltage are started up from 0 V to 5 V in time period of 300 ms as an example.

Figure 16. Power On Sequence

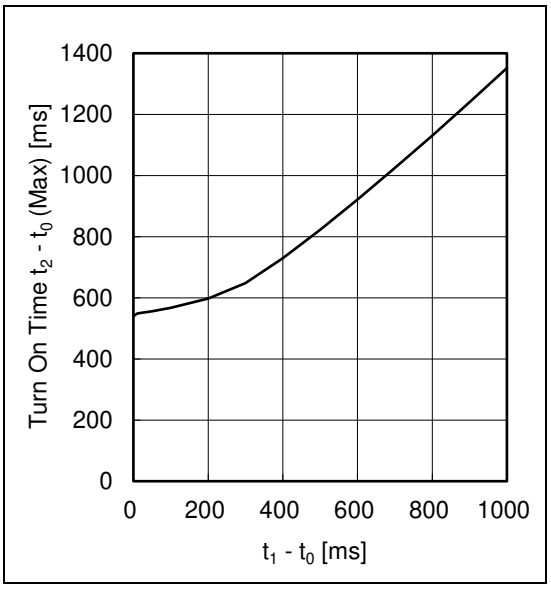


Figure 17. Turn On Time $t_2 – t_0$ (Max) vs $t_1 - t_0$

Caution:
Start to input signal after waiting maximum Turn On Time after setting the VDD pin and the SDB pin voltage high.
Turn On Time depends on time period in which the VDD pin and the SDB pin voltage are started up.

Timing Chart – continued

2. Power down sequence
   (1) Turn down voltage of the SDB pin and the VDD pin in order

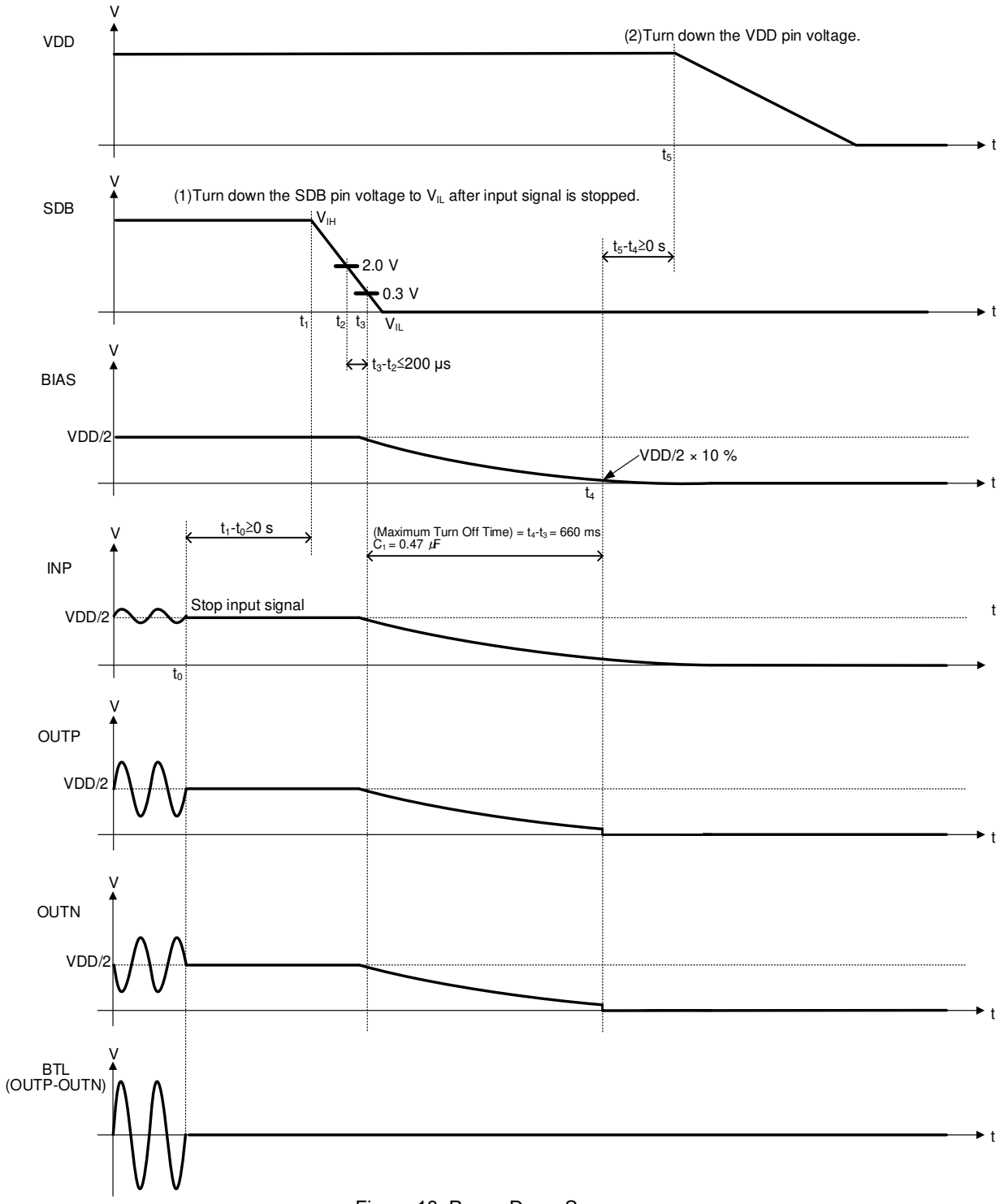
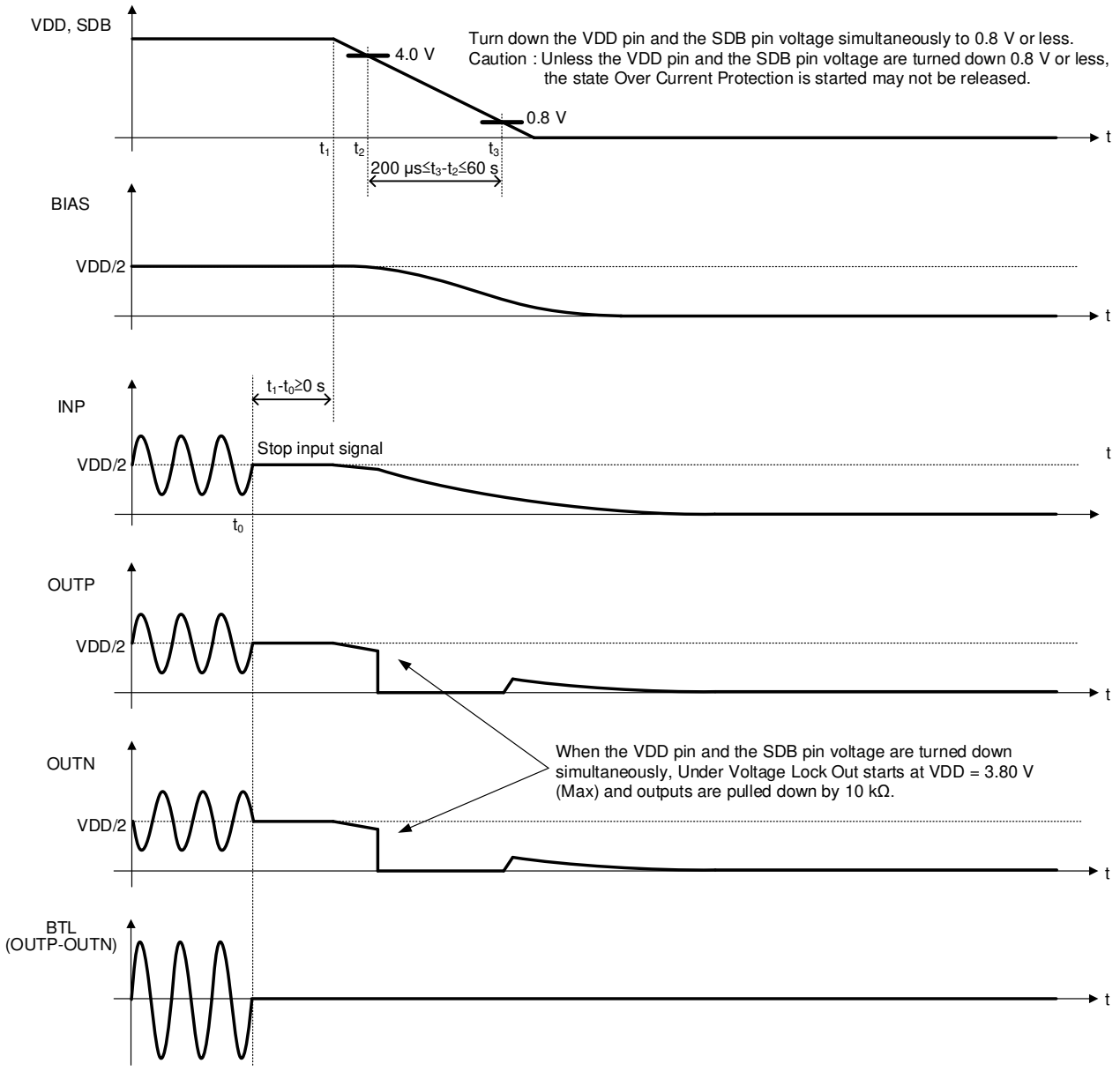


Figure 18. Power Down Sequence

Caution:
Turn down the VDD pin voltage after waiting maximum Turn Off Time 660 ms (C_1 = 0.47 µF) after setting the SDB pin voltage low. Output waveform may be clipped if signal is still input after Turn Off starts.

Timing Chart – continued

(2) Turn down voltage of the VDD pin and the SDB pin simultaneously



Caution:
Turn down waveforms in the figure above, are described in case the VDD pin and the SDB pin voltage are turned down from 5 V to 0 V in time period of 300 ms as an example.

Figure 19. Power Down Sequence

Application Examples

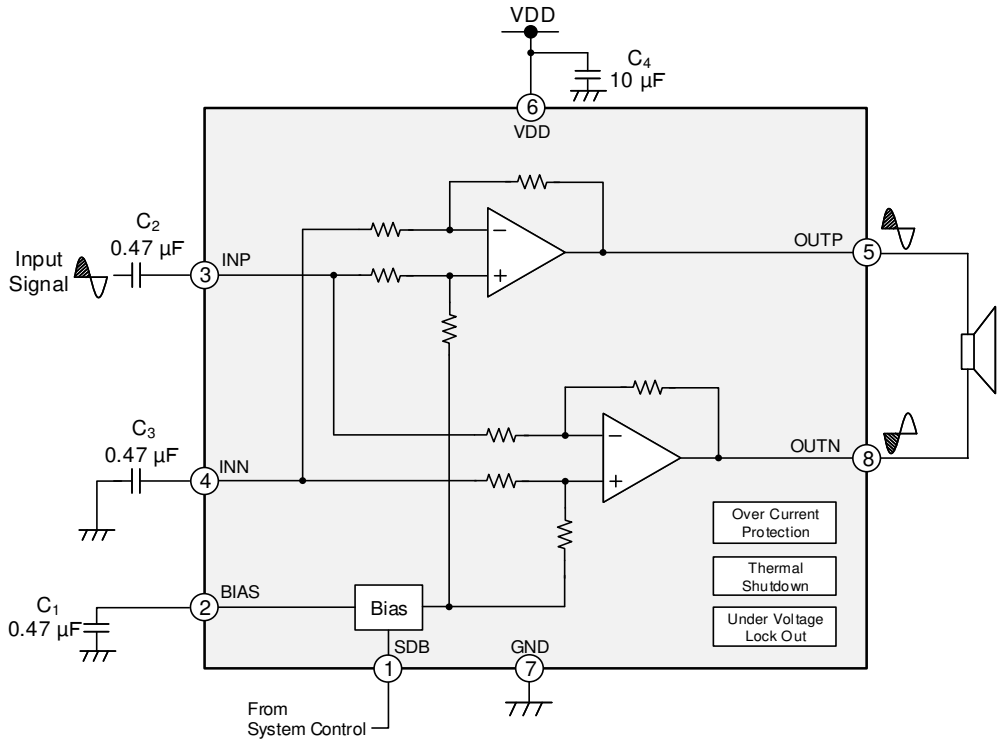


Figure 20. Single-ended Input

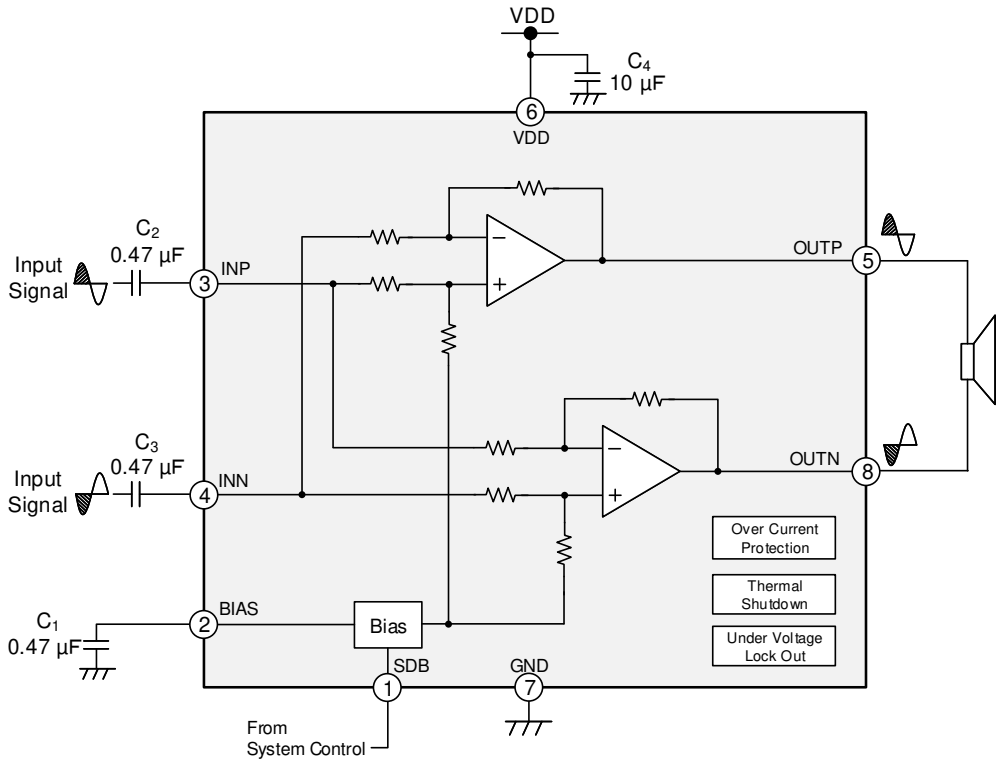


Figure 21. Differential Input

Parts	Parts Symbol	Value	Manufacturer	Product No.
Capacitor	C_1, C_2, C_3	0.47 µF	MURATA	GCM188R71E474KA64
	C_4	10 µF	MURATA	GRT188C81C106ME13

(This is only example of components externally connected.)

Selection of Components Externally Connected

1. Input Coupling Capacitors (C_2, C_3)
   The frequency characteristic of input composes high pass filter (Figure 22. HPF) by input impedance Z_{IN} and input coupling capacitor C_2, C_3 (= C_{IN}).
   Cut off frequency f_C is determined in following equation, set C_{IN} considering it.

$$f_C = \frac{1}{2\pi \times Z_{IN} \times C_{IN}} \quad [\text{Hz}]$$

   In case that Z_{IN} = 45 kΩ and C_{IN} = 0.47 μF, f_C is 7.5 Hz (Typ).

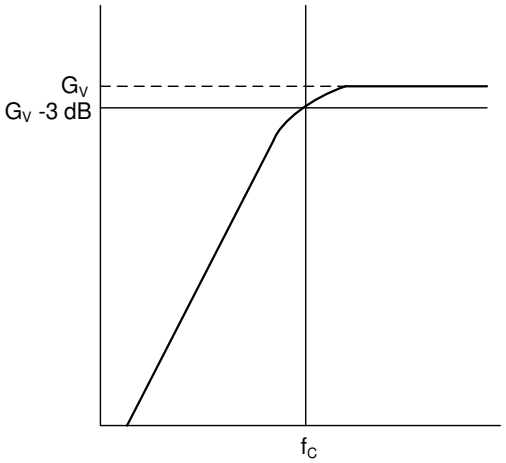


Figure 22. HPF

   The capacitance of C_2 and C_3 should be the same at the INP and INN pins.
   If the capacitance is different, audio characteristics such as THD+N may get worse and pop noise may be large.

2. Power Supply Decoupling Capacitor (C_4)
   Power supply decoupling capacitor influences audio characteristics such as THD+N. Locate low ESR capacitor close to the VDD pin.
   Capacitance of C_4 should be 10 μF or more.

3. The BIAS pin Capacitor (C_1)
   The BIAS pin capacitor influences audio characteristic such as PSRR and THD+N. Locate low ESR capacitor close to the BIAS pin.
   Determine capacitance of C_1 included in the range below, including variation and temperature characteristic also.

   Turn On Time and Turn Off Time are also determined by capacitance of the BIAS pin capacitor.
   Refer to the following section "Turn On and Turn Off".

	Capacitance		
	Min	Typ	Max
C_1	0.35 μF	0.47 μF	0.59 μF

Turn On and Turn Off

This IC has built-in circuit controls transition time of the OUTP pin and the OUTN pin when the operation mode is switched between active (SDB = High) and shutdown (SDB = Low). It achieves reducing pop noise.

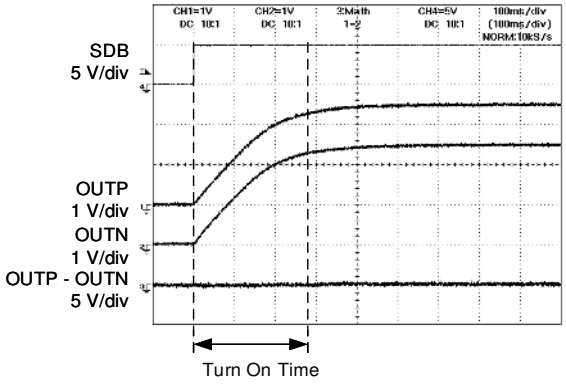


Figure 23. Turn On Waveform

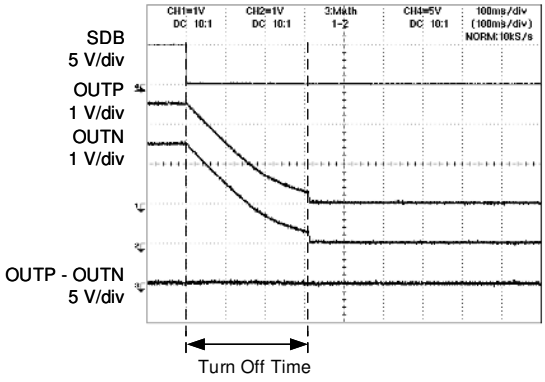


Figure 24. Turn Off Waveform

Following table shows Turn On Time and Turn Off Time with C_1 = 0.47 µF.

C_1	Turn On Time	Turn Off Time
0.47 µF	270 ms (Typ) 540 ms (Max)	330 ms (Typ) 660 ms (Max)

Turn On Time is defined as the time until the BIAS pin voltage rises to 90 % of VDD/2 after the SDB pin voltage is Low to High.
Turn Off Time is defined as the time until the BIAS pin voltage falls to 10 % of VDD/2 after the SDB pin voltage is High to Low.
Turn On Time and Turn Off Time may vary from typical value as the table above.
Maximum value above is calculated assuming that variation of resistors in IC: ±60 % (-40 °C to +105 °C), accuracy of C_1: ±25 % (including variation and temperature characteristic).

Protection Functions

This IC has protection functions that detect several kinds of abnormal conditions and protect itself.

Protection Functions	Detection and Release Condition		State of Output Pins
Over Current Protection	Detection	The OUTP pin or the OUTN pin is shorted to the VDD pin / the GND pin.	Signal Output stopped and Latched to High-Z
	Release	Over Current Protection is released after setting SDB to Low and waiting Turn Off Time. After that, the IC becomes normal operation state by setting the SDB pin to High.	Signal Output available
Thermal Shutdown	Detection	Tj : 180 °C (Typ) or more	Signal Output stopped and Pulled down by 10 kΩ (Typ)
	Release	Tj : 160 °C (Typ) or less (released automatically)	Signal Output available
Under Voltage Lock Out	Detection	VDD : 3.43 V (Typ) / 3.80 V (Max) or less Ta = -40 °C to +105 °C	Signal Output stopped and Pulled down by 10 kΩ (Typ)
	Release	VDD : 3.58 V (Typ) / 3.95 V (Max) or more Ta = -40 °C to +105 °C (released automatically)	Signal Output available

Protection Functions - continued

1. Over Current Protection
   (1) Over Current Protection (Short to the VDD pin)
   In case that the OUTP pin or the OUTN pin is shorted to the VDD pin, Over Current Protection starts to stop output signal and latch output pins to High-Z.
   Once Over Current Protection is started, the latch state is not released automatically even if the OUTP pin and the OUTN pin are not shorted to the VDD pin. Over Current Protection is released by shutdown.

Detection	The OUTP pin or the OUTN pin is shorted to the VDD pin.
Release	Over Current Protection is released after setting the SDB pin to Low and waiting Turn Off Time (660 ms Max). After that, it is possible that the IC outputs signal by setting the SDB pin to High.

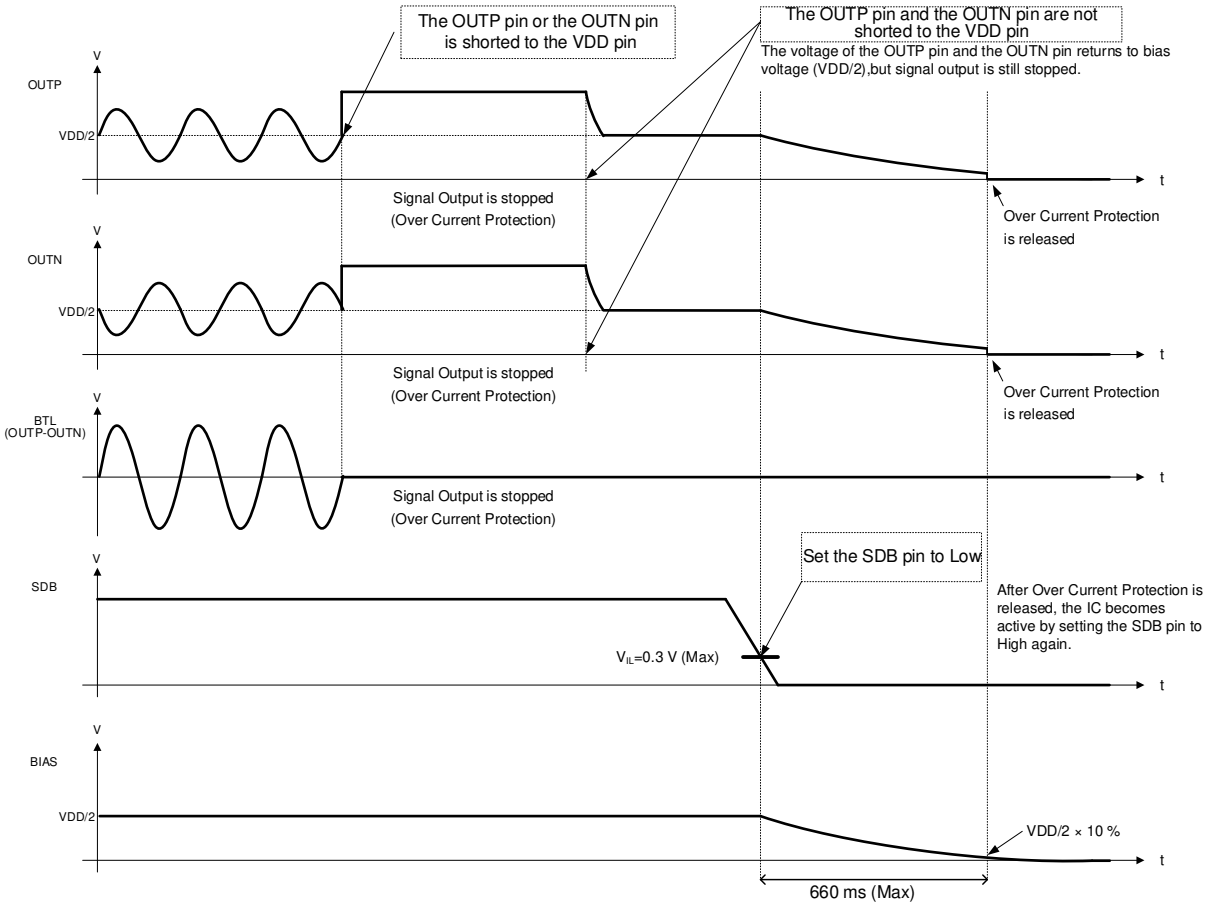


Figure 25. Over Current Protection (Short to the VDD pin)

Protection Functions – continued

(2) Over Current Protection (Short to the GND pin)
In case that the OUTP pin or the OUTN pin is shorted to the GND pin, Over Current Protection starts to stop output signal and latch output pins to High-Z.
Once Over Current Protection is started, the latch state is not released automatically even if the OUTP pin and the OUTN pin are not shorted to the GND pin, Over Current Protection is released by shutdown.

Detection	The OUTP pin or the OUTN pin is shorted to the GND pin
Release	Over Current Protection is released after setting the SDB pin to Low and waiting Turn Off Time (660 ms Max). After that, it is possible that the IC outputs signal by setting the SDB pin to High.

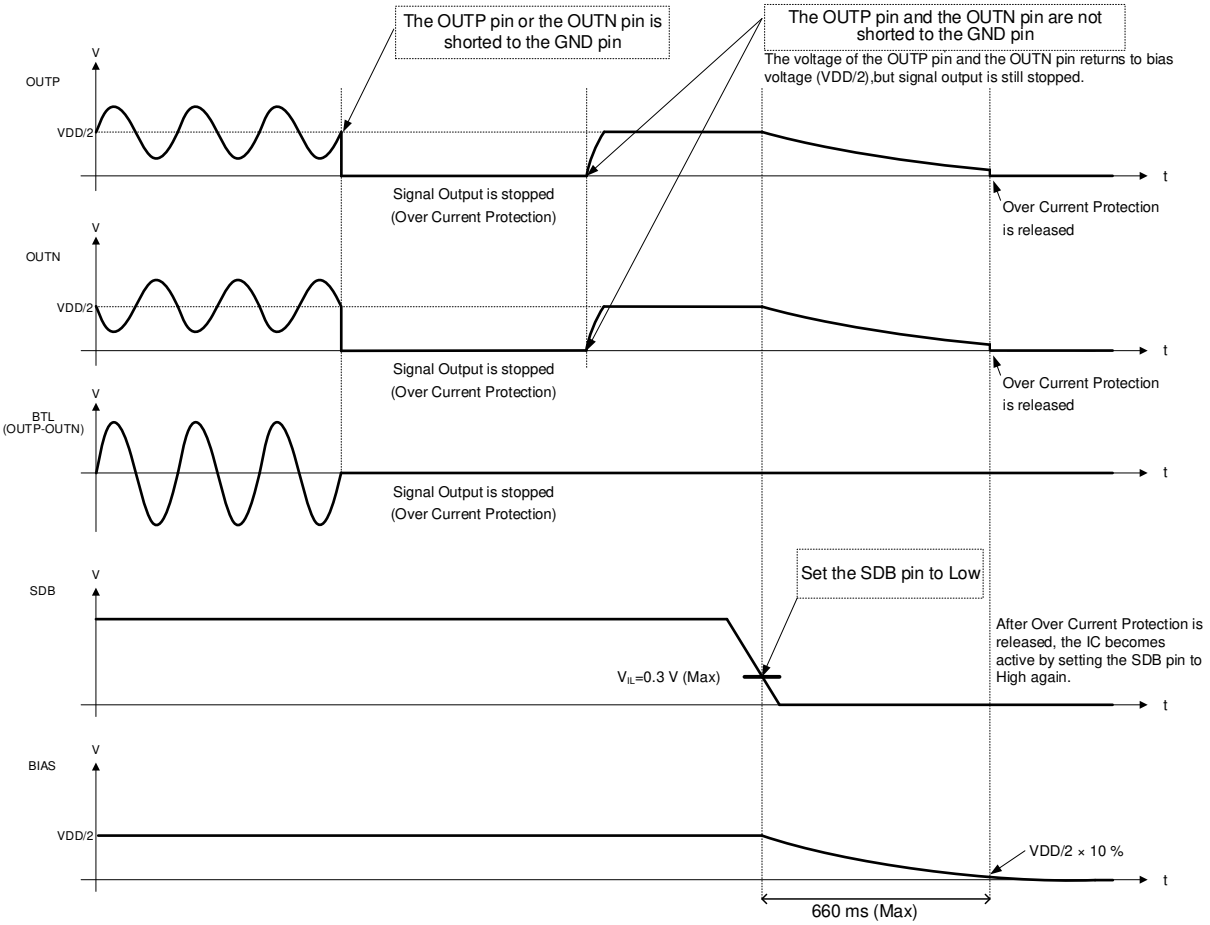


Figure 26. Over Current Protection (Short to the GND pin)

Protection Functions – continued

2. Thermal Shutdown
In case that Tj rises to 180 °C (Typ) or more, Thermal Shutdown starts to stop output signal and pulls down output pins by 10 kΩ (Typ).

Detection	Tj : 180 °C (Typ) or more
Release	Tj : 160 °C (Typ) or less (released automatically)

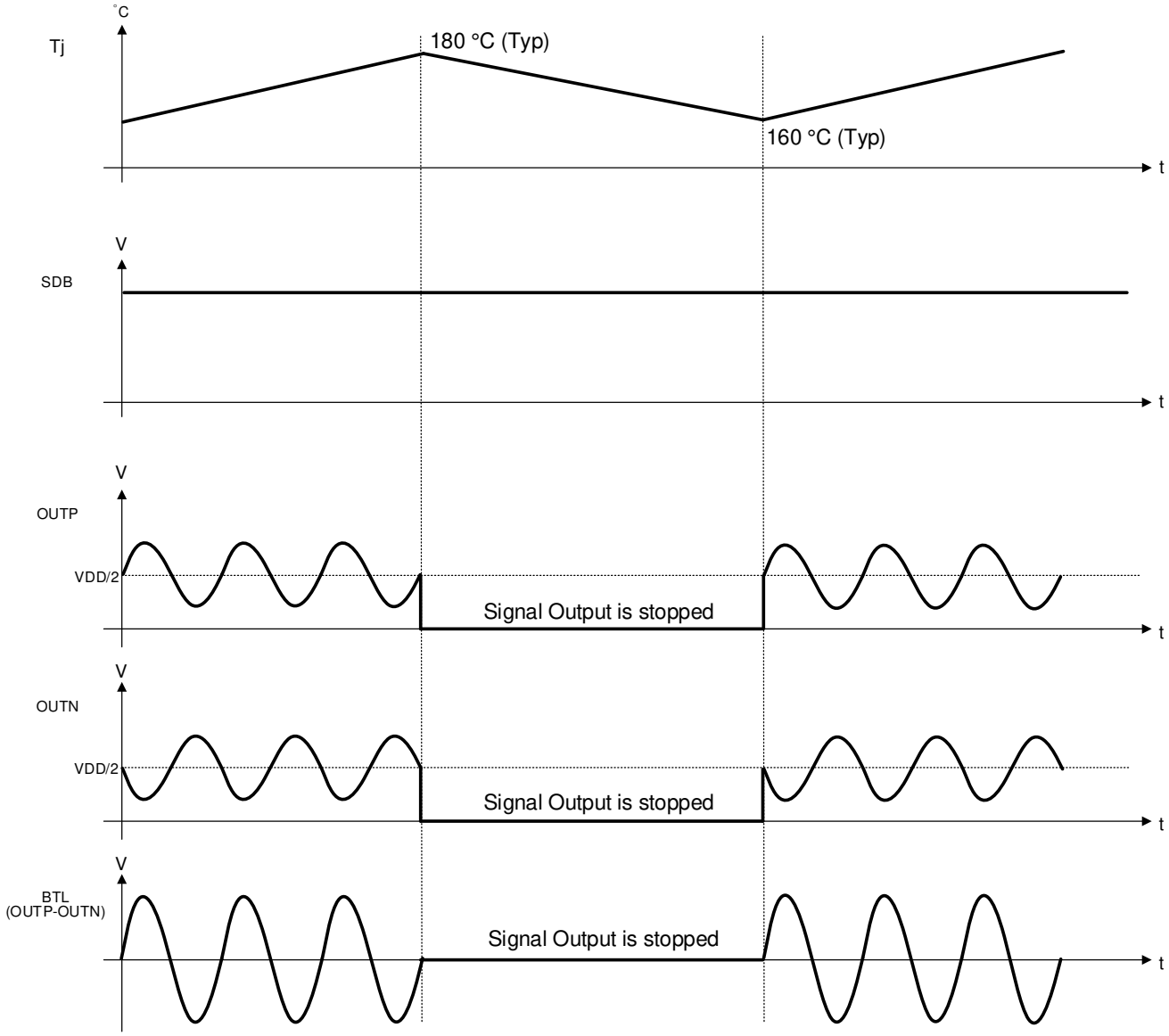


Figure 27. Thermal Shutdown

Protection Functions – continued

3. Under Voltage Lock Out
In case that VDD drops to 3.43 V (Typ) or less, Under Voltage Lock Out starts to stop output signal and pulls down output pins by 10 kΩ (Typ).

Detection	VDD : 3.43 V (Typ) / 3.80 V (Max) or less
Release	VDD : 3.58 V (Typ) / 3.95 V (Max) or more (released automatically)

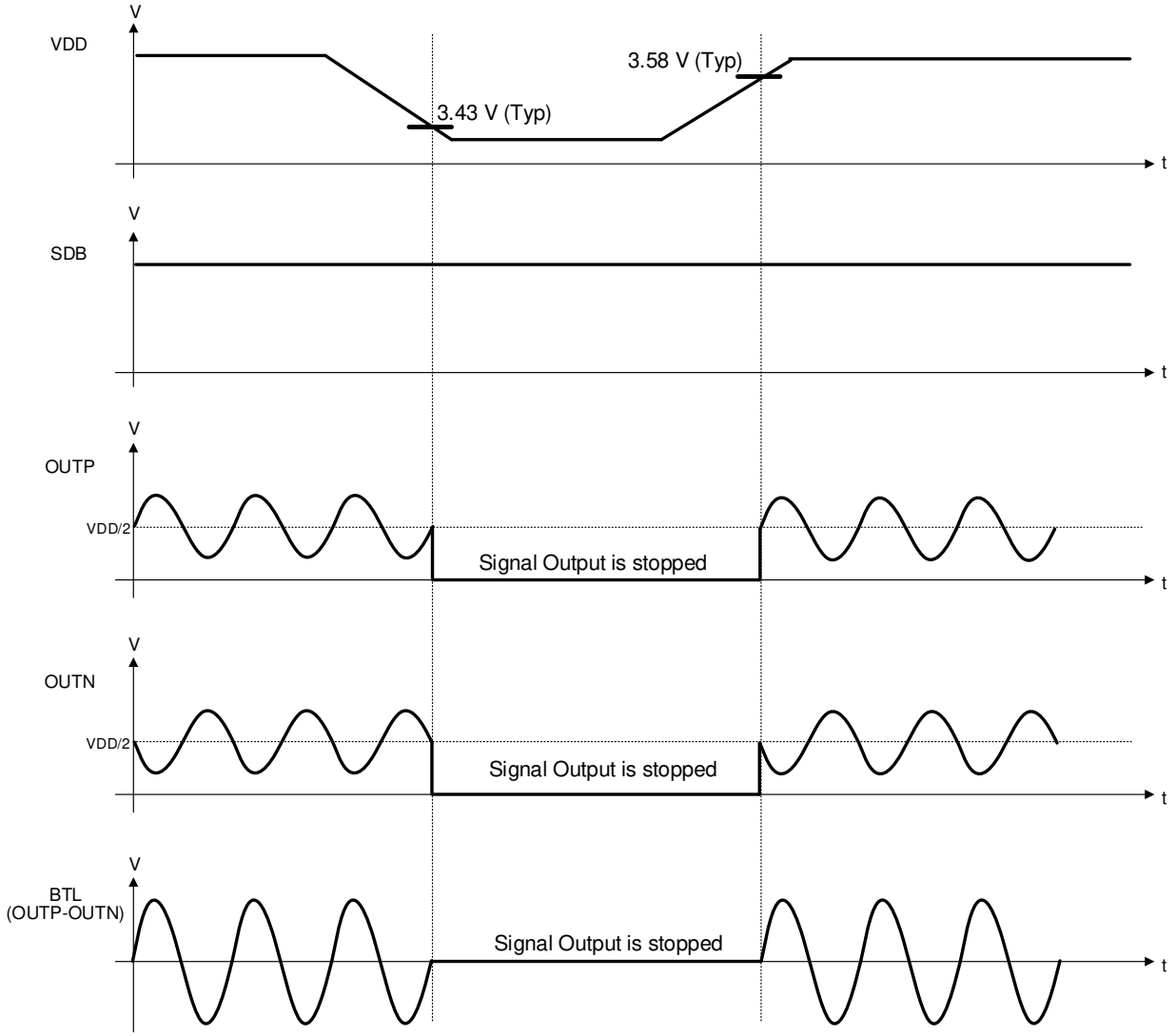
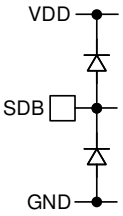
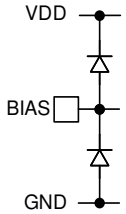
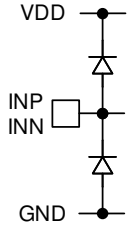
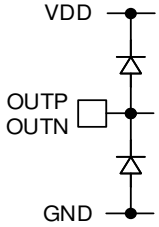
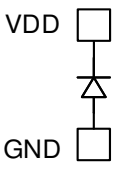


Figure 28. Under Voltage Lock Out

Caution:
In case that the voltage of VDD falls to 3.80 V (Max) or less by fluctuation of the power supply voltage, note that Under Voltage Lock Out may start.
Under the condition that R_L = 6 Ω, depending on output signal level, back electromotive force may occur because of the fluctuation of load current when Under Voltage Lock Out starts and parasitic inductance inside the IC.
Similarly, IR voltage drop may occur because of load current and parasitic resistance of the VDD pin.
These back electromotive force or IR voltage drop may cause intermittent action between “Detection” and “Release”.
This action may be heard as noise under the condition the voltage of the VDD pin is near the threshold voltage of detection.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Voltage	Equivalent Circuit	Pin Description
1	SDB	-		Shutdown High : Active Low : Shutdown
2	BIAS	2.5 V		Bias
3 4	INP INN	2.5 V		Positive Differential Input Negative Differential Input
5 8	OUTP OUTN	2.5 V		Positive Output Negative Output
6	VDD	5 V		Power Supply
7	GND	0 V		GND

Pin voltage is the value when VDD is 5.0 V and the operating mode is active (The SDB pin is High).

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

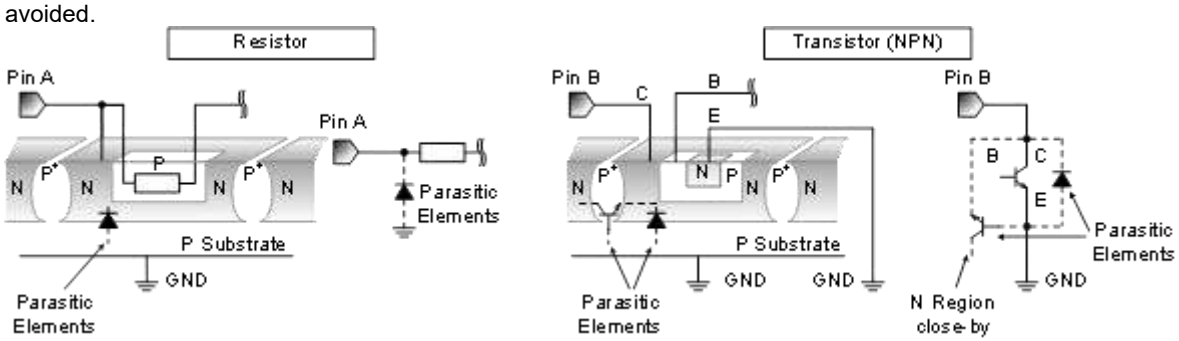


Figure 29. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

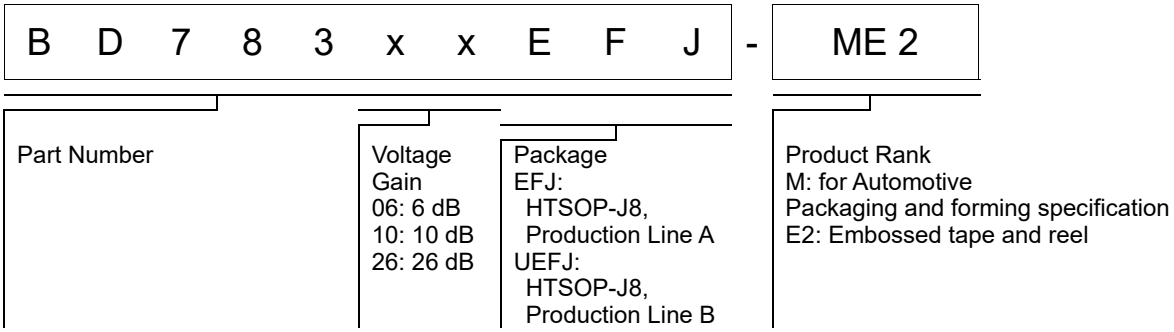
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

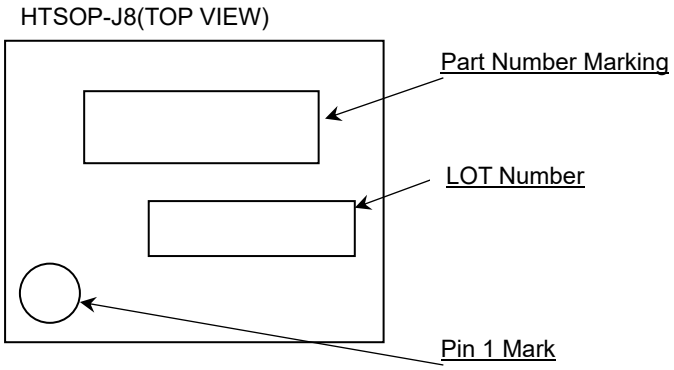


Lineup

Part Number	Voltage Gain	Part Number Marking	Production Line*(Note 1)*
BD78306EFJ-M	6 dB	78306	A
BD78306UEFJ-M		78306U	B
BD78310EFJ-M	10 dB	78310	A
BD78310UEFJ-M		78310U	B
BD78326EFJ-M	26 dB	78326	A
BD78326UEFJ-M		78326U	B

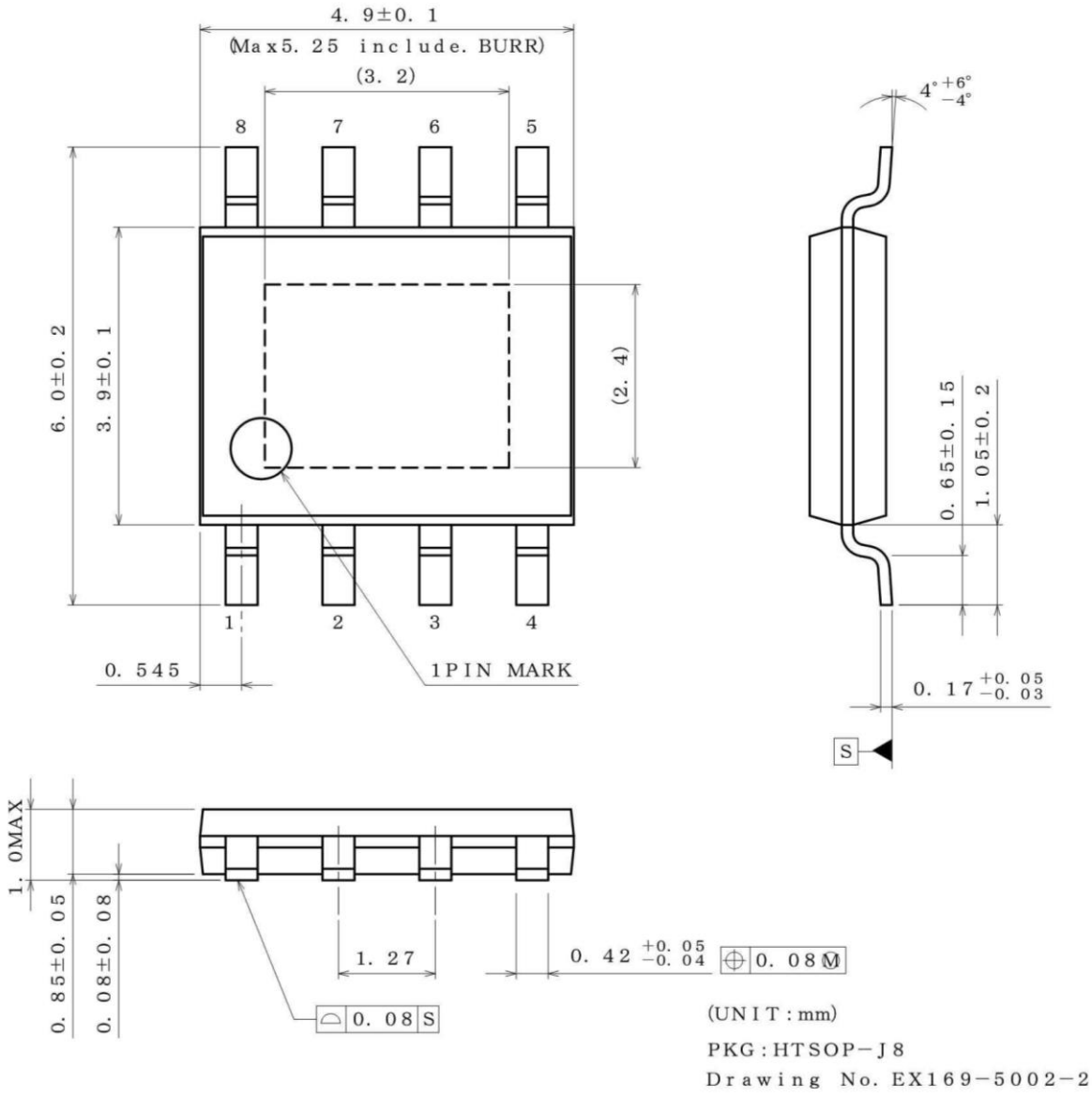
(Note 1) For the purpose of improving production efficiency, Production Line A and B have a multi-line configuration.
Electric characteristics noted in Datasheet does not differ between Production Line A and B.
Production Line B is recommended for new product.

Marking Diagram



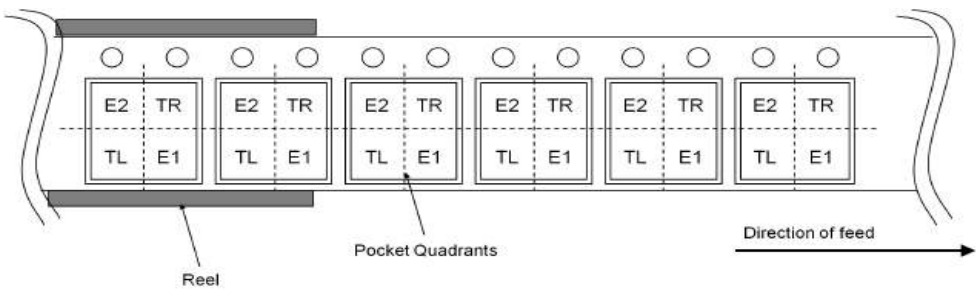
Physical Dimension and Packing Information

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	**Embossed carrier tape**
Quantity	**2500pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**



Revision History

Date	Revision	Changes
19.Jul.2019	001	New Release
28.Mar.2023	002	page 1 Changed the notation from typical output to the maximum output. '1.2 W' → '2.8 W High Power' Addition of part numbers corresponding to production line B page 2 Addition of part numbers corresponding to production line B in the block diagram. Deletion of part numbers under development. page 4 Addition of part numbers corresponding to production line B in Electrical Characteristics 1. Deletion of part numbers under development in Electrical Characteristics 1. page 6 Deletion of part numbers under development from characteristics data page 23 Addition of part numbers corresponding to production line B in Ordering Part Number Information. Deletion of part numbers under development. Add part numbers corresponding to production line B to the lineup. Delete part numbers under development.

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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