D2999, DECEMBER 1985—REVISED OCTOBER 1989

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Collector N-P-N Outputs Using Ramped Supply**
- **300-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

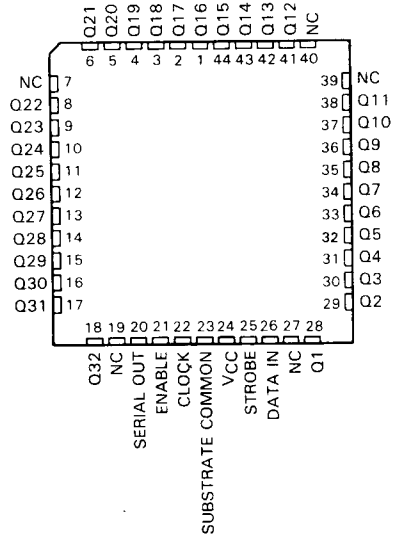
description

These devices are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-collector n-p-n transistors. The SN65558 and SN75558 output sequences are reversed from the SN65557 and SN75557 for ease in printed circuit board layout.

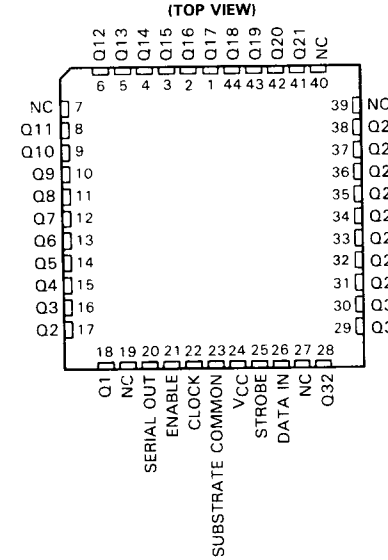
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the SUBSTRATE COMMON terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The Serial Data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

The SN65557 and SN65558 are characterized for operation from −40°C to 85°C. The SN75557 and SN75558 are characterized for operation from 0°C to 70°C.

SN65557, SN75557 . . . FN PACKAGE
(TOP VIEW)



SN65558, SN75558 . . . FN PACKAGE
(TOP VIEW)

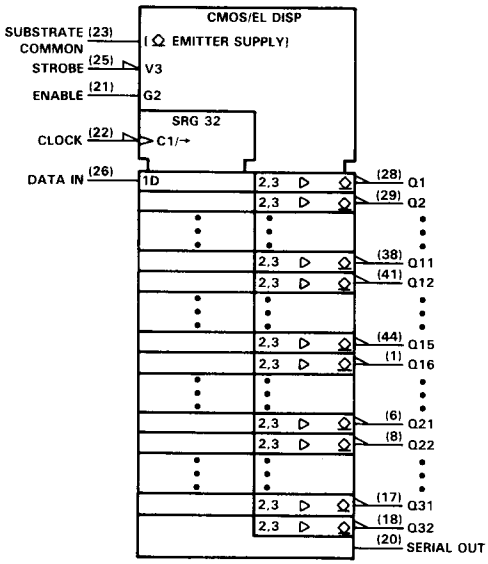


NC—No internal connection

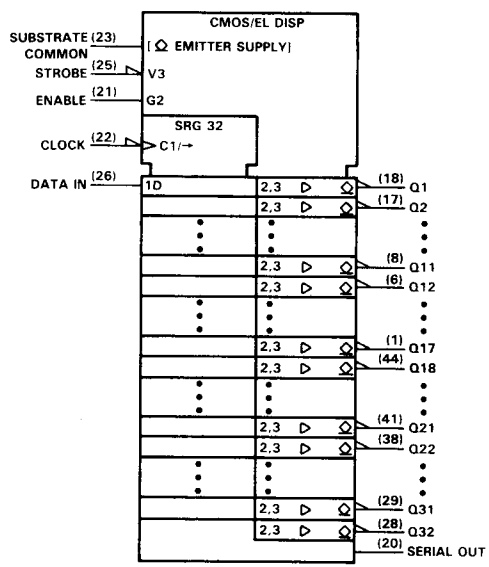
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process

logic symbols†

SN65557, SN75557

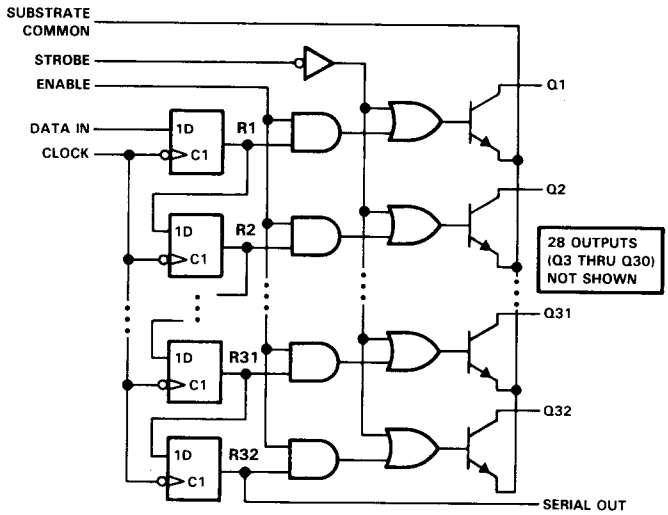


SN65558, SN75558



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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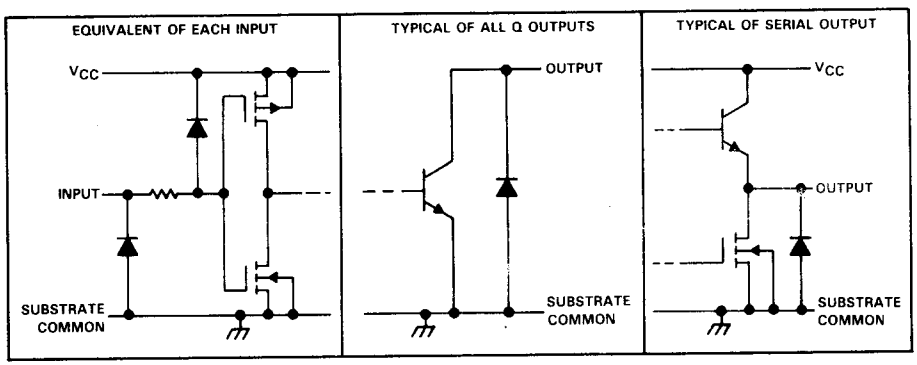
FUNCTION TABLE

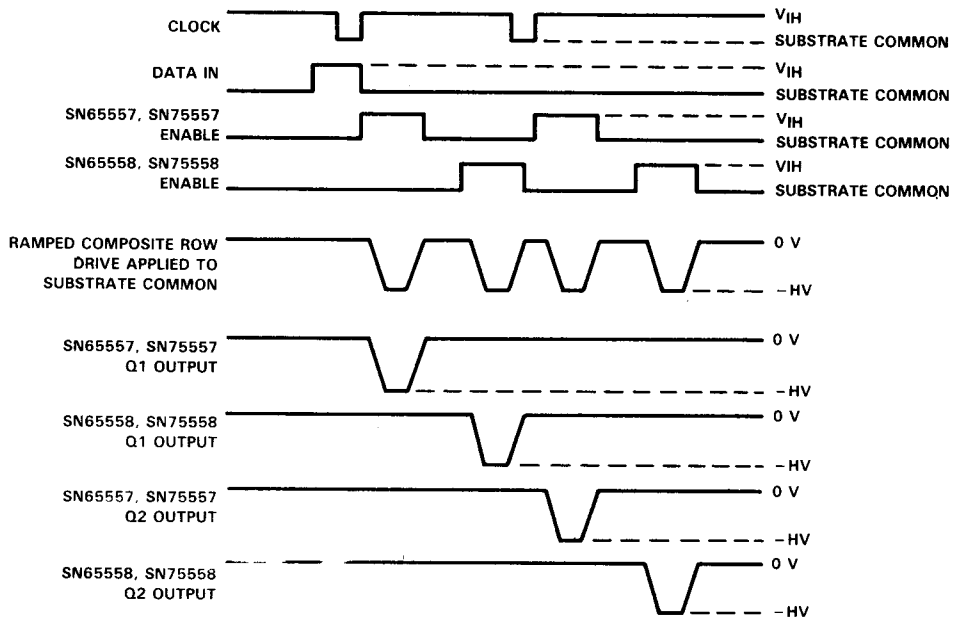
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	OUTPUTS	
	CLOCK	ENABLE	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No Change	R32	Determined by ENABLE and STROBE
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

schematics of inputs and outputs



typical operating sequence



HV = High voltage

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Off-state output voltage, $V_{O(off)}$ (see Note 2) . . . . . 110 V
Input voltage . . . . . V_{CC} + 0.3 V
Substrate common terminal current (see Note 3) . . . . . 750 mA
Continuous total power dissipation at (or below)
25°C free-air temperature (see Note 4) . . . . . 1700 mW
Operating free-air temperature range: SN65557, SN65558 . . . . . −40°C to 85°C
SN75557, SN75558 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON terminal.
2. Data must be clocked into the shift register and Q outputs enabled prior to ramping SUBSTRATE COMMON to −HV (see typical operating sequence).
3. Duty cycle is limited by package dissipation.
4. For operation above 25°C free-air temperature, derate linearly to 1088 mW at 70°C, and 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			10.8	12	15	V
High-level input voltage, V_{IH} (see Figure 1)		V_{CC} = 10.8 V	8.1		11.1	V
		V_{CC} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)		V_{CC} = 10.8 V	−0.3		2.7	V
		V_{CC} = 15 V	−0.3		3.75	
Off-state Q output voltage, $V_{O(off)}$			−0.3		100	V
On-state Q output current, $I_{O(on)}$, duty cycle ≤ 1%, V_{CC} = 15 V					300	mA
Rate of rise for SUBSTRATE COMMON, dV/dt (see Figure 4)					100	V/μs
Clock frequency, f_{clock}			0		4	MHz
Pulse duration, CLOCK high or low, t_w			125			ns
Setup time, t_{su}	DATA IN before CLOCK↓ (see Figure 2)		50			ns
	ENABLE before SUBSTRATE COMMON ↓ (see Figure 4)		500			
Hold time, t_h, DATA IN after CLOCK↓ (see Figure 2)			100			ns
Operating free-air temperature, T_A		SN65557, SN65558	−40		85	°C
		SN75557, SN75558	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 12 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN65557 SN65558		SN75557 SN75558		UNIT
				MIN	MAX	MIN	MAX	
$I_{O(off)}$	Off-state Q output current		V_O = 100 V		20		10	μA
V_{OH}	High-level output voltage	Serial outputs	I_O = −100 μA	10.5		10.5		V
V_{VOL}	Low-level output voltage	Q outputs	I_{OL} = 300 mA		20		10	V
		Serial output	I_{OL} = 100 μA		1		1	
I_{IH}	High-level input current		V_I = 12 V		1		1	μA
I_{IL}	Low-level input current		V_I = 0		−1		−1	μA
I_{CC}	Supply current from V_{CC}				250		250	μA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUTPUT from CLOCK	C_L = 20 pF to SUBSTRATE COMMON (see Figure 3)		200	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUTPUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	dV/dt = 100 V/μs, STROBE at V_{CC}, R_L = 2 kΩ to 60 V (see Figure 4)		500	ns

RECOMMENDED OPERATING CONDITIONS

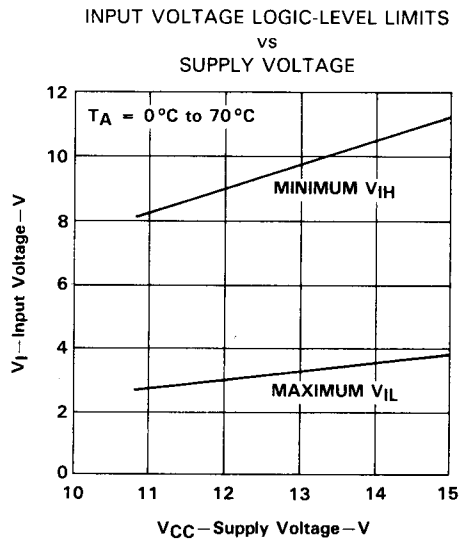

FIGURE 1

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PARAMETER MEASUREMENT INFORMATION

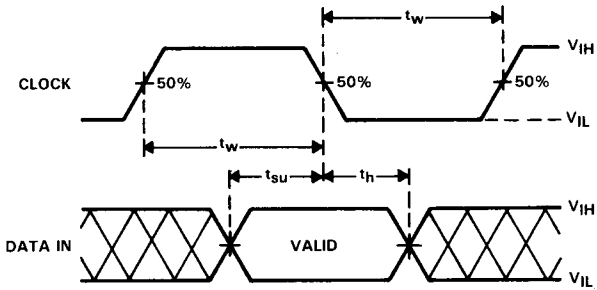

FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

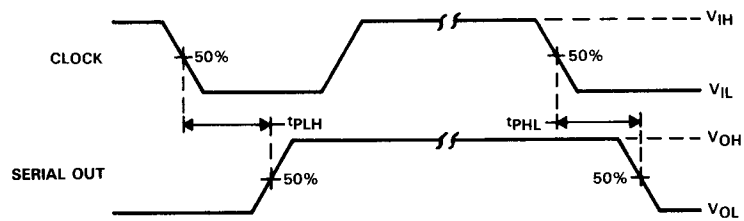

FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

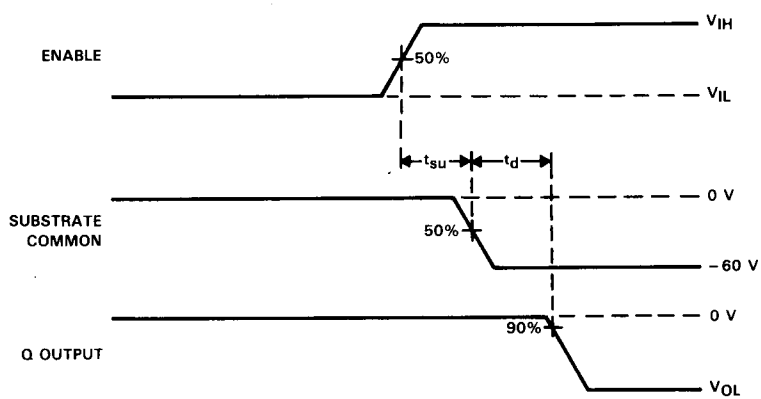

FIGURE 4. VOLTAGE WAVEFORMS FOR TURN ON DELAY TIME, SUBSTRATE COMMON TO Q OUTPUT

TYPICAL CHARACTERISTICS

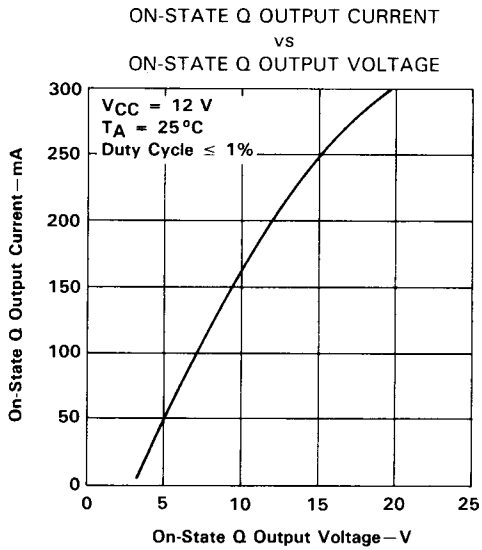

FIGURE 5