JFET Switching Transistors

N-Channel - Depletion

Features

• Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	30	Vdc
Drain - Gate Voltag	V_{DG}	30	Vdc
Gate-Source Voltage	V _{GS}	30	Vdc
Forward Gate Current	I _{G(f)}	50	mAdc
Total Device Dissipation @ T _A = 25°C Derate above 25°C	P _D	350 2.8	mW mW/°C
Operating and Storage Channel Temperature Range	T _{channel} , T _{stg}	-65 to +150	°C

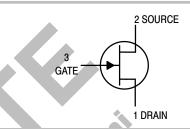
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

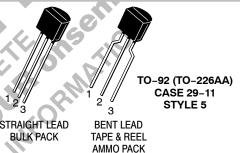




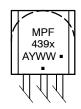
ON Semiconductor®

http://onsemi.com





MARKING DIAGRAM



MPF439x = Device Code

x = 2 or 3

A = Assembly Location

Y = Year
WW = Work Week
• Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]		
MPF4392	TO-92	1000 Units / Bulk		
MPF4392G	TO-92 (Pb-Free)	1000 Units / Bulk		
MPF4393	TO-92	1000 Units / Bulk		
MPF4393G	TO-92 (Pb-Free)	1000 Units / Bulk		
MPF4393RLRP	TO-92	1000 / Ammo Box		
MPF4393RLRPG	TO-92 (Pb-Free)	1000 / Ammo Box		

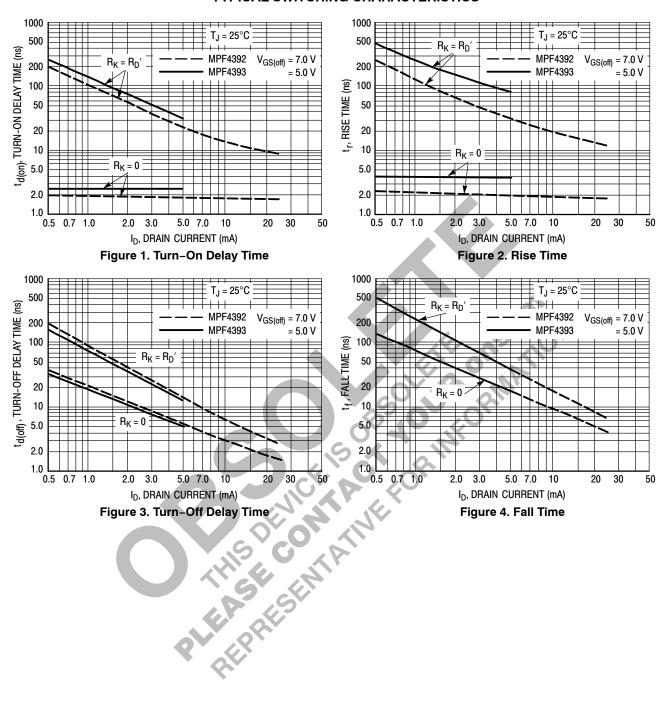
^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	· ·	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS		<u> </u>	I		I	
Gate – Source Breakdown Voltage ($I_G = -1.0 \mu Adc, V_{DS} = 0$)		V _{(BR)GSS}	30	-	-	Vdc
Gate Reverse Current $(V_{GS} = -15 \text{ Vdc}, V_{DS} = 0)$ $(V_{GS} = -15 \text{ Vdc}, V_{DS} = 0, T_A = 100^{\circ}\text{C})$		I _{GSS}	- -	- -	1.0 0.2	nAdc μAdc
		I _{D(off)}	- -	- -	1.0 1.0	nAdc μAdc
Gate Source Voltage (V _{DS} = 15 Vdc, I _D = 10 nAdc)	MPF4392 MPF4393	V _{GS}	-2.0 -0.5	- -	-5.0 -3.0	Vdc
ON CHARACTERISTICS						
Zero – Gate – Voltage Drain Current (Note 1) (V _{DS} = 15 Vdc, V _{GS} = 0)	MPF4392 MPF4393	Ipss	25 5.0	- -	75 30	mAdc
	MPF4392 MPF4393	V _{DS(on)}	- 0		0.4 0.4	Vdc
Static Drain–Source On Resistance (I _D = 1.0 mAdc, V _{GS} = 0)	MPF4392 MPF4393	r _{DS(on)}	0125	(<u> </u>	60 100	Ω
SMALL-SIGNAL CHARACTERISTICS			120			
Forward Transfer Admittance (V_{DS} = 15 Vdc, I_D = 25 mAdc, f = 1.0 kHz) (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 kHz)	MPF4392 MPF4393	y _{fs}	2 <u>6</u>	17 12	- -	mmhos
Drain-Source "ON" Resistance (V _{GS} = 0, I _D = 0, f = 1.0 kHz)	MPF4392 MPF4393	r _{ds(on)}	- -	- -	60 100	Ω
Input Capacitance (V _{GS} = 15 Vdc, V _{DS} = 0, f = 1.0 MHz)	P . (C _{iss}	-	6.0	10	pF
Reverse Transfer Capacitance (V_{GS} = 12 Vdc, V_{DS} = 0, f = 1.0 MHz) (V_{DS} = 15 Vdc, I_{D} = 10 mAdc, f = 1.0 MHz)	TIME	C _{rss}	- -	2.5 3.2	3.5 -	pF
SWITCHING CHARACTERISTICS						
Rise Time (See Figure 2) (I _{D(on)} = 6.0 mAdc) (I _{D(on)} = 3.0 mAdc)	MPF4392 MPF4393	t _r	- -	2.0 2.5	5.0 5.0	ns
Fall Time (See Figure 4) (V _{GS(off)} = 7.0 Vdc) (V _{GS(off)} = 5.0 Vdc) Turn On Time (See Figures 1 and 2)	MPF4392 MPF4393	t _f	- -	15 29	20 35	ns
Turn-On Time (See Figures 1 and 2) (I _{D(on)} = 6.0 mAdc) (I _{D(on)} = 3.0 mAdc)	MPF4392 MPF4393	t _{on}	- -	4.0 6.5	15 15	ns
Turn-Off Time (See Figures 3 and 4) (V _{GS(off)} = 7.0 Vdc) (V _{GS(off)} = 5.0 Vdc)	MPF4392 MPF4393	t _{off}	- -	20 37	35 55	ns

^{1.} Pulse Test: Pulse Width \leq 300 $\mu\text{s},$ Duty Cycle \leq 3.0%.

TYPICAL SWITCHING CHARACTERISTICS



 $V_{GG} + V_{DS}$.

flow is reversed.

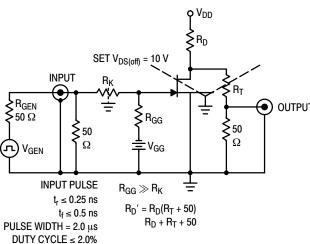
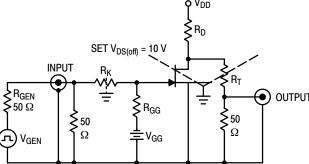
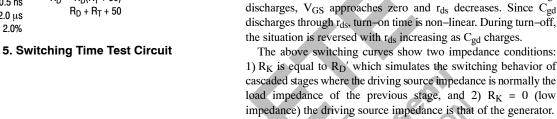


Figure 5. Switching Time Test Circuit



OUTPUT



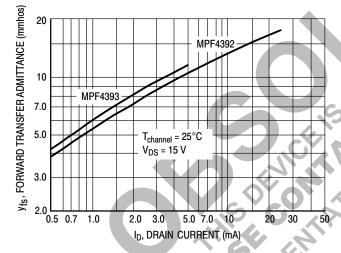
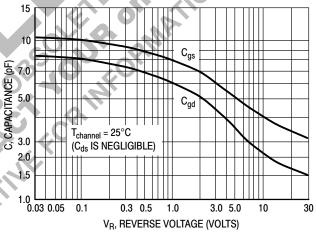


Figure 6. Typical Forward Transfer Admittance



NOTE 1 The switching characteristics shown above were measured using a

test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage (-V_{GG}). The

Drain-Source Voltage (VDS) is slightly lower than Drain Supply Voltage (VDD) due to the voltage divider. Thus Reverse Transfer

Capacitance (Crss) or Gate-Drain Capacitance (Cgd) is charged to

During the turn-on interval, Gate-Source Capacitance (Cgs)

discharges through the series combination of R_{Gen} and R_K. C_{gd}

must discharge to $V_{DS(on)}$ through R_G and R_K in series with the

parallel combination of effective load impedance (R'D) and

Drain-Source Resistance (rds). During the turn-off, this charge

resistance r_{ds} is a function of the gate-source voltage. While C_{gs}

Predicting turn-on time is somewhat difficult as the channel

Figure 7. Typical Capacitance

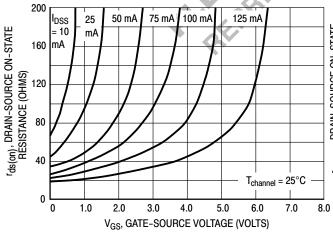


Figure 8. Effect of Gate-Source Voltage On Drain-Source Resistance

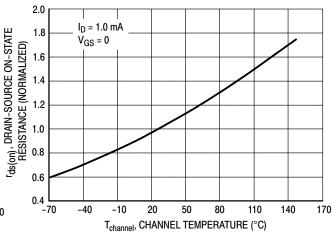


Figure 9. Effect of Temperature On **Drain-Source On-State Resistance**

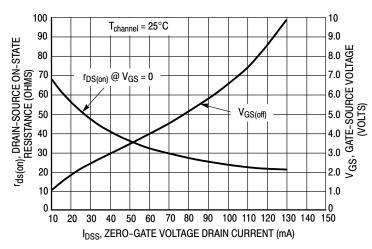


Figure 10. Effect of I_{DSS} On Drain-Source Resistance and Gate-Source Voltage

NOTE 2

The Zero–Gate–Voltage Drain Current (I_{DSS}), is the principle determinant of other J–FET characteristics. Figure 10 shows the relationship of Gate–Source Off Voltage ($V_{GS(off)}$) and Drain–Source On Resistance ($r_{ds(on)}$) to I_{DSS} . Most of the devices will be within $\pm 10\%$ of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

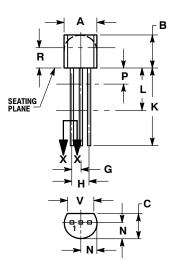
For example:

Unknown

 $r_{ds(on)}$ and V_{GS} range for an MPF4392 The electrical characteristics table indicates that an MPF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10 shows $r_{ds(on)}$ = 52 Ω for I_{DSS} = 25 mA and 30 Ω for I_{DSS} 75 mA. The corresponding V_{GS} values are 2.2 V and 4.8 V.

PACKAGE DIMENSIONS

TO-92 (TO-226) CASE 29-11 ISSUE AM



STRAIGHT LEAD **BULK PACK**



BENT LEAD

TAPE & REEL

AMMO PACK

NOTES

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- CONTOUR OF PACKAGE BEYOND DIMENSION R
 IS UNCONTROLLED.
- LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

		INCHES		MILLIMETERS		
L	DIM	MIN	MAX	MIN	MAX	
I	A	0.175	0.205	4.45	5.20	
	В	0.170	0.210	4.32	5.33	
ĺ	C	0.125	0.165	3.18	4.19	
1	D	0.016	0.021	0.407	0.533	
I	G	0.045	0.055	1.15	1.39	
I	н	0.095	0.105	2.42	2.66	
	J	0.015	0.020	0.39	0.50	
I	K	0.500		12.70		
I	٢	0.250		6.35		
I	N	0.080	0.105	2.04	2.66	
I	P		0.100		2.54	
	R	0.115		2.93	-2-	
ľ	W	0.105	- 0	2.42		

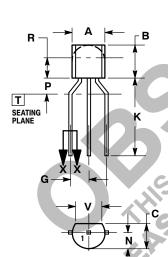
STYLE 5:

DRAIN PIN 1

SOURCE

3. GATE

- NOTES: 1. DI DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
 CONTOUR OF PACKAGE BEYOND
- DIMENSION R IS UNCONTROLLED. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM
 - **MILLIMETERS** DIM MIN MAX Α 4.45 5.20 В 4.32 5.33 3.18 4.19 D 0.40 0.54 G 2.40 2.80 0.39 0.50 12.70 N 2.04 2.66 Ρ 1.50 4.00 R 2.93



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