

### DESCRIPTION

The MP5007 is a protection device designed to protect circuitry on the output (source) from transients on input ( $V_{CC}$ ). It also protects  $V_{CC}$  from undesired shorts and transients coming from the source.

At start up, inrush current is limited by limiting the slew rate at the source. The slew rate is controlled by a small capacitor at the dv/dt pin. The dv/dt pin has an internal circuit that allows the customer to float this pin and still receives a 1.1ms ramp time at the source.

The max load at the output (source) is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor from the I-Limit pin to the Source pin.

An internal charge pump drives the gate of the power device, allowing a very low on-resistance DMOS power FET of just 37m $\Omega$ .

The source is protected from the  $V_{CC}$  input being too low or too high. Under Voltage Lockout (UVLO) assures that  $V_{CC}$  is above the minimum operating threshold, before the power device is turned on. If  $V_{CC}$  goes above the high output threshold, the source voltage will be limited.

### FEATURES

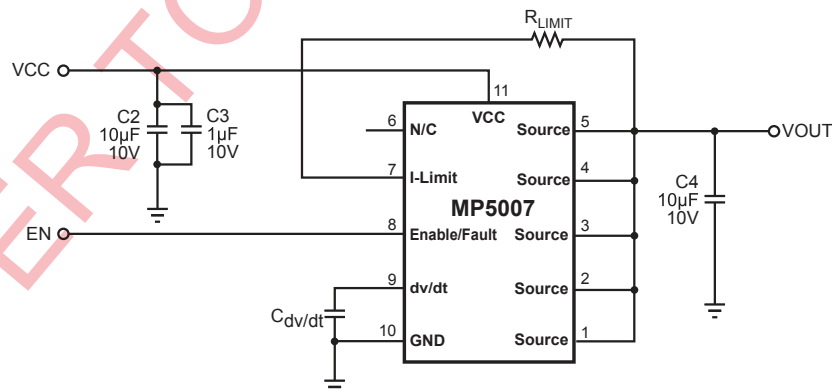
- Integrated 37m $\Omega$  Power FET
- Enable/Fault Pin
- Adjustable Slew Rate for Output Voltage
- Adjustable Current Limit
- Thermal Protection
- Over Voltage Limit
- Available in 3x3mm QFN10 Package

### APPLICATIONS

- Hot Swap
- PC Cards
- Cell Phones
- Laptops

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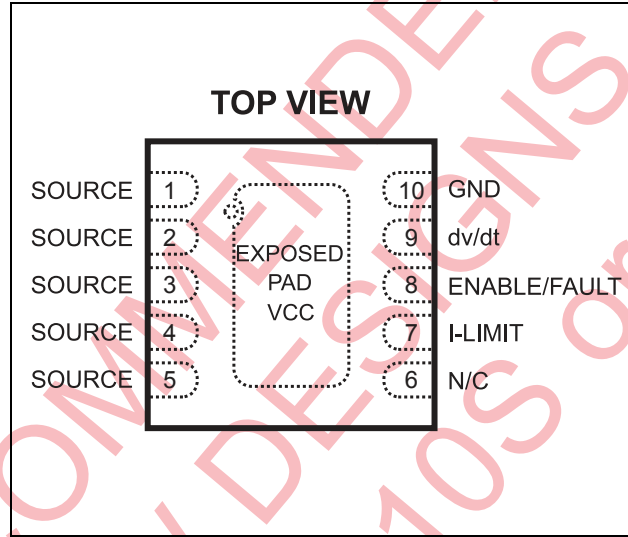
### TYPICAL APPLICATION



**ORDERING INFORMATION**

Part Number*	Package	Top Marking	Free Air Temperature (T <sub>A</sub> )
MP5007DQ	QFN10 (3x3)	3R	-40°C to +85°C

\* For Tape & Reel, add suffix -Z (e.g. MP5007DQ-Z);  
 For RoHS Compliant Packaging, add suffix -LF (e.g. MP5007DQ-LF-Z)

**PACKAGE REFERENCE**

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

VCC, SOURCE, I-LIMIT..... -0.3V to 22V  
 dv/dt, ENABLE/FAULT..... -0.3V to 6V  
 Continuous Power Dissipation (T<sub>A</sub> = +25°C)<sup>(2)</sup>  
 .....2.5W  
 Storage Temperature..... -65°C to +155°C

**Recommended Operating Conditions**

VCC Operating Range..... 4V to 6V  
 Operating Junct. Temp. (T<sub>J</sub>)..... -40°C to +125°C

**Thermal Resistance** <sup>(3)</sup>       $\theta_{JA}$        $\theta_{JC}$   
 QFN10..... 50 ..... 12 ... °C/W

**Notes:**

- Exceeding these ratings may damage the device
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub>(MAX)=(T<sub>J</sub>(MAX)-T<sub>A</sub>)/  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage...
- Measured on JESD51-7 4-layer board.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$ ,  $R_{LIMIT}=22\Omega$ ,  $C_{OUT}= 10\mu F$ ,  $T_J=25^\circ C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Power FET</b>						
Delay Time	$t_{DLY}$	Enabling of chip to $I_D=100mA$ with a $12\Omega$ resistive load		0.2		ms
ON Resistance	$R_{DSon}$	$T_J=25^\circ C$		37	43	m $\Omega$
		$T_J=80^\circ C$ , Note 4		45		
Off State Output Voltage	$V_{OFF}$	$V_{CC}=18V$ , Enable=0V, $R_L=500\Omega$			120	mV
Continuous Current	$I_D$	$0.5\text{ in}^2$ pad, $T_J=25^\circ C$		4.2		A
		minimum copper, $T_J=80^\circ C$		2.3		
<b>Thermal Latch</b>						
Shutdown Temperature	$T_{SD}$	Note 4		175		$^\circ C$
<b>Under/Over Voltage Protection</b>						
Output Clamping Voltage	$V_{CLAMP}$	Overvoltage Protection $V_{CC}=8V$	5.95	6.65	7.35	V
Under Voltage Lockout	$V_{UVLO}$	Turn on, Voltage going high	3.2	3.6	4.0	V
Under Voltage Lockout (UVLO) Hysteresis	$V_{HYST}$			0.4		V
<b>Current Limit</b>						
Hold Current	$I_{LIM-SS}$	$R_{LIMIT}=22\Omega$ , $0\Omega$ short resistance, Note 4	1.5	2.1	2.8	A
Trip Current	$I_{LIM-OL}$	$R_{LIMIT}=22\Omega$ , Note 4		3.3		A
<b>dv/dt Circuit</b>						
Rise Time	$T_r$	Float dv/dt pin, Note 5	0.64	1.1	2.0	ms
<b>Enable/Fault</b>						
Low Level Input Voltage	$V_{IL}$	Output Disabled,			0.5	V
Intermediate Level Input Voltage	$V_{I(INT)}$	Thermal Fault, Output Disabled	0.82	1.6	2.0	V
High Level Input Voltage	$V_{IH}$	Output Enabled	2.5			V
High State Maximum Voltage	$V_{I(MAX)}$			4.8		V
Low Level Input Current (Sink)	$I_{IL}$	$V_{ENABLE}=0V$		-28	-50	$\mu A$
Maximum Fanout for Fault Signal		Total number of chips that can be connected for simultaneous shutdown			3	Units
Maximum Voltage on Enable Pin	$V_{MAX}$	Note 6			$V_{CC}$	V
<b>Total Device</b>						
Bias Current	$I_{BIAS}$	Device Operational		2	3	mA
		Thermal Shutdown		1.3		
Minimum Operating Voltage for UVLO	$V_{MIN}$	Enable<0.5V			3.0	V

**Notes:**

- 4) Guaranteed by design.
- 5) Measured from 10% to 90%.
- 6) Maximum Input Voltage on Enable pin to be  $\leq 6.0V$  if  $V_{CC} \geq 6.0V$ . Maximum Input Voltage on Enable pin to be  $V_{CC}$  if  $V_{CC} \leq 6.0V$ .

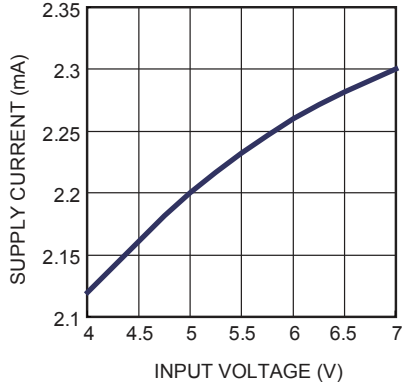
**PIN FUNCTIONS**

Pin #	Name	Description
1-5	SOURCE	This pin is the source of the internal power FET and the output terminal of the IC.
6	N/C	DO NOT CONNECT, The pin must be float.
7	I-Limit	A resistor between this pin and the Source pin sets the overload and short circuit current limit levels.
8	Enable/Fault	The Enable/Fault pin is a tri-state, bi-directional interface. It can be used to enable the output of the device by floating the pin, or disable the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over the period of 1.1ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left float.
10	GND	Negative Input Voltage to the Device. This is used as the internal reference for the IC.
11	VCC	Positive input voltage to the device (Exposed Pad).

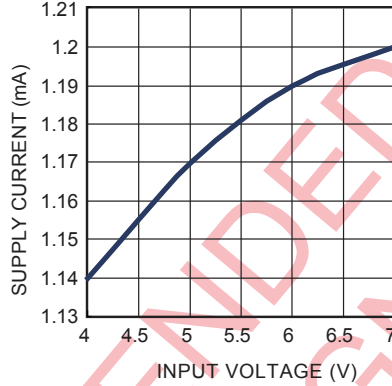
**TYPICAL PERFORMANCE CHARACTERISTICS**

$V_{CC} = 5V$ ,  $R_{LIMIT}=22\Omega$ ,  $C_{OUT}=10\mu F$ ,  $C_{dv}/dt=1nF$ ,  $T_A=25^\circ C$ , unless otherwise noted.

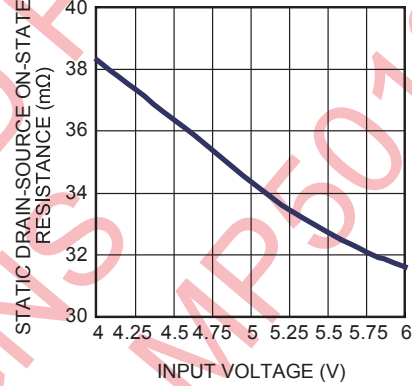
**Supply Current, Output Enabled vs. Input Voltage**



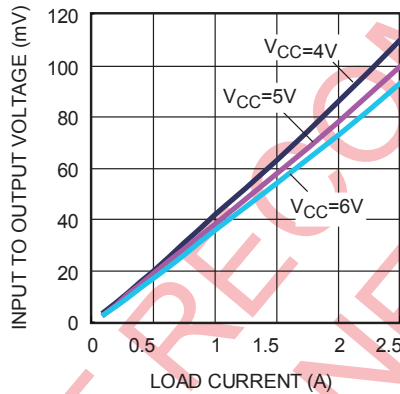
**Supply Current, Output Disabled vs. Input Voltage**  
 $V_{EN}=0V$



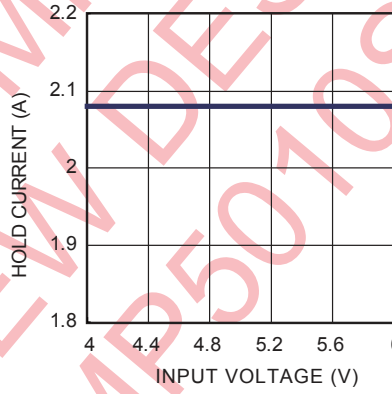
**Static Drain-Source On-State Resistance vs. Input Voltage**  
 $I_{OUT}=0.5A$



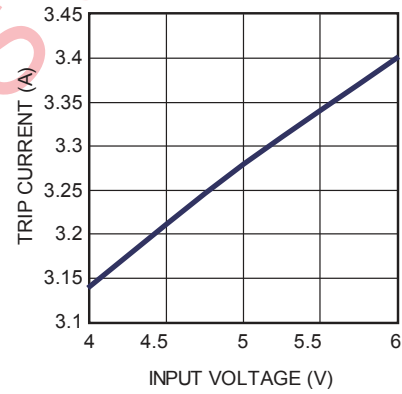
**Input to Output Voltage vs. Load Current**



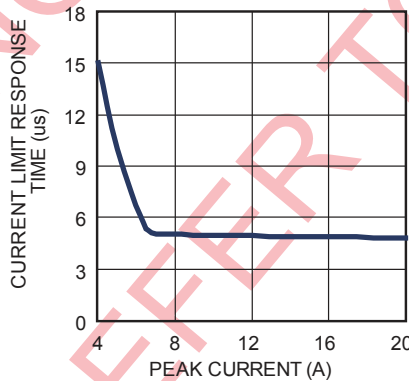
**Short Circuit Output Current vs. Input Voltage**



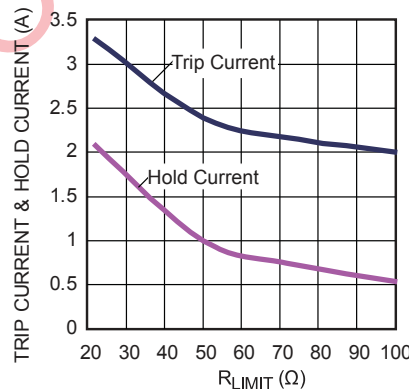
**Trip Current vs. Input Voltage**



**Current Limit Response vs. Peak Current**  
no  $C_{OUT}$



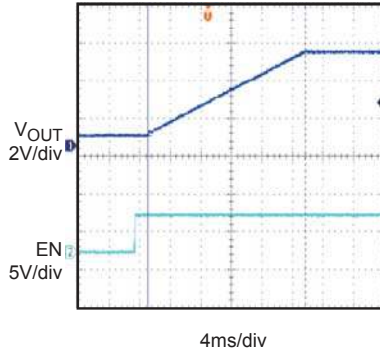
**Trip Current & Hold Current vs. R<sub>LIMIT</sub>**



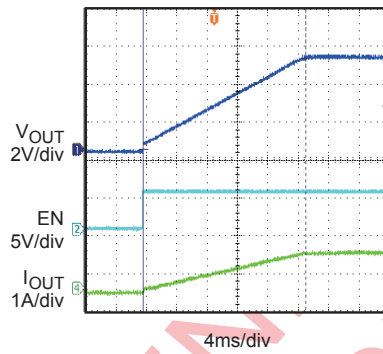
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{CC} = 5V$ ,  $R_{LIMIT} = 22\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{dv/dt} = 1nF$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

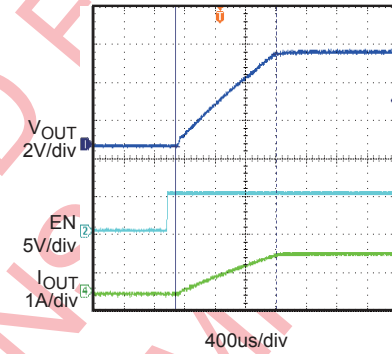
**Turn on Delay and Rise Time**  
 $I_{OUT} = 0A$



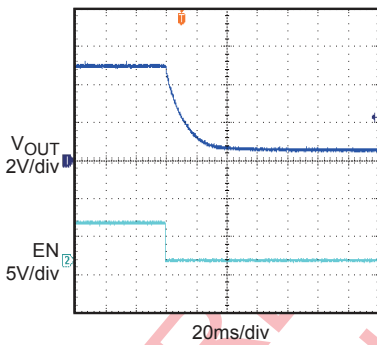
**Turn on Delay and Rise Time**  
 $I_{OUT} = 1A$



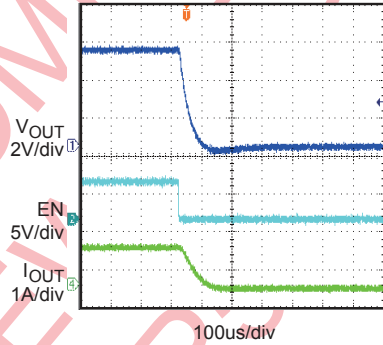
**Turn on Delay and Rise Time**  
 $I_{OUT} = 1A$ , no  $C_{dv/dt}$



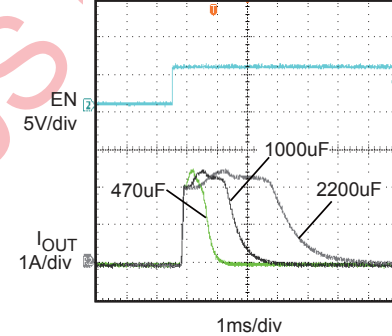
**Turn off Delay and Fall Time**  
 $I_{OUT} = 0A$



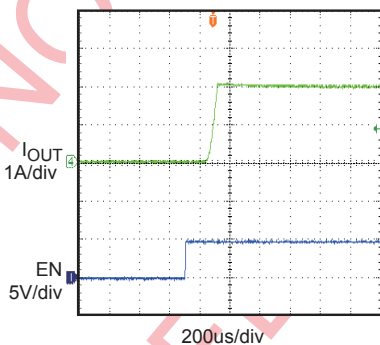
**Turn off Delay and Fall Time**  
 $I_{OUT} = 1A$



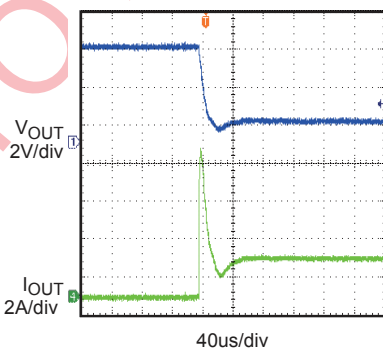
**Inrush Current with Different Load Capacitance**  
no  $C_{dv/dt}$



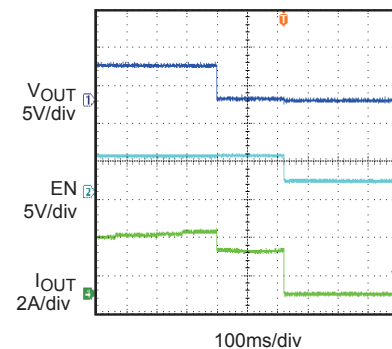
**Short Circuit Current, Device Enabled into Short**



**0.33Ω Load Connected to Enabled Device**



**Trip Current with Ramped Load and Thermal shutdown**



BLOCK DIAGRAM

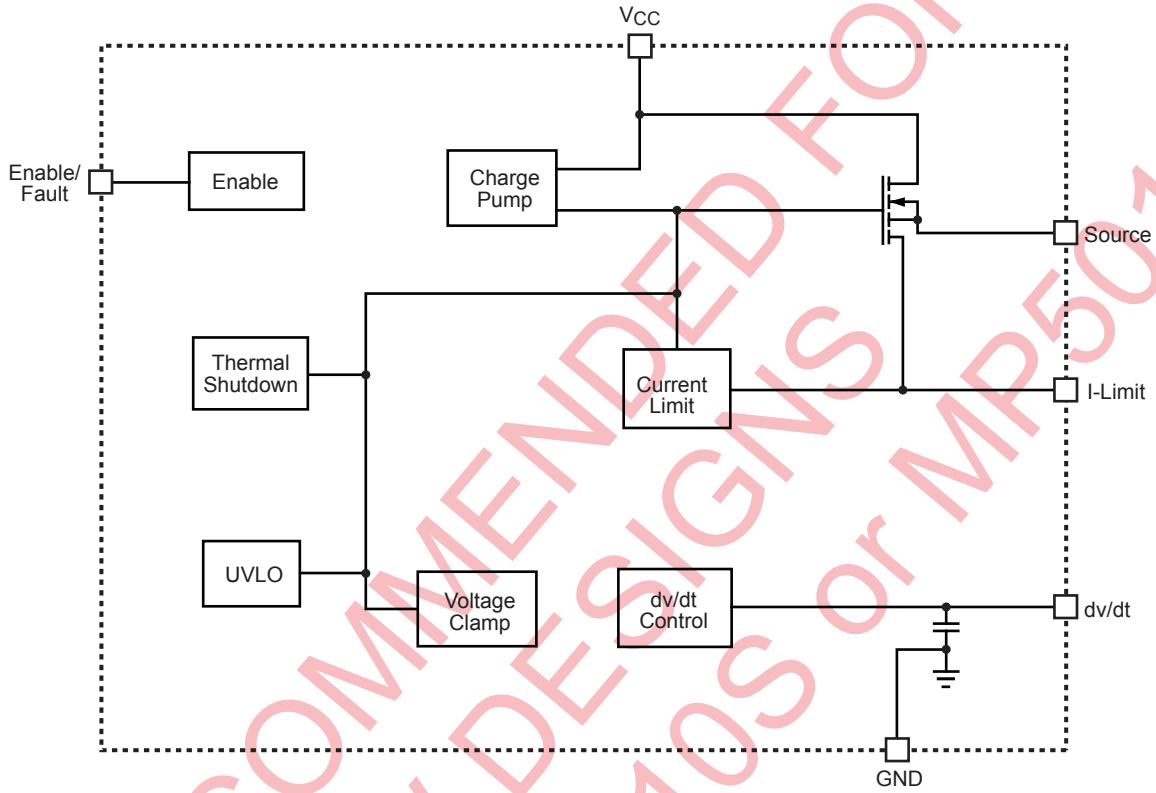


Figure 1 — Functional Block Diagram

## DETAILED DESCRIPTION

### Current Limit

The desired current limit is a function of the external current limit resistor.

**Table1 — Current Limit vs. Current Limit Resistor (V<sub>CC</sub>=5V)**

Current Limit Resistor(Ω)	22	50	75	100
Trip Current(A)	3.3	2.4	2.1	2
Hold Current(A)	2.1	1	0.7	0.6

When the part is active, if load reaches trip current (minimum threshold current triggering overcurrent protection) or a short is present, the part switches into to a constant-current (hold current) mode. Part will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

However, when the part is powered up by V<sub>CC</sub> or EN, the load current should be smaller than hold current. Otherwise, the part can't be fully turned on.

In a typical application using a current limit resistor of 22Ω, the trip current will be 3.3A and the hold current will be 2.1A. If the device is in its normal operating state and passing 2.0A it will need to dissipate only 148mW with the very low on resistance of 37mΩ. For the package dissipation of 50°C/Watt, the temperature rise will only be + 7.4°C. Combined with a 25°C ambient, this is only 32.4°C total package temperature.

During a short circuit condition, the device has 5V across it and the hold current clamps at 2.1A and therefore must dissipate 10.5W. At 50°C/watt, if uncontrolled, the temperature would rise above the MP5007 thermal protection (+175°C) and the device will be shutdown.

Proper heat sink must be used if the device is intended to supply the hold current and not shutdown. Without a heat sink, hold current should be maintained below 600mA at +25°C and below 360mA at +85°C to prevent the device from activating the thermal shutdown feature.

### Rise Time

The rise time is a function of the capacitor (Cdv/dt) on the dv/dt pin.

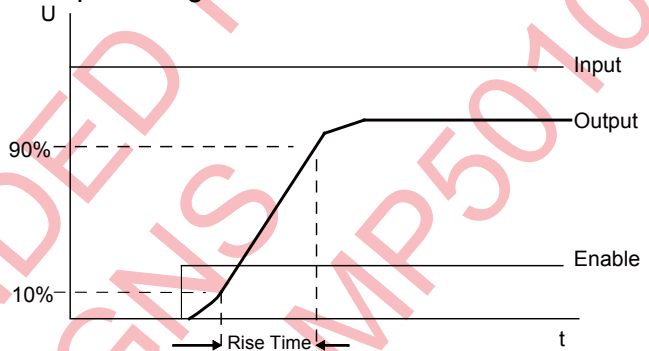
**Table2 — Rise Time\* vs. Cdv/dt**

Cdv/dt	none	50pF	500pF	1nF
Rise Time (ms)	1.1	2.2	12.3	23.5

Rise Time (TYPICAL) (ms)	1.1	2.2	12.3	23.5
* Notes: Rise Time = KRT*(50pF+Cdv/dt), KRT =22E6				

\* Notes: Rise Time = KRT\*(50pF+Cdv/dt), KRT =22E6

The “rise time” is measured by from 10% to 90% of output voltage.



**Figure2 — Rise Time**

### Fault and Enable Pin

The Enable/Fault Pin is a Bi-Directional three levels I/O with a weak pull up current (28uA typical). The three levels are low, mid and high. It functions to enable/disable the part and to indicate Fault information.

Enable pin as an input:

1. Low and mid disable the part.
2. Low, in addition to disabling the part, clears the fault flag.
3. High enables the part (if the fault flag is clear).

Enable pin as an output:

1. The pull up current may (if not overridden) allow a “wired nor” pull up to enable the part.
2. An under voltage will cause a low on the enable pin, and will clear the fault flag.
3. A thermal fault will cause a mid level on the enable pin, and will set the fault flag.



The Enable/Fault line must be above the mid level for the output to be turned on.

The fault flag is a internal flip-flop that can be set or reset under various conditions:

1. Thermal Shutdown: set fault flag
2. Under Voltage: reset fault flag
3. Low voltage on Enable/Fault pin: reset fault flag
4. Mid voltage on Enable/Fault pin: no effect

Under a fault, the Enable/Fault pin is driven to the mid level.

There are 4 types of faults, and each fault has a direct and indirect effect on the Enable/Fault pin and the internal fault flag. In a typical application there are one or more of the MP5007 chips in a system. The Enable/Fault lines will typically be connected together.

**Table3 — Fault Function Influence in Application**

Fault description	Internal action	Effect on Fault Pin	Effect on Flag	Effect on secondary Part
Short/over current	Limit current	none	none	none
Under Voltage	Output is turned off	Internally drives Enable/Fault pin to Logic low	Flag is reset	Secondary part output is disabled, and fault flag is reset.
Over Voltage	Limit output voltage	None	None	None
Thermal Shutdown	Shutdown part. The part is latched off until a UVLO or externally driven to ground.	Internally drives Enable/Fault pin to mid level	Flag is Set	Secondary part output is disabled.

**Under Voltage Lock Out Operation**

If the supply (input) is below the UVLO threshold, the output is disabled, and the fault line is driven low.

When the supply goes above the UVLO threshold, the output is enabled and the fault line is released. When the fault line is released, EN will be pulled high by a 28uA current source. No external pull up resistor is required. In addition, the pull up voltage is limited to 5 volts.

**Thermal Protection**

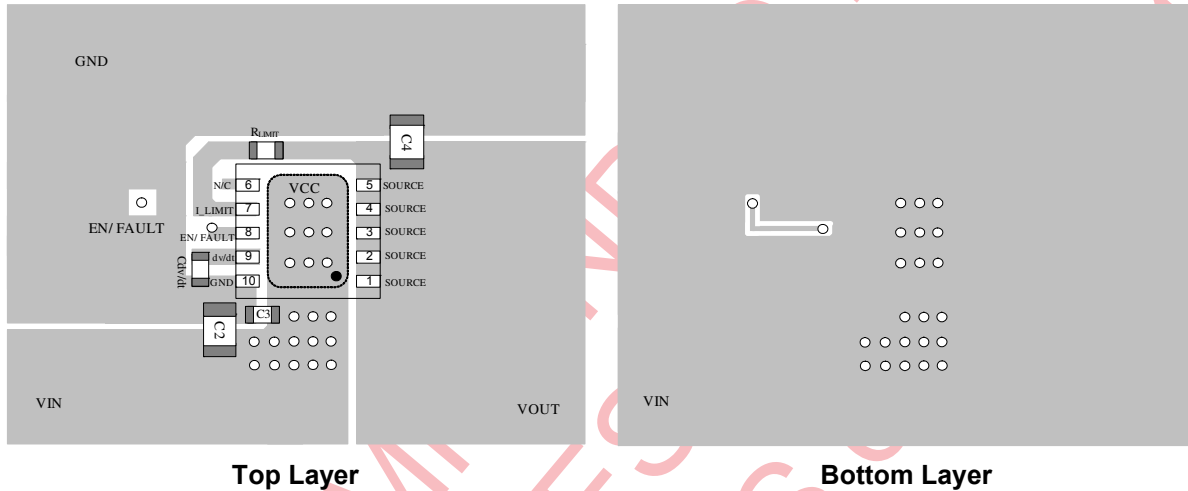
When thermal protection is triggered, the output is disabled and the fault line is driven to the mid level. The thermal fault condition is latched (meaning the fault flag is set), and the part will remain latched off until the fault (enable) line is brought low. Cycling the power below the UVLO threshold will also reset the fault flag.

**PCB Layout**

PCB layout is very important to achieve stable operation. Please follow these guidelines and take below figure for reference.

Place R<sub>limit</sub> close to I<sub>limit</sub> pin, C<sub>dv/dt</sub> close to

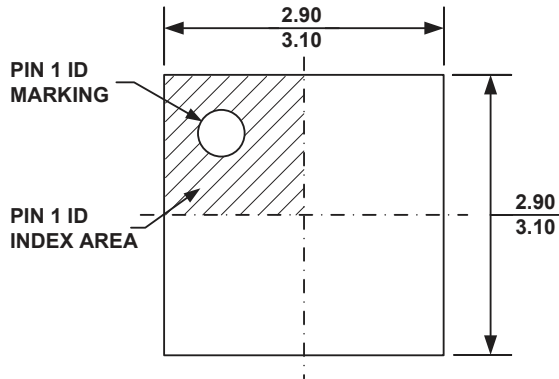
dv/dt pin and input cap close to V<sub>cc</sub>. Keep the N/C pin float. Put vias in thermal pad and ensure enough copper area near V<sub>cc</sub> and source to achieve better thermal performance.



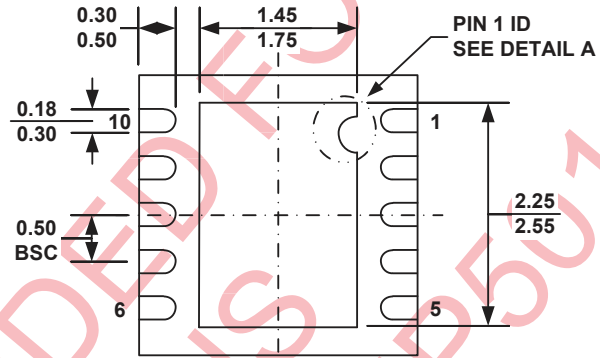
**Figure3 — PCB Layout**

**PACKAGE INFORMATION**

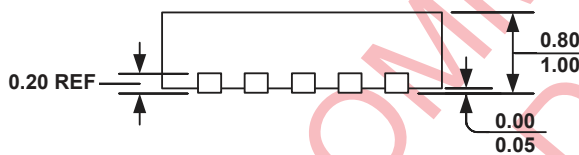
**QFN10 (3mm X 3mm)**



**TOP VIEW**



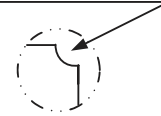
**BOTTOM VIEW**



**SIDE VIEW**

**PIN 1 ID OPTION A  
R0.20 TYP.**

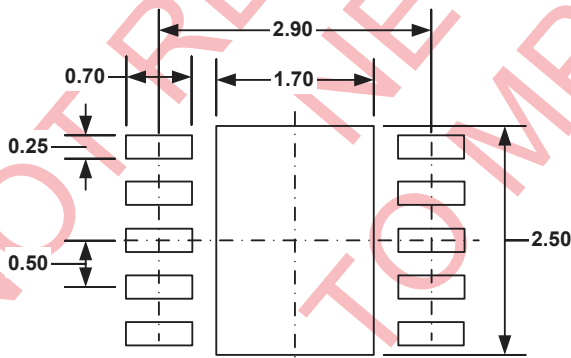
**PIN 1 ID OPTION B  
R0.20 TYP.**



**DETAIL A**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
- 5) DRAWING IS NOT TO SCALE.



**RECOMMENDED LAND PATTERN**

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