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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET



MOS FIELD EFFECT TRANSISTOR Phase-out/Discontinued 2SK3111

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3111 is N channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter, actuator driver.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3111	TO-220AB
2SK3111-S	TO-262
2SK3111-ZJ	TO-263

FEATURES

- Gate voltage rating ±30 V
- Low on-state resistance
 - $R_{DS(on)} = 180 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 10 \text{ A})$
- Low input capacitance

 $C_{iss} = 1000 \text{ pF TYP}. (V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V})$

- Avalanche capability rated
- Built-in gate protection diode
- Surface mount device available

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to source voltage ($V_{GS} = 0 V$)	VDSS	200	V
Gate to source voltage ($V_{DS} = 0 V$)	Vgss	±30	V
Drain current (DC) (Tc = 25 °C)	D(DC)	±20	А
Drain current (pulse) ^{Note1}	D(pulse)	±60	А
Total power dissipation ($T_A = 25 \ ^{\circ}C$)	P T1	1.5	W
Total power dissipation (Tc = 25 °C)	P _{T2}	65	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C
Single avalanche current Note2	las	20	А
Single avalanche energy Note2	Eas	100	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

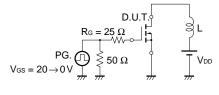
2. Starting $T_{ch} = 25 \text{ °C}$, $V_{DD} = 100 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

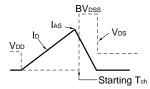
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ELECTRICAL CHARACTERISTICS (TA = 25 °C)

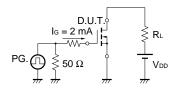
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain Leakage Current	IDSS	VDS = 200 V, VGS = 0 V			100	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 30 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	VDS = 10 V, ID = 1 mA	2.5		4.5	V
Forward Transfer Admittance	yfs	Vds = 10 V, Id = 10 A	3.0			S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, Id = 10 A		120	180	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		1000		pF
Output Capacitance	Coss	Vgs = 0 V		300		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		150		pF
Turn-on Delay Time	td(on)	VDD = 100 V		25		ns
Rise Time	tr	ID = 10 A		90		ns
Turn-off Delay Time	td(off)	$V_{GS(on)} = 10 V$		80		ns
Fall Time	tr	Rg = 10 Ω		40		ns
Total Gate Charge	QG	Vdd = 160 V		40		nC
Gate to Source Charge	QGS	Vgs = 10 V		7		nC
Gate to Drain Charge	Qgd	ID = 20 A		25		nC
Diode Forward Voltage	VF(S-D)	IF = 20 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 20 A, VGS = 0 V		300		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/ μ s		1.7		μC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

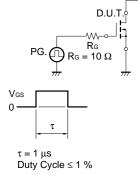


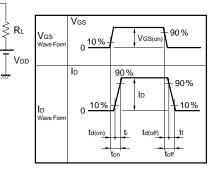


TEST CIRCUIT 3 GATE CHARGE



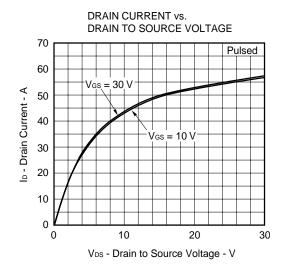
TEST CIRCUIT 2 SWITCHING TIME



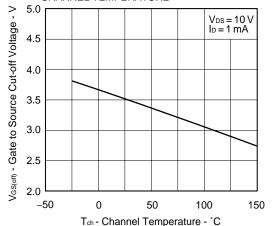


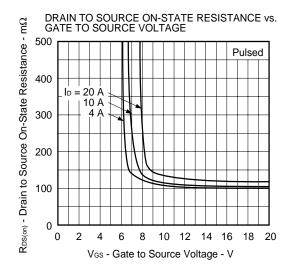
Phase-out/Discontinued

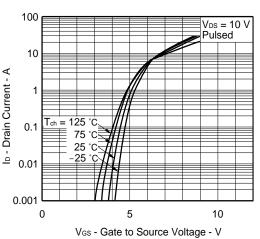
TYPICAL CHARACTERISTICS (TA = 25°C)



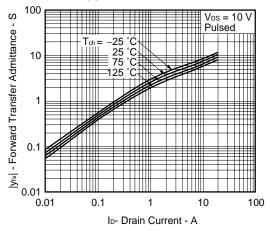


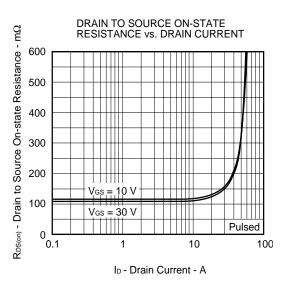






FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



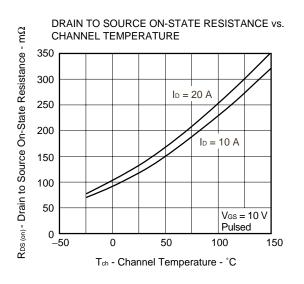


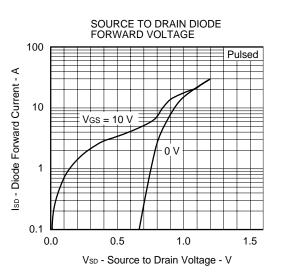
Data Sheet D13334EJ2V0DS

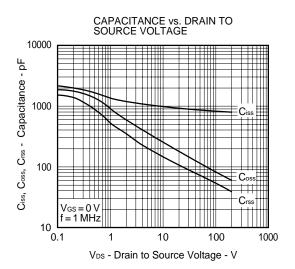
FORWARD TRANSFER CHARACTERISTICS

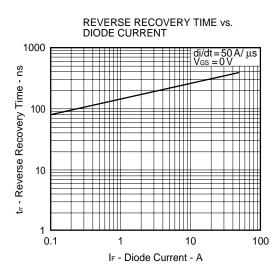
NEC



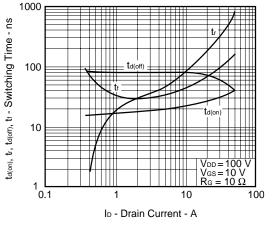


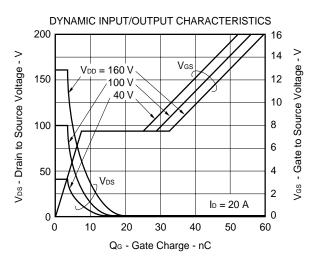




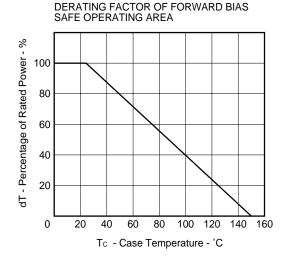


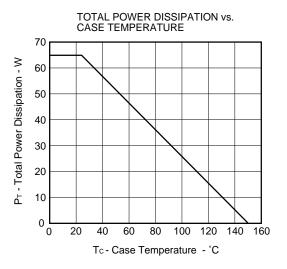
SWITCHING CHARACTERISTICS





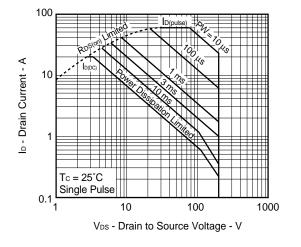
Phase-out/Discontinued



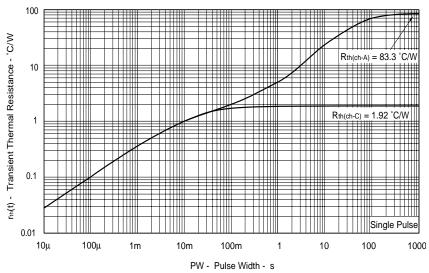


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FORWARD BIAS SAFE OPERATING AREA



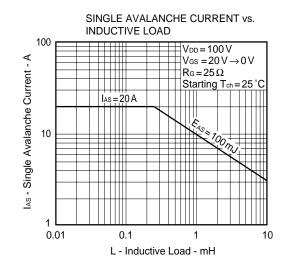


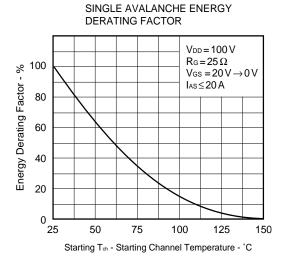


Data Sheet D13334EJ2V0DS

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Phase-out/Discontinued

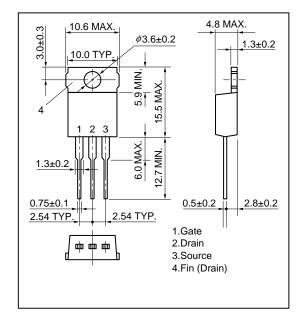




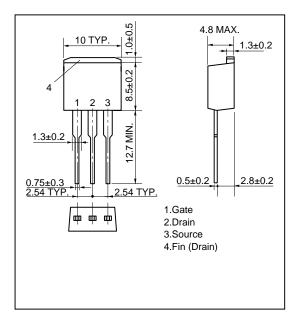
Data Sheet D13334EJ2V0DS

* PACKAGE DRAWINGS (Unit : mm)

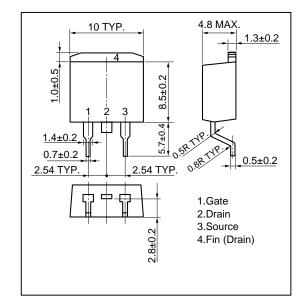
1)TO-220AB (MP-25)



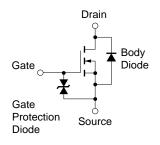
2)TO-262 (MP-25 Fin Cut)



3)TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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