



# 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

## ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)

V+ .....-0.3V to +4V

AD0, SDA, SCL.....-0.3V to +5.5V

All Other Pins.....-0.3V to (V+ + 0.3V)

Current

V+ .....200mA

GND .....-200mA

PHASE1, PHASE2, PORT0, PORT1, PUMP .....±150mA

VFCLK, VFDOOUT, VFLOAD, VFBLANK .....±150mA

SDA .....15mA

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )

16-Pin QSOP (derate at 8.34mW/°C above +70°C).....667mW

Operating Temperature Range ( $T_{\text{MIN}}$ ,  $T_{\text{MAX}}$ )

MAX6853AEE.....-40°C to +125°C

Junction Temperature .....+150°C

Storage Temperature Range .....-65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(Typical operating circuit,  $V_+ = 2.7\text{V}$  to  $3.6\text{V}$ ,  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$ , unless otherwise noted.) (Note 1)

| PARAMETER                                        | SYMBOL                            | CONDITIONS                                                                                                                            | MIN                                        | TYP | MAX    | UNITS         |
|--------------------------------------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|-----|--------|---------------|
| Operating Supply Voltage                         | V+                                |                                                                                                                                       | 2.7                                        |     | 3.6    | V             |
| Shutdown Supply Current                          | I <sub>SHDN</sub>                 | Shutdown mode, all digital inputs at V+ or GND                                                                                        | $T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$ |     | 160    | $\mu\text{A}$ |
|                                                  |                                   |                                                                                                                                       | $T_A = +25^\circ\text{C}$                  |     | 9 20   |               |
| Operating Supply Current                         | I+                                | OSC = 4MHz<br>VFLOAD, VFDOOUT, VFCLK,<br>VFBLANK, loaded 100pF                                                                        | $T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$ |     | 3      | mA            |
|                                                  |                                   |                                                                                                                                       | $T_A = +25^\circ\text{C}$                  |     | 1.65 2 |               |
| Master Clock Frequency (OSC Internal Oscillator) | f <sub>OSC</sub>                  | OSC1 fitted with C <sub>OSC</sub> = 56pF, OSC2 fitted with R <sub>OSC</sub> = 10k $\Omega$ ; see the <i>Typical Operating Circuit</i> |                                            | 4   |        | MHz           |
| Master Clock Frequency (OSC External Oscillator) |                                   | OSC1 overdriven with external f <sub>OSC</sub>                                                                                        | 2                                          |     | 8      | MHz           |
| Dead-Clock Protection Frequency                  |                                   |                                                                                                                                       |                                            | 200 |        | kHz           |
| OSC High Time                                    | t <sub>CH</sub>                   |                                                                                                                                       | 50                                         |     |        | ns            |
| OSC Low Time                                     | t <sub>CL</sub>                   |                                                                                                                                       | 50                                         |     |        | ns            |
| Fast or Slow Segment Blink Duty Cycle            |                                   | (Note 2)                                                                                                                              | 49.5                                       |     | 50.5   | %             |
| <b>LOGIC INPUTS AND OUTPUTS</b>                  |                                   |                                                                                                                                       |                                            |     |        |               |
| Input Leakage Current AD0, SDA, SCL              | I <sub>IH</sub> , I <sub>IL</sub> |                                                                                                                                       |                                            | 0.2 | 1      | $\mu\text{A}$ |
| Logic-High Input Voltage AD0, SDA, SCL           | V <sub>IH</sub>                   |                                                                                                                                       | 2.4                                        |     |        | V             |
| Logic-Low Input Voltage AD0, SDA, SCL            | V <sub>IL</sub>                   |                                                                                                                                       |                                            |     | 0.6    | V             |
| SDA Output Low Voltage                           | V <sub>OLSDA</sub>                | I <sub>SINK</sub> = 3mA                                                                                                               |                                            |     | 0.5    | V             |
| Input Capacitance                                | C <sub>I</sub>                    |                                                                                                                                       |                                            |     | 10     | pF            |

# 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

**MAX6853**

## DC ELECTRICAL CHARACTERISTICS (continued)

(Typical operating circuit, V+ = 2.7V to 3.6V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 1)

| PARAMETER                                                                                                       | SYMBOL               | CONDITIONS                                                      | MIN      | TYP                       | MAX  | UNITS |
|-----------------------------------------------------------------------------------------------------------------|----------------------|-----------------------------------------------------------------|----------|---------------------------|------|-------|
| Output Rise and Fall Time<br>PHASE1, PHASE2, PORT0,<br>PORT1, PUMP, VFLOAD,<br>VFDOUT, VFCLK, VFBLANK           | t <sub>RFT</sub>     | C <sub>LOAD</sub> = 100pF                                       |          |                           | 25   | ns    |
| Output High-Voltage<br>PHASE1, PHASE2, PORT0,<br>PORT1, PUMP, VFLOAD,<br>VFDOUT, VFCLK, VFBLANK                 | V <sub>OH</sub>      | I <sub>SOURCE</sub> = 10mA                                      | V+ - 0.6 |                           |      | V     |
| Output Low-Voltage<br>PHASE1, PHASE2, PORT0,<br>PORT1, PUMP, VFLOAD,<br>VFDOUT, VFCLK, VFBLANK                  | V <sub>OL</sub>      | I <sub>SINK</sub> = 10mA                                        |          |                           | 0.4V | V     |
| Output Short-Circuit Source<br>Current PHASE1, PHASE2,<br>PORT0, PORT1, PUMP, VFLOAD,<br>VFDOUT, VFCLK, VFBLANK | I <sub>OHSC</sub>    | Output programmed high, output short<br>circuit to GND (Note 2) |          | 62                        | 125  | mA    |
| Output Short-Circuit Sink Current<br>PHASE1, PHASE2, PORT0,<br>PORT1, PUMP, VFLOAD,<br>VFDOUT, VFCLK, VFBLANK   | I <sub>OLSC</sub>    | Output programmed low, output short<br>circuit to V+ (Note 2)   |          | 72                        | 125  | mA    |
| <b>1°C TIMING CHARACTERISTICS</b> (Figure 6)                                                                    |                      |                                                                 |          |                           |      |       |
| Serial Clock Frequency                                                                                          | f <sub>SCL</sub>     |                                                                 |          |                           | 400  | kHz   |
| Bus Free Time Between a STOP<br>and a START Condition                                                           | t <sub>BUF</sub>     |                                                                 | 1.3      |                           |      | μs    |
| Hold Time (Repeated) START<br>Condition                                                                         | t <sub>HD, STA</sub> |                                                                 | 0.6      |                           |      | μs    |
| Repeated START Condition<br>Setup Time                                                                          | t <sub>SU, STA</sub> |                                                                 | 0.6      |                           |      | μs    |
| STOP Condition Setup Time                                                                                       | t <sub>SU, STO</sub> |                                                                 | 0.6      |                           |      | μs    |
| Data Hold Time                                                                                                  | t <sub>HD, DAT</sub> | (Note 3)                                                        |          |                           | 0.9  | μs    |
| Data Setup Time                                                                                                 | t <sub>SU, DAT</sub> |                                                                 | 100      |                           |      | ns    |
| SCL Clock Low Period                                                                                            | t <sub>LOW</sub>     |                                                                 | 1.3      |                           |      | μs    |
| SCL Clock High Period                                                                                           | t <sub>HIGH</sub>    |                                                                 | 0.6      |                           |      | μs    |
| Rise Time of Both SDA and SCL<br>Signals, Receiving                                                             | t <sub>R</sub>       | (Notes 2, 4)                                                    |          | 20 +<br>0.1C <sub>B</sub> | 300  | ns    |
| Fall Time of Both SDA and SCL<br>Signals, Receiving                                                             | t <sub>F</sub>       | (Notes 2, 4)                                                    |          | 20 +<br>0.1C <sub>B</sub> | 300  | ns    |

# 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

## DC ELECTRICAL CHARACTERISTICS (continued)

(Typical operating circuit,  $V_+ = 2.7V$  to  $3.6V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.) (Note 1)

| PARAMETER                                               | SYMBOL     | CONDITIONS   | MIN | TYP              | MAX  | UNITS   |
|---------------------------------------------------------|------------|--------------|-----|------------------|------|---------|
| Fall Time of SDA Transmitting                           | $t_F$      | (Notes 2, 5) |     | 20 +<br>$0.1C_B$ | 250  | ns      |
| Pulse Width of Spike Suppressed                         | $t_{SP}$   | (Note 6)     | 0   | 50               |      | ns      |
| Capacitive Load for Each Bus Line                       | CB         | (Note 2)     |     | 400              |      | pF      |
| <b>VFD INTERFACE TIMING CHARACTERISTICS</b> (Figure 14) |            |              |     |                  |      |         |
| VFCLK Clock Period                                      | $t_{VCP}$  | (Note 2)     | 250 |                  | 1050 | ns      |
| VFCLK Pulse Width High                                  | $t_{VCH}$  | (Note 2)     | 125 |                  |      | ns      |
| VFCLK Pulse Width Low                                   | $t_{VCL}$  | (Note 2)     | 125 |                  |      | ns      |
| VFCLK Rise to VFD Load Rise Hold Time                   | $t_{VCSH}$ | (Note 2)     | 19  |                  |      | $\mu s$ |
| VFDOUT Setup Time                                       | $t_{VDS}$  | (Note 2)     | 50  |                  |      | ns      |
| VFLOAD Pulse High                                       | $t_{VCSW}$ | (Note 2)     | 245 |                  |      | ns      |

**Note 1:** All parameters tested at  $T_A = +25^\circ C$ . Specifications over temperature are guaranteed by design.

**Note 2:** Guaranteed by design.

**Note 3:** A master device must provide a hold time of at least 300ns for the SDA signal (referred to  $V_{IL}$  of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

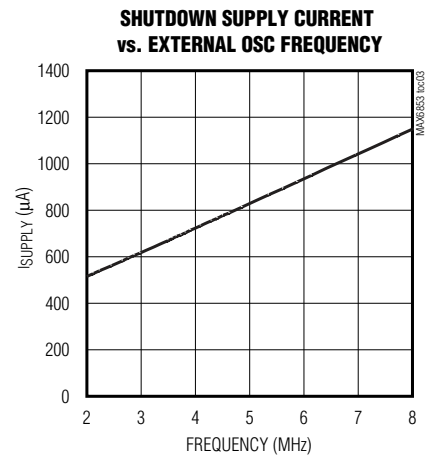
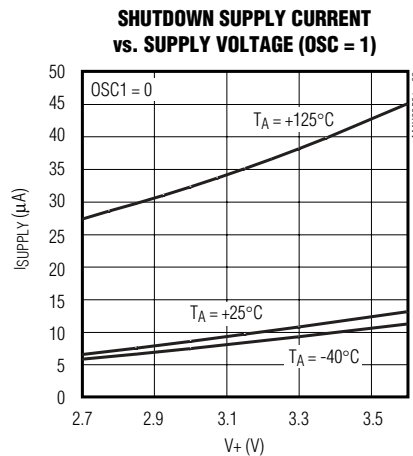
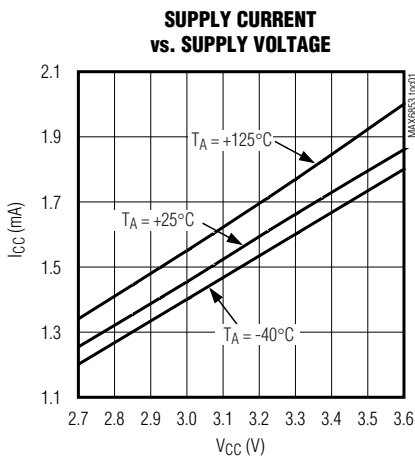
**Note 4:**  $C_B$  = total capacitance of one bus line in pF.  $t_R$  and  $t_F$  measured between  $0.3V_+$  and  $0.7V_+$ .

**Note 5:**  $I_{SINK} \leq 6mA$ .  $C_B$  = total capacitance of one bus line in pF.  $t_R$  and  $t_F$  measured between  $0.3V_+$  and  $0.7V_+$ .

**Note 6:** Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

## Typical Operating Characteristics

(Typical Operating Circuit,  $V_+ = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

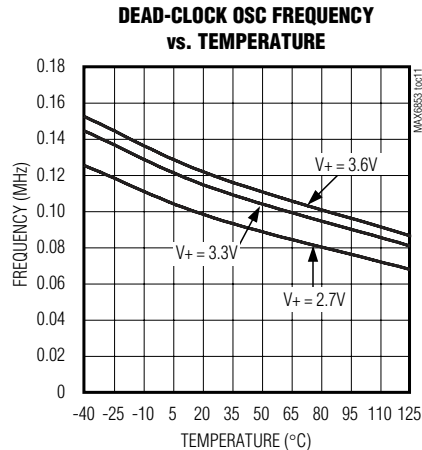
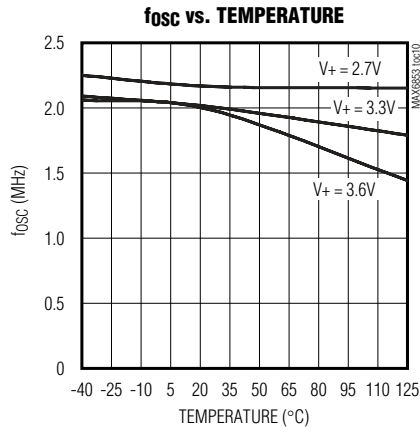
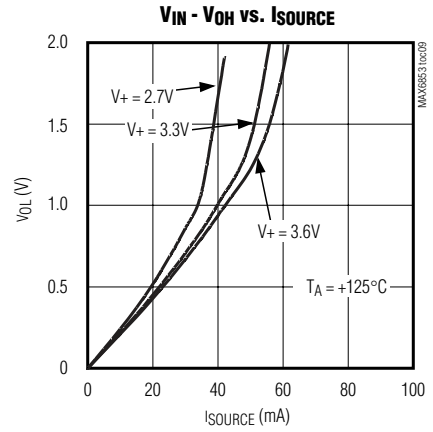
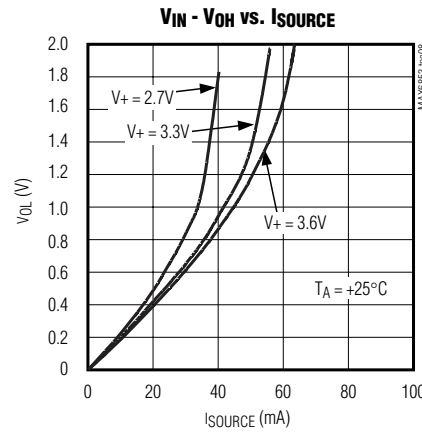
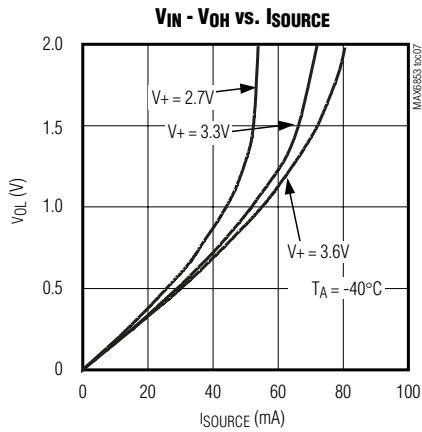
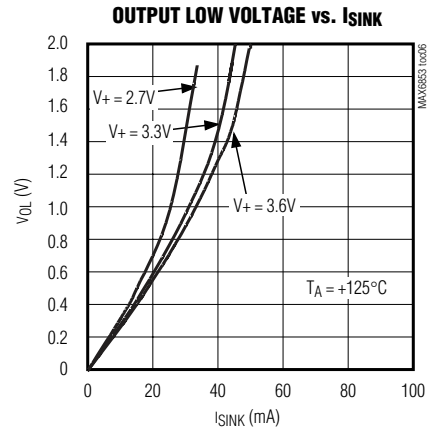
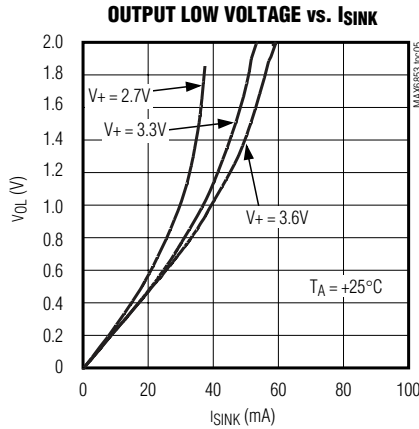
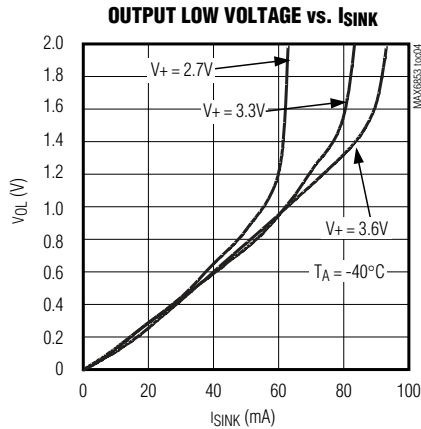


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MAX6853

## Typical Operating Characteristics (continued)

(Typical Operating Circuit,  $V_+ = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

### Pin Description

| PIN | NAME    | FUNCTION                                                                                                                                                                            |
|-----|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | VFCLK   | Serial-Clock Output to External Driver. Push-pull clock output to external display driver. On VFCLK's falling edge, data is clocked out of VFDOOUT.                                 |
| 2   | VFDOOUT | Serial-Data Output to External Driver. Push-pull data output to external display driver.                                                                                            |
| 3   | VFLOAD  | Serial-Load Output to External Driver. Push-pull load output to external display driver. Rising edge is used by external display driver to load serial data into display latch.     |
| 4   | VFBLANK | Display Blanking Output to External Driver. Push-pull blanking output to external display driver used for PWM intensity control.                                                    |
| 5   | PUMP    | PUMP General-Purpose Output. User-configurable push-pull logic output.                                                                                                              |
| 6   | PHASE1  | Filament Drive PHASE1 Output and General-Purpose Output. User-configurable push-pull logic output can also be used as a driver for external filament bridge drive.                  |
| 7   | PHASE2  | Filament Drive PHASE2 Output and General-Purpose Output. User-configurable push-pull logic output can also be used as a driver for external filament bridge drive.                  |
| 8   | V+      | Positive Supply Voltage. Bypass V+ to GND with a 0.1µF ceramic capacitor.                                                                                                           |
| 9   | GND     | Ground                                                                                                                                                                              |
| 10  | PORT0   | PORT0 General-Purpose Output. User-configurable push-pull logic output.                                                                                                             |
| 11  | SCL     | Serial-Clock Input                                                                                                                                                                  |
| 12  | SDA     | Serial-Data I/O                                                                                                                                                                     |
| 13  | AD0     | Address Input 0. Sets device slave address. Connect to either GND, V+, SCL, or SDA to give four logic combinations. See Table 7.                                                    |
| 14  | PORT1   | PORT1 General-Purpose Output. User-configurable push-pull logic output.                                                                                                             |
| 15  | OSC2    | Multiplex Clock Input 2. Connect resistor R <sub>OSC</sub> from OSC2 to GND.                                                                                                        |
| 16  | OSC1    | Multiplex Clock Input 1. To use the internal oscillator, connect capacitor C <sub>OSC</sub> from OSC1 to GND. To use the external clock, drive OSC1 with a 2MHz to 8MHz CMOS clock. |

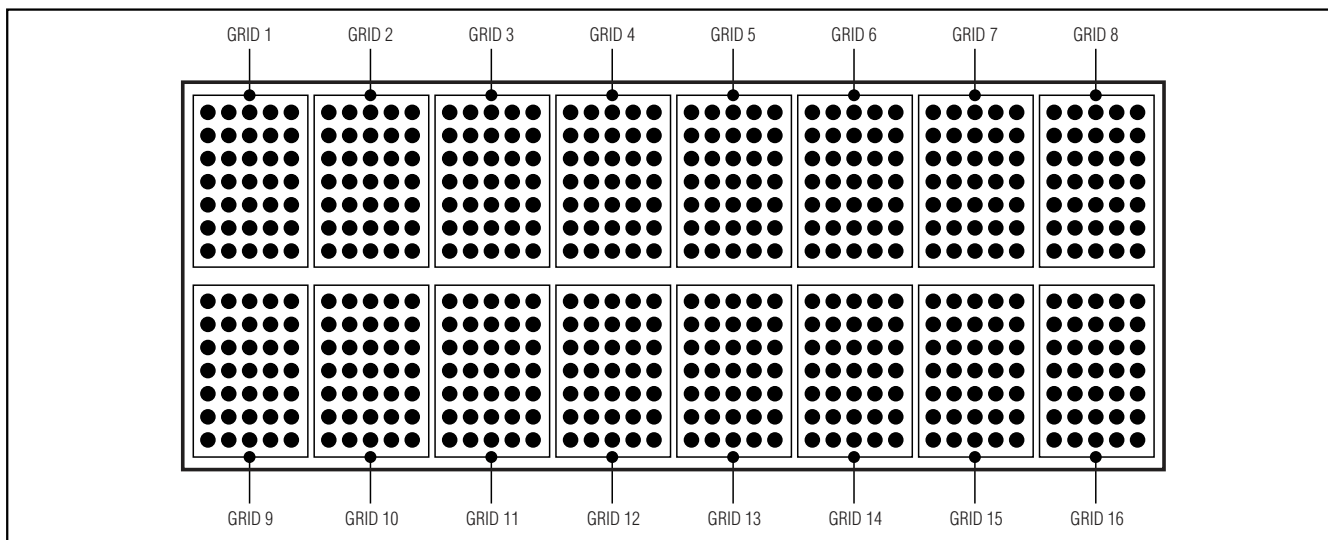


Figure 1. Example of a One-Digit-per-Grid Display

# 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

**MAX6853**

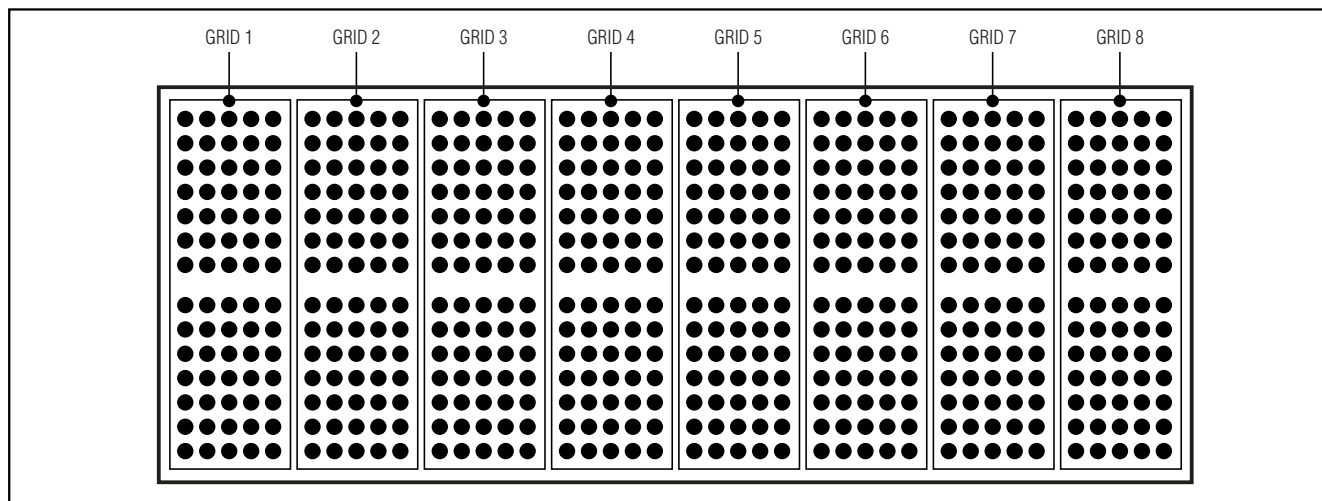


Figure 2. Example of a Two-Digits-per-Grid Display (8 Grids, 16 Digits)

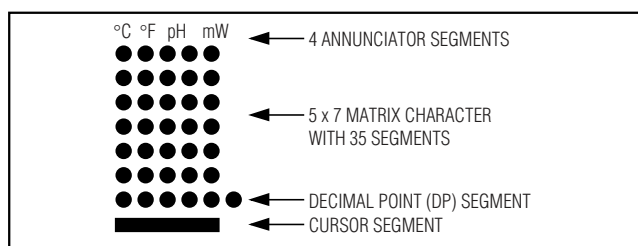


Figure 3. Digit Structure with 5 × 7 Matrix Character, DP Segment, Cursor Segment, Four Annunciators

Each digit can have a 5 × 7 matrix character, a DP segment, a cursor segment, and (for one-digit-per-grid displays only) four annunciators (Figure 3).

The 5 × 7 matrix character segments are not controlled directly, but use on-chip fonts that map the segments. The fonts comprise an ASCII 104-character fixed-font set, and 24 user-definable characters. The predefined characters follow the Arial font, with the addition of the following common symbols: £, €, ¥, °, μ, ±, ↑, and ↓. The 24 user-definable characters are uploaded by the user into on-chip RAM through the serial interface and are lost when the device is powered down. As well as custom 5 × 7 characters, the user-definable fonts can control up to 35 custom segments, bar graphs, or graphics.

Annunciator segments have individual, independent control, so any combination of annunciators can be lit. Annunciators can be off, lit, or blink either in phase or out of phase with the cursor. The blink-speed control is software selectable to be one or two blinks per second (OSC = 4MHz).

DP segments can be lit or off, but have no blink control. A DP segment is set by the same command that writes the digit's 5 × 7 matrix character.

The cursor segment is controlled differently. A single register selects one digit's cursor from the entire display, and that can be lit either continuously or blinking. All the other digits' cursors are off.

The designations of DP, cursor, and annunciator are interchangeable. For example, consider an application requiring only one DP lit at a time, but the DP needs to

## Detailed Description

### Overview of the MAX6853

The MAX6853 VFD controller generates the multiplex timing for the following VFD display types:

- Multiplexed displays with one digit per grid, and up to 48 grids (in 48/1 mode). Each grid can contain one 5 × 7 matrix character, a DP segment, a cursor segment, and four extra annunciator segments (Figure 1).
- Multiplexed displays with two digits per grid, and up to 48 grids (in 96/2 mode). Each grid can contain two 5 × 7 matrix characters, two DP segments, and two cursor segments. No annunciator segments are supported (Figure 2).

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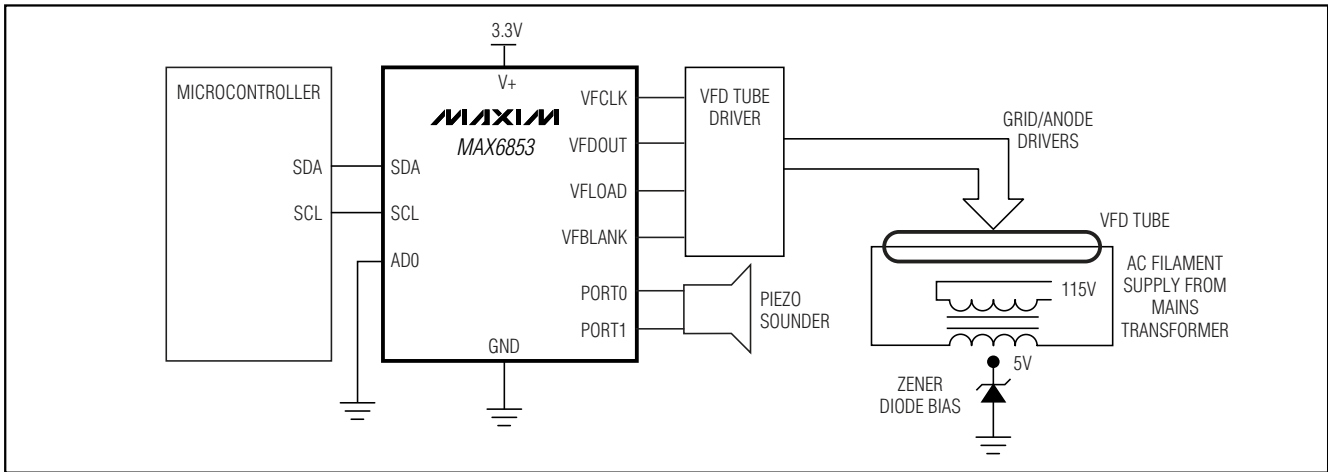


Figure 4. Connection of the MAX6853 to VFD Driver and VFD Tube

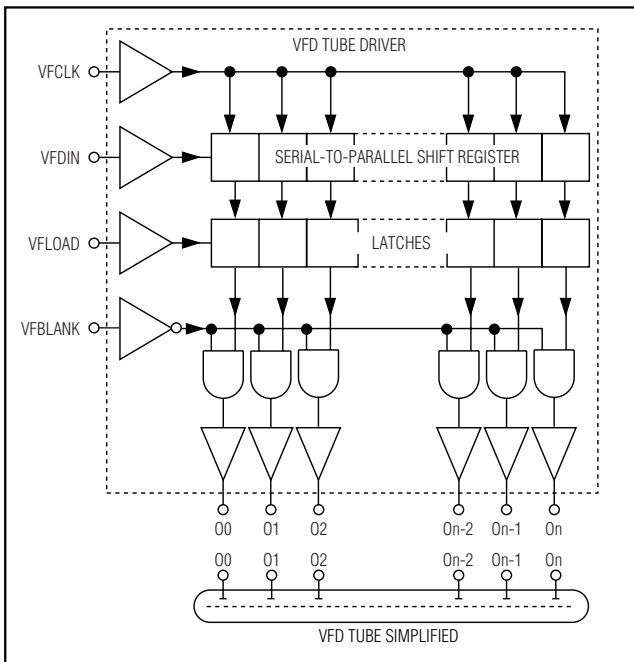


Figure 5. Block Diagram of VFD Tube Driver and VFD Tube

blink. The DP function does not have blink capability. Instead, the DP segments on the display are routed (using the output map) to the cursor function. In this case, the DP segments are controlled using the cursor register.

The output of the controller is a 4-wire serial stream that interfaces to industry-standard, shift-register, high-voltage grid/anode VFD tube drivers (Figure 4). This inter-

face uses three outputs to transfer and latch grid and anode data into the tube drivers, and a fourth output that enables/disables the tube driver outputs (Figure 5). The enable/disable control is modulated by the MAX6853 for both PWM intensity control and interdigit blanking, and disables the tube driver in shutdown. The controller multiplexes the display by enabling each grid of the VFD in turn for 100 $\mu$ s (OSC = 4MHz) with the correct segment (anode) data. The data for the next grid is transferred to the tube drivers during the display time of the current grid.

The controller uses an internal output map to match any tube-driver's shift-register grid/anode order, and is therefore compatible with all VFD internal chip-in-glass or external tube drivers.

The MAX6853 provides five high-current output ports, which can be configured for a variety of functions:

The PUMP output can be configured as either an 80kHz (OSC = 4MHz) clock intended for DC-to-DC converter use or a general-purpose logic output.

The PHASE1 and PHASE2 outputs can be individually configured as either 10kHz PWM outputs (OSC = 4MHz) intended for filament driving, blink status outputs, or general-purpose logic outputs.

The PORT0 and PORT1 outputs can be individually configured as either 625Hz, 1250Hz, or 2500Hz clocks (OSC = 4MHz) intended for buzzer driving, blink or shutdown status outputs, or general-purpose logic outputs.

## Display Modes

The MAX6853 has two display modes (Table 1), selected by the M bit in the configuration register (Table 23). The display modes trade the maximum allowable num-



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MAX6853

**Table 1. Display Modes**

| DISPLAY MODE | MAXIMUM NO. OF DIGITS                                  | MAXIMUM NO. OF ANNUNCIATORS | MAXIMUM NO. OF GRIDS | DIGITS COVERED BY EACH GRID |
|--------------|--------------------------------------------------------|-----------------------------|----------------------|-----------------------------|
| 48/1 mode    | 48 digits, each with a DP segment and a cursor segment | 4 per digit                 | 48 grids             | 1 digit per grid            |
| 96/2 mode    | 96 digits, each with a DP segment and a cursor segment | None                        |                      | 2 digits per grid           |

**Table 2. Register Address Map**

| REGISTER                                           | COMMAND ADDRESS |     |     |     |     |     |    |    | HEX CODE |
|----------------------------------------------------|-----------------|-----|-----|-----|-----|-----|----|----|----------|
|                                                    | D15             | D14 | D13 | D12 | D11 | D10 | D9 | D8 |          |
| No-op                                              | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0x00     |
| VFBLANK polarity                                   | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 0   | 0  | 1  | 0x01     |
| Intensity                                          | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 0   | 1  | 0  | 0x02     |
| Grids                                              | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 0   | 1  | 1  | 0x03     |
| Configuration                                      | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 1   | 0  | 0  | 0x04     |
| User-defined fonts                                 | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 1   | 0  | 1  | 0x05     |
| Output map                                         | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 1   | 1  | 0  | 0x06     |
| Display test and device ID                         | R/ $\bar{W}$    | 0   | 0   | 0   | 0   | 1   | 1  | 1  | 0x07     |
| PUMP register                                      | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 0   | 0  | 0  | 0x08     |
| Filament duty cycle                                | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 0   | 0  | 1  | 0x09     |
| PHASE1                                             | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 0   | 1  | 0  | 0x0A     |
| PHASE2                                             | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 0   | 1  | 1  | 0x0B     |
| PORT0                                              | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 1   | 0  | 0  | 0x0C     |
| PORT1                                              | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 1   | 0  | 1  | 0x0D     |
| Shift limit                                        | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 1   | 1  | 0  | 0x0E     |
| Cursor                                             | R/ $\bar{W}$    | 0   | 0   | 0   | 1   | 1   | 1  | 1  | 0x0F     |
| Factory reserved. <b>Do not write to register.</b> | X               | 0   | 0   | 1   | 0   | 0   | 0  | 0  | 0x10     |

ber of digits (96/2 mode) against the availability of annunciator segments (48/1 mode). Table 2 is the register address map.

### Initial Power-Up

Initial power-up resets all control registers, clears display segment and annunciator data, sets intensity to minimum, and enables shutdown. (Table 3).

### Character Registers

The MAX6853 uses 48 character registers (48/1 mode) (Table 4) or 96 character registers (96/2 mode) (Table 5) to store the 5 x 7 characters (Table 6). Each digit is represented by 1 byte of memory. The data in the character registers does not control the character segments directly. Instead, the register data is used to address a character generator, which stores the data of the 128-character font (Table 9). The lower 7 bits of the character data (D6 to D0) select a character from the font

table. The most significant bit (MSB) of the register data (D7) controls the DP segment of the digit; it is set to light the DP, cleared to leave it unlit.

The character registers address maps are shown in Table 4 (48/1 mode) and Table 5 (96/2 mode).

In 48/1 mode, the character registers use a single address range 0x20 to {0x20 + g}, where g is the value in the grids register (Table 25). The 48/1 mode upper address limit, when g is 0x2F, is therefore 0x4F. The address range 0x50 to 0x7F is used for annunciator data in 48/1 mode.

In 96/2 mode, the character registers use two address ranges. The first row's address range is 0x20 to {0x20 + g}. The second row's address range is 0x50 to {0x50 + g}. Therefore, in 96/2 mode, the character registers are only one contiguous memory range when a 48-grid display is used.

## 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

### Character Generator Font Mapping

The font is a 5 × 7 matrix comprising 104 characters in ROM, and 24 user-definable characters. The selection from the total of 128 characters is represented by the lower 7 bits of the 8-bit digit registers. The MSB, shown as x in the ROM map (Table 9), controls the DP segment of the digit; it is set to light the DP, cleared to leave it unlit.

The character map follows the Arial font for 96 characters in the x0100000 through x1111111 range. The first 32 characters map the 24 user-definable positions (RAM00 to RAM23), plus eight extra common characters in ROM.

### User-Defined Fonts

The 24 user-definable characters are represented by 120 entries of 7-bit data, five entries per character, and are stored in the MAX6853's internal RAM.

The 120 user-definable font data entries are written and read through a single register, address 0x05. An autoincrementing font address pointer in the MAX6853 indirectly accesses the font data. The font address pointer can be written, setting one of 120 addresses between 0x00 and 0xF7, but cannot be read back. The font data is written to and read from the MAX6853 indirectly, using this font address pointer. Unused font locations can be used as general-purpose scratch RAM, noting that the font registers are only 7 bits wide, not 8.

**Table 3. Initial Power-Up Register Status**

| REGISTER                          | POWER-UP CONDITION                                             | COMMAND ADDRESS | REGISTER DATA                       |    |    |    |    |    |    |    |
|-----------------------------------|----------------------------------------------------------------|-----------------|-------------------------------------|----|----|----|----|----|----|----|
|                                   |                                                                |                 | D7                                  | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| VFBLANK polarity                  | VFBLANK is high to disable the display                         | 0x01            | X                                   | X  | X  | X  | X  | X  | 0  | 0  |
| Intensity                         | 1/16 (min on)                                                  | 0x02            | X                                   | X  | X  | X  | 0  | 0  | 0  | 0  |
| Grids                             | Display has 1 grid                                             | 0x03            | X                                   | X  | 0  | 0  | 0  | 0  | 0  | 0  |
| Configuration                     | Shutdown enabled, configuration unlocked                       | 0x04            | 1                                   | 0  | 0  | 0  | X  | 0  | 0  | 0  |
| User-defined font address pointer | Address 0x80; pointing to the first user-defined font location | 0x05            | 1                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| User-defined fonts                | All 24 characters blank                                        | —               | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Output map pointer                | Pointing to first entry address                                | 0x06            | 1                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Output map data                   | Predefined for 40-digit display                                | —               | See Table 30 for power-up patterns. |    |    |    |    |    |    |    |
| Display test                      | Normal operation                                               | 0x07            | 0                                   | 0  | 0  | 0  | 0  | 1  | 1  | 0  |
| PUMP                              | General-purpose output, logic                                  | 0x08            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Filament duty cycle               | Minimum duty cycle                                             | 0x09            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| PHASE1                            | General-purpose output, logic                                  | 0x0A            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| PHASE2                            | General-purpose output, logic                                  | 0x0B            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| PORT0                             | General-purpose output, logic                                  | 0x0C            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| PORT1                             | General-purpose output, logic                                  | 0x0D            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Shift limit                       | 2 output bits                                                  | 0x0E            | X                                   | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Cursor                            | Off                                                            | 0x0F            | 0                                   | 1  | 1  | 0  | 0  | 0  | 0  | 0  |
| Character and annunciator data    | Clear                                                          | 0x20            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| <b>UP TO</b>                      | —                                                              | <b>UP TO</b>    | —                                   | —  | —  | —  | —  | —  | —  | —  |
| Character and annunciator data    | Clear                                                          | 0x7F            | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

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**Table 4. Character and Annunciator Register Address Map in 48/1 Mode**

| REGISTER                        | COMMAND ADDRESS |     |     |     |     |     |    |    | HEX CODE |
|---------------------------------|-----------------|-----|-----|-----|-----|-----|----|----|----------|
|                                 | D15             | D14 | D13 | D12 | D11 | D10 | D9 | D8 |          |
| Digit 0 5 × 7 matrix character  | 0               | 0   | 1   | 0   | 0   | 0   | 0  | 0  | 0x20     |
| Digit 1 5 × 7 matrix character  | 0               | 0   | 1   | 0   | 0   | 0   | 0  | 1  | 0x21     |
| Digit 2 5 × 7 matrix character  | 0               | 0   | 1   | 0   | 0   | 0   | 1  | 0  | 0x22     |
| <b>UP TO</b>                    | —               | —   | —   | —   | —   | —   | —  | —  | —        |
| Digit 45 5 × 7 matrix character | 0               | 1   | 0   | 0   | 1   | 1   | 0  | 1  | 0x4D     |
| Digit 46 5 × 7 matrix character | 0               | 1   | 0   | 0   | 1   | 1   | 1  | 0  | 0x4E     |
| Digit 47 5 × 7 matrix character | 0               | 1   | 0   | 0   | 1   | 1   | 1  | 1  | 0x4F     |
| Digit 0 annunciators            | 0               | 1   | 0   | 1   | 0   | 0   | 0  | 0  | 0x50     |
| Digit 1 annunciators            | 0               | 1   | 0   | 1   | 0   | 0   | 0  | 1  | 0x51     |
| Digit 2 annunciators            | 0               | 1   | 0   | 1   | 0   | 0   | 1  | 0  | 0x52     |
| <b>UP TO</b>                    | —               | —   | —   | —   | —   | —   | —  | —  | —        |
| Digit 45 annunciators           | 0               | 1   | 1   | 1   | 1   | 1   | 0  | 1  | 0x7D     |
| Digit 46 annunciators           | 0               | 1   | 1   | 1   | 1   | 1   | 1  | 0  | 0x7E     |
| Digit 47 annunciators           | 0               | 1   | 1   | 1   | 1   | 1   | 1  | 1  | 0x7F     |

Table 10 shows how to use the single user-defined font register 0x05 to set the font address pointer, write font data, and read font data. A read action always returns font data from the font address pointer position. A write action sets the 7-bit font address pointer if the MSB is set, or writes 7-bit font data to the font address pointer position if the MSB is clear.

The font address pointer autoincrements after a valid access to the user-definable font data. Auto-incrementing allows the 120-font data entries to be written and read back very quickly because the font pointer address need only be set once. After the last data location 0xF7 has been written, further font data entries are ignored until the font address pointer is reset. If the font address pointer is set to an out-of-range address by writing data in the 0xF8 to 0xFF range, then address 0x80 is set instead (Table 11).

Table 12 shows the user-definable font pointer base addresses.

Table 13 shows an example of data (characters 0, 1, and 2) being stored in the first three user-defined font locations, illustrating the orientation of the data bits.

Table 14 shows the six sequential write commands required to set a MAX6853's font character RAM02 with the data to display character 2 given in Table 9.

### Cursor Register

The cursor register controls the behavior of the cursor segments (Table 15). The MAX6853 controls 48 cursors in 48/1 mode, and 96 cursors in 96/2 mode. The cursor

register selects one digit's cursor to be lit either continuously or blinking. All the other digits' cursors are off.

The 7 least significant bits (LSBs) of the cursor register identify the cursor position. The MSB is clear for the cursor to be on continuously, and set for the cursor to be lit only during the first half of each blink period.

The valid cursor position address range is contiguous: 0 to 47 (0x00 to 0x2F) for the first digit row, and 48 to 95 (0x30 to 0x5F) for the last digit row. If the cursor register is programmed with an out-of-range value of 95 to 127 (0x60 to 0x7F), then all cursors are off.

### Annunciator Registers

The annunciator registers are organized in bytes, with each segment of each grid being represented by 2 bits. Thus, the four annunciators segments allowed for each grid are represented by exactly 1 byte (Table 16). Annunciators are only available in 48/1 mode. The annunciator address map is shown in Table 4.

### Configuration Register

The configuration register is used to enter and exit shutdown, lock the key VFD configuration settings, select the blink rate, globally clear the digit and annunciator data, reset the blink timing, and select between 48/1 and 96/2 display modes (Table 17).

### Shutdown Mode (S Data Bit D0) Format

The S bit in the configuration register selects shutdown or normal operation (Table 18). The display driver can be programmed while in shutdown mode, and shut-

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**Table 5. Character Register Address Map in 96/2 Mode**

| REGISTER                                 | COMMAND ADDRESS |     |     |     |     |     |    |    | HEX CODE |
|------------------------------------------|-----------------|-----|-----|-----|-----|-----|----|----|----------|
|                                          | D15             | D14 | D13 | D12 | D11 | D10 | D9 | D8 |          |
| Digit 0 5 × 7 matrix character, 1st row  | 0               | 0   | 1   | 0   | 0   | 0   | 0  | 0  | 0x20     |
| Digit 1 5 × 7 matrix character, 1st row  | 0               | 0   | 1   | 0   | 0   | 0   | 0  | 1  | 0x21     |
| Digit 2 5 × 7 matrix character, 1st row  | 0               | 0   | 1   | 0   | 0   | 0   | 1  | 0  | 0x22     |
| <b>UP TO</b>                             | —               | —   | —   | —   | —   | —   | —  | —  | —        |
| Digit 45 5 × 7 matrix character, 1st row | 0               | 1   | 0   | 0   | 1   | 1   | 0  | 1  | 0x4D     |
| Digit 46 5 × 7 matrix character, 1st row | 0               | 1   | 0   | 0   | 1   | 1   | 1  | 0  | 0x4E     |
| Digit 47 5 × 7 matrix character, 1st row | 0               | 1   | 0   | 0   | 1   | 1   | 1  | 1  | 0x4F     |
| Digit 0 5 × 7 matrix character, 2nd row  | 0               | 1   | 0   | 1   | 0   | 0   | 0  | 0  | 0x50     |
| Digit 1 5 × 7 matrix character, 2nd row  | 0               | 1   | 0   | 1   | 0   | 0   | 0  | 1  | 0x51     |
| Digit 2 5 × 7 matrix character, 2nd row  | 0               | 1   | 0   | 1   | 0   | 0   | 1  | 0  | 0x52     |
| <b>UP TO</b>                             | —               | —   | —   | —   | —   | —   | —  | —  | —        |
| Digit 45 5 × 7 matrix character, 2nd row | 0               | 1   | 1   | 1   | 1   | 1   | 0  | 1  | 0x7D     |
| Digit 46 5 × 7 matrix character, 2nd row | 0               | 1   | 1   | 1   | 1   | 1   | 1  | 0  | 0x7E     |
| Digit 47 5 × 7 matrix character, 2nd row | 0               | 1   | 1   | 1   | 1   | 1   | 1  | 1  | 0x7F     |

**Table 6. Character Registers Format**

| MODE                                                                     | COMMAND ADDRESS                                      | REGISTER DATA |                                               |    |    |    |    |    |    |  |
|--------------------------------------------------------------------------|------------------------------------------------------|---------------|-----------------------------------------------|----|----|----|----|----|----|--|
|                                                                          |                                                      | D7            | D6                                            | D5 | D4 | D3 | D2 | D1 | D0 |  |
| Writing character data to use font map data with DP segment <b>unlit</b> | 0x20 to 0x4F (48/1 mode)<br>0x20 to 0x7F (96/2 mode) | 0             | Bits D6 to D0 select font characters 0 to 127 |    |    |    |    |    |    |  |
| Writing character data to use font map data with DP segment <b>lit</b>   | 0x20 to 0x4F (48/1 mode)<br>0x20 to 0x7F (96/2 mode) | 1             |                                               |    |    |    |    |    |    |  |

down mode is overridden when in display test mode. For normal operation, set S bit to 1.

When the MAX6853 is in shutdown mode, the multiplex oscillator is halted at the end of the current 100μs multiplex period (OSC = 4MHz), and the VFBLANK output is used to disable the VFD tube driver. Data in the digit and other control registers remains unaltered.

If the PUMP output is configured as a square-wave clock, then the PUMP output is forced low for the duration of shutdown, and the square-wave clock restored when the MAX6853 comes out of shutdown.

If the PHASE1 output or PHASE2 output is configured as a filament driver, then that output is forced low for the duration of shutdown and the filament drive waveforms restored when the MAX6853 comes out of shutdown.

When the MAX6853 comes out of shutdown, the external VFD tube driver is presumed to contain invalid data. The VFBLANK output is used to disable the VFD tube driver for the first multiplex cycle after exiting shutdown,

clearing any invalid data. The next multiplex cycle uses newly sent valid data.

### **Configuration Lock (L Data Bit D1) Format**

The configuration lock register is a safety feature to reduce the risk of the VFD configuration settings being inadvertently changed due to spurious writes if software fails. When set, the shift-limit register (0x0E), grids register (0x03), and output map data (0x06) can be read but cannot be written. The output map data pointer itself may be written in order to allow the output map data to be read back (Table 19).

### **Blink Rate Selection (B Data Bit D2) Format**

The B bit in the configuration register selects the blink rate of the cursor and annunciator segments. This is the speed that the segments blink on and off when blinking is selected for these segments. The frequency of the multiplex clock OSC and the setting of the B bit (Table 20) determine the blink rate.

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## **Global Blink Timing Synchronization (T Data Bit D4) Format**

Setting the T bit in multiple MAX6853s at the same time (or in quick succession) synchronizes the blink timing across all the devices (Table 21). The display multiplexing sequence is also reset, which can give rise to a one-time display flicker when the register is written.

## **Global Clear Digit Data (R Data Bit D5) Format**

When the R bit (Table 22) is set, the segment and annunciator data are cleared.

## **Display Mode (M Data Bit D6) Format**

The M bit (Table 23) selects the display modes (Table 1). The display modes trade the maximum allowable number of digits (mode 96/2) against the availability of annunciator segments (mode 48/1).

## **Blink Phase Readback (P Data Bit D7) Format**

When the configuration register is read, the P bit reflects the blink phase at that time (Table 24).

## **Serial Interface**

### **Serial Addressing**

The MAX6853 operates as a slave that sends and receives data through an I<sup>2</sup>C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX6853, and generates the SCL clock that synchronizes the data transfer (Figure 6).

The MAX6853 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on the SDA. The MAX6853 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 7) sent by a master, followed by the MAX6853 7-bit slave address plus R/W bit (Figure 10), a register address byte, 1 or more data bytes, and finally a STOP condition (Figure 7).

### **Start and Stop Conditions**

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning the SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 7).

## **Bit Transfer**

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 8).

## **Acknowledge**

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 9). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX6853, the MAX6853 generates the acknowledge bit because the MAX6853 is the recipient. When the MAX6853 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. In this case, the master acknowledges all bytes received from the MAX6853 except for the last byte required, after which the master issues a STOP condition to signify end of transmission.

## **Slave Address**

The MAX6853 has a 7-bit-long slave address (Figure 10). The eighth bit following the 7-bit slave address is the R/W bit. Set it low for a write command and high for a read command.

The first 5 bits (MSBs) of the MAX6853 slave address are always 11101. Slave address bits A1 and A0 are selected by the address input pins AD0. This input may be connected to GND, V+, SDA, or SCL. The MAX6853 has four possible slave addresses (Table 7) and therefore a maximum of four MAX6853 devices may share the same interface.

## **Message Format for Writing**

A write to the MAX6853 comprises the transmission of the MAX6853's slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte, which determines which register of the MAX6853 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, then the MAX6853 takes no further action (Figure 11) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX6853 selected by the command byte (Figure 12).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX6853 internal registers because the

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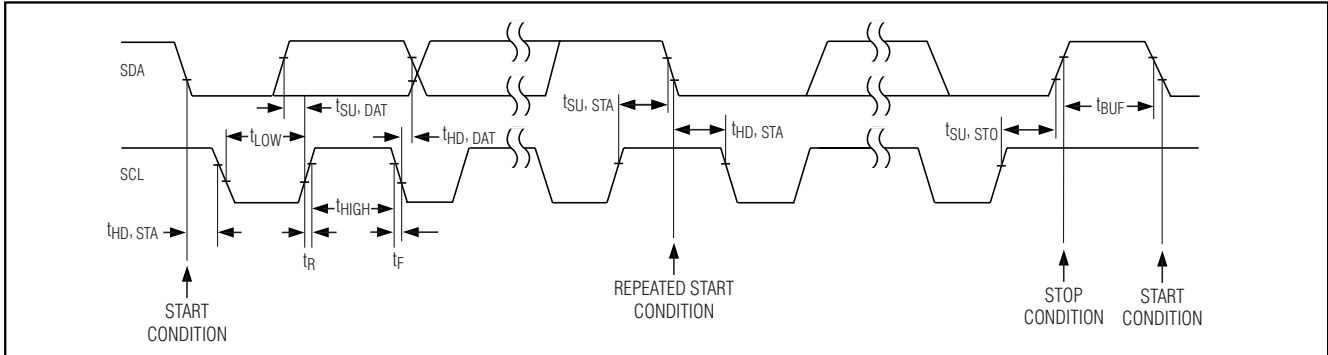


Figure 6. 2-Wire Serial Interface Timing Details

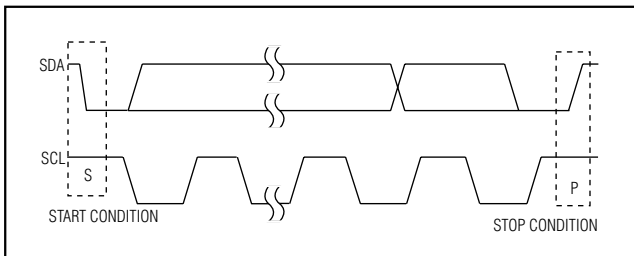


Figure 7. Start and Stop Conditions

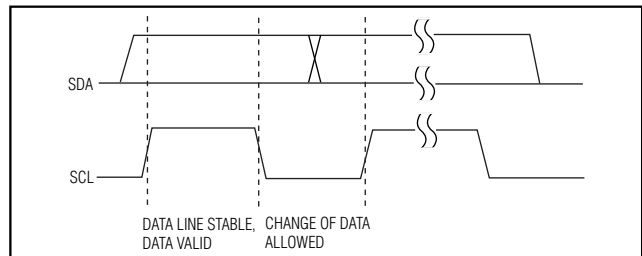


Figure 8. Bit Transfer

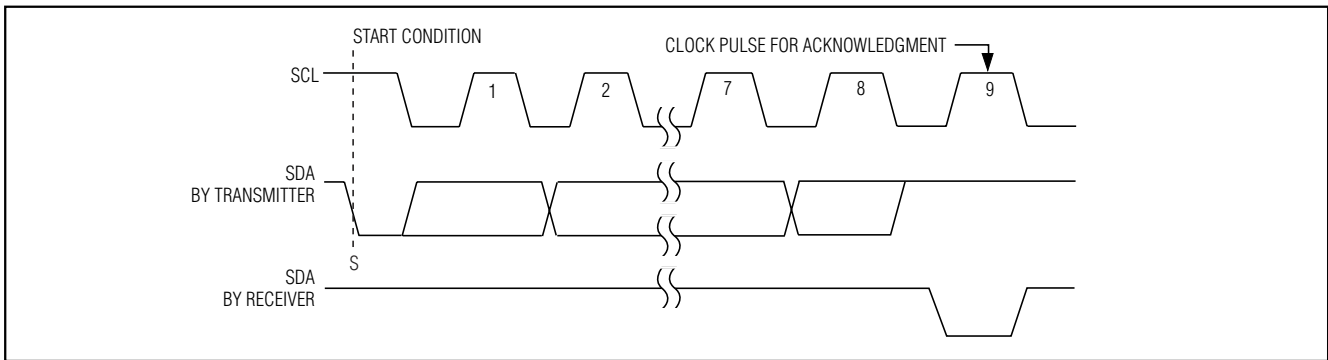


Figure 9. Acknowledge

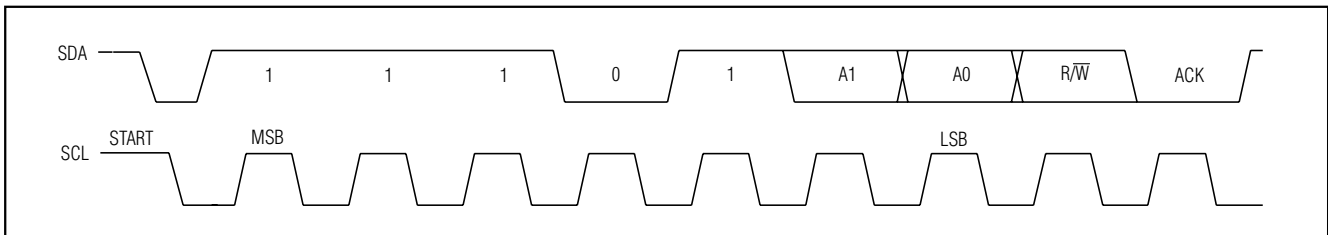


Figure 10. Slave Address

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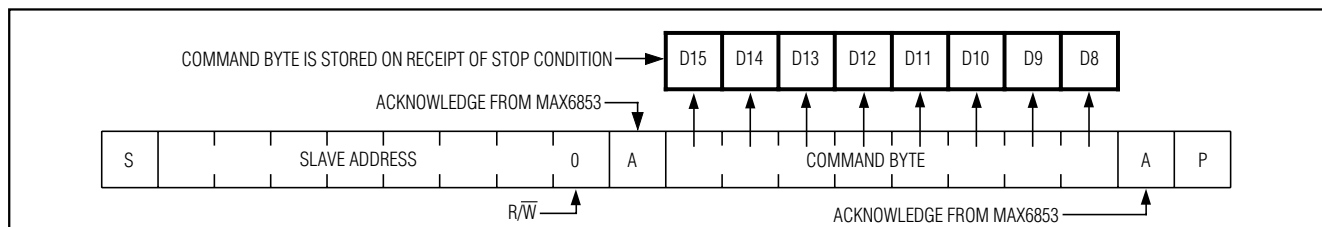


Figure 11. Command Byte Received

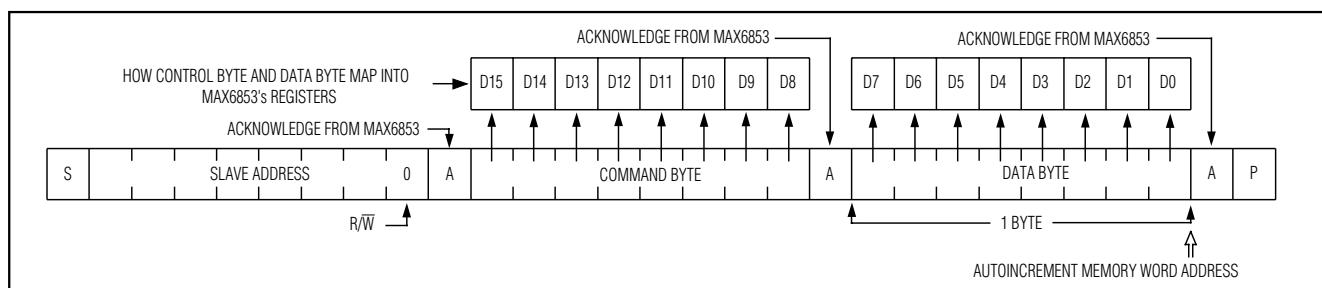


Figure 12. Command and Single Data Byte Received

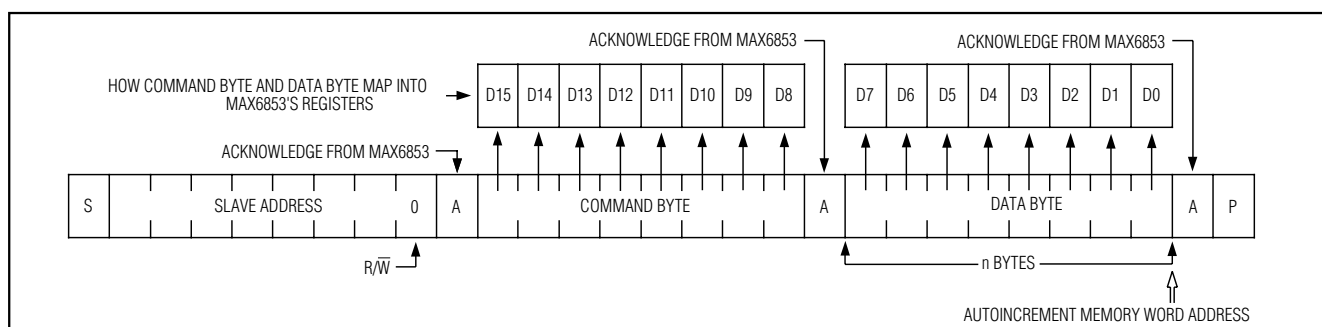


Figure 13. n Data Bytes Received

command byte address generally autoincrements (Table 8) (Figure 13).

### Message Format for Reading

The MAX6853 is read using the MAX6853's internally stored command byte as address pointer, the same way the stored command byte is used as address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 8). Thus, a read is initiated by first configuring the MAX6853's command byte by performing a write (Figure 11). The master can now read n consecutive bytes from the MAX6853, with the first data byte being read from the register addressed by the initialized command byte (Figure 13). When performing read-after-write verification, reset the command byte's address because the stored byte address is autoincremented after the write (Table 8).

### Operation with Multiple Masters

If the MAX6853 is operated on a 2-wire interface with multiple masters, a master reading the MAX6853 should use a repeated start between the write, which sets the MAX6853's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master

Table 7. MAX6853 Address Map

| PIN | DEVICE ADDRESS |    |    |    |    |    |    |
|-----|----------------|----|----|----|----|----|----|
|     | A6             | A5 | A4 | A3 | A2 | A1 | A0 |
| GND | 1              | 1  | 1  | 0  | 1  | 0  | 0  |
| V+  | 1              | 1  | 1  | 0  | 1  | 0  | 1  |
| SDA | 1              | 1  | 1  | 0  | 1  | 1  | 0  |
| SCL | 1              | 1  | 1  | 0  | 1  | 1  | 1  |



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**Table 8. Command Address Autoincrement Rules**

| COMMAND BYTE ADDRESS RANGE | AUTOINCREMENT BEHAVIOR                                                                                                       |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------|
| x0000000 to x0000100       | Command byte address autoincrements after byte read or written.                                                              |
| x0000110                   | Command byte address remains at x0000110 after byte read or written, but the font output map address pointer autoincrements. |
| x0010000                   | Factory reserved; do not write to this register.                                                                             |
| x000111 to x1111110        | Command byte address autoincrements after byte read or written.                                                              |
| x1111111                   | Command byte address remains at x1111111 after byte read or written.                                                         |

1 has set up the MAX6853's address pointer but before master 1 has read the data. If master 2 subsequently changes the MAX6853's address pointer, then master 1's delayed read may be from an unexpected location.

### Command Address Autoincrementing

Address autoincrementing allows the MAX6853 to be configured with the shortest number of transmissions by minimizing the number of times the command byte needs to be sent. The command address or the font pointer address stored in the MAX6853 generally increments after each data byte is written or read (Table 8).

### VFD Driver Serial Interface

The VFD driver interface on the MAX6853 is a serial interface using three outputs, VFLOAD, VFCLK, and VFDOOUT (Figure 14) to drive industry-standard, shift-register, high-voltage grid/anode VFD tube drivers (Figures 3 and 4). The speed of VFCLK is 2MHz when OSC is 4MHz. The maximum speed of VFCLK is 4MHz when OSC is 8MHz. This interface transfers display data from the MAX6853 to the VFD tube driver. The serial interface bit stream output is programmable up to 122 bits, which are labeled DD0–DD121.

The functions of the three interface outputs are as follows: VFCLK is the serial clock output, which shifts data on its falling edge from the MAX6853's 122-bit output shift register to VFLOAD.

VFDOOUT is the serial data output. The data changes on VFCLK's falling edge, and is stable when it is sampled by the display driver on the rising edge of VFCLK.

VFLOAD is the latch-load output. VFLOAD is high to transfer data from the display tube driver's shift register to the display driver's output latch (transparent mode), and low to retain that data in the display driver's output latch.

A fourth output, VFBLANK, provides gating control of the tube driver. VFBLANK can be configured to be either high or low using the VBLANK polarity register (Table 27) to enable the VFD tube driver. In the default

condition, VFBLANK is high to disable the VFD tube driver, which is expected to force its driver outputs low to blank the display without altering the contents of its output latches. In the default condition, VFBLANK is low to enable its VFD tube driver outputs to follow the state of the VFD tube driver's output latches. The VFBLANK output is used for PWM intensity control and to disable the VFD tube driver in shutdown.

### Multiplex Architecture

The multiplex engine transmits grid and anode control data to the external VFD driver using the VFCLK, VFDOOUT, and VFLOAD. The number of data bits  $m$  transmitted is set by the user in the shift-limit register (Table 29). Figure 15 is the VFD multiplex timing diagram.

The essential rules for multiplex action are as follows:

- The external VFD driver's data latch contains the data for the current grid being displayed.
- The VFBLANK input is controlled to provide the PWM intensity control.
- The VFCLK and VFDOOUT outputs are used to fill the external VFD driver's shift register with the multiplex data for the next grid, during the multiplex timeslot for the current grid.
- The VFLOAD output loads the new grid-anode data pattern at the start of its multiplex cycle.

### Grids Register

The grids register sets how many grids are multiplexed from 1 to 48 (Table 25).

When the grids register is written, the external VFD tube driver is presumed to contain invalid data. The VFBLANK output disables the VFD tube driver for the first multiplex cycle after exiting shutdown, clearing any invalid data. The next multiplex cycle uses newly sent valid data. If the grids register is written with an out-of-range value of 0x30 to 0xFF, then the value 0x2F is stored instead.



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## Intensity Register

Digital control of display brightness is provided by pulse-width modulation of the tube blanking time, which is controlled by the lower nibble of the intensity register (Table 26). The modulator scales the VFBLANK output in 15 steps from a minimum of 1/16 up to 15/16 of each grid's multiplex period (Figure 16). Figure 17 shows the modulator behavior when the VFBLANK polarity register is set to 0x00 (Table 27), so VFBLANK is high to disable (blank) the display.

The minimum off-time period of a 1/16 multiplex period (6.25μs with OSC = 4MHz) is always at the start of the multiplex cycle. This allows time for slow display drivers to turn off, and slow display phosphors time to decay between grids. Thus, image ghosting is avoided. If a display has very slow phosphor, double the allowed decay time by not using a 15/16 duty cycle.

## VFBLANK Polarity Register

The VFBLANK polarity register sets the active level of the VFBLANK output pin (Table 27).

## No-Op Register

A write to the no-op register is ignored.

## Display-Test and Device ID Register

Writing the display-test and device ID register switches the drivers between one of two modes: normal and display test. Display-test mode turns all segments and annunciators on and sets the duty cycle to 7/16 (half-power) (Table 28).

Reading the display-test and device ID register returns the MAX6853 device ID 0b0000 011 that identifies the driver type, plus the display-test status in the LSB.

## Output Shift-Limit Register

The output serial interface transfers display data from the MAX6853 to the display driver. The serial interface bit-stream output length is programmable up to 122 bits, which are labeled DD0–DD121. Set the number of bits with the shift-limit register, address 0x0E. If the shift-limit register is written with an out-of-range value 0x7A to 0xFF, then the value 0x79 is stored instead. Table 29 shows the shift-limit register.

## Output Map

The output map comprises 122 words of 7-bit RAM. The output map data should be written when the MAX6853 is configured after power-up. Table 30 shows the output map RAM codes.

Table 9. Character Map

| MSB<br>LSB | x000  | x001  | x010 | x011 | x100 | x101 | x110 | x111 |
|------------|-------|-------|------|------|------|------|------|------|
| 0000       | RAM00 | RAM16 |      |      |      |      |      |      |
| 0001       | RAM01 | RAM17 |      |      |      |      |      |      |
| 0010       | RAM02 | RAM18 |      |      |      |      |      |      |
| 0011       | RAM03 | RAM19 |      |      |      |      |      |      |
| 0100       | RAM04 | RAM20 |      |      |      |      |      |      |
| 0101       | RAM05 | RAM21 |      |      |      |      |      |      |
| 0110       | RAM06 | RAM22 |      |      |      |      |      |      |
| 0111       | RAM07 | RAM23 |      |      |      |      |      |      |
| 1000       | RAM08 |       |      |      |      |      |      |      |
| 1001       | RAM09 |       |      |      |      |      |      |      |
| 1010       | RAM10 |       |      |      |      |      |      |      |
| 1011       | RAM11 |       |      |      |      |      |      |      |
| 1100       | RAM12 |       |      |      |      |      |      |      |
| 1101       | RAM13 |       |      |      |      |      |      |      |
| 1110       | RAM14 |       |      |      |      |      |      |      |
| 1111       | RAM15 |       |      |      |      |      |      |      |

# 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

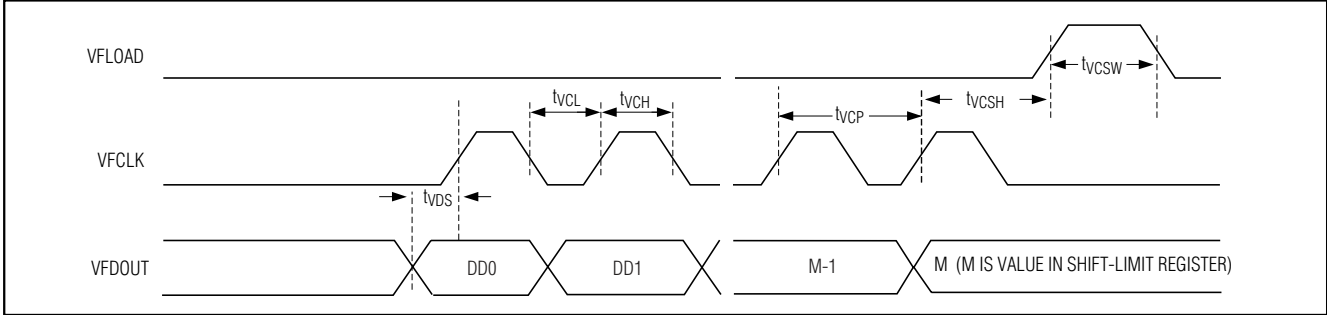


Figure 14. VFD Interface Timing Diagram

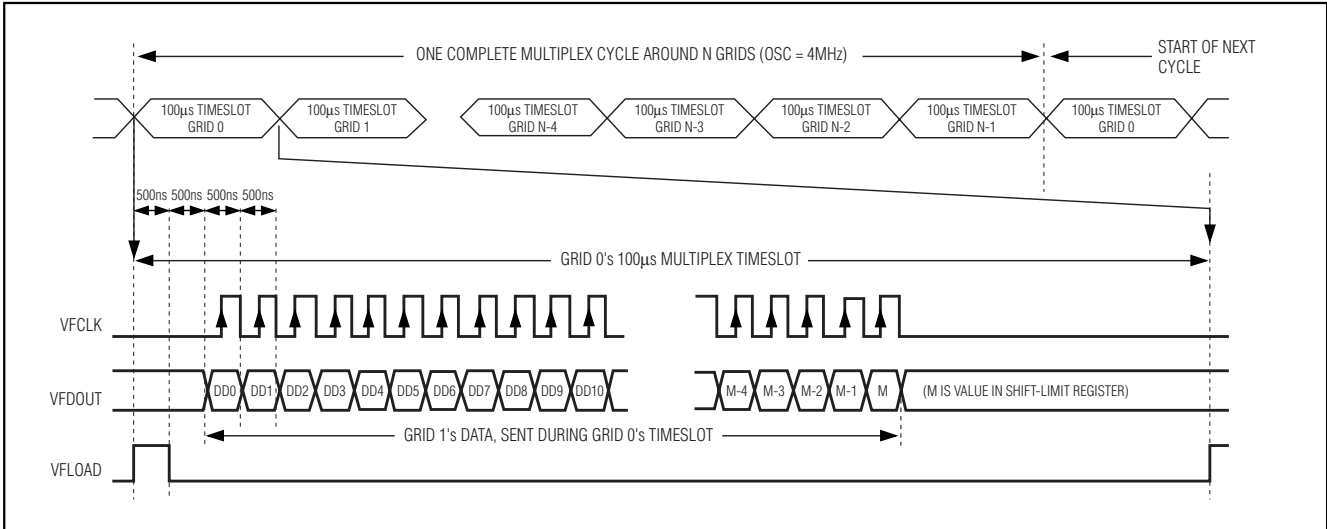


Figure 15. VFD Multiplex Timing Diagram

The output map is an indirect addressing reference table. It translates bit position in the output shift register (valid range: from zero to the value in shift-limit register 0x0E) to bit function. Any output shift-register bit position may be set to any grid, 5 × 7 matrix segment, DP segment, annunciator segment, or cursor segment.

The power-up default pattern for output map RAM maps a 40-digit, two-digits-per-grid display with DPs and cursors (Table 31).

Selecting an unused map RAM entry (126 or 127) for an output shift-register position always resets the corresponding output bit to low (segment or grid OFF).

When selecting an invalid map RAM entry (for example, codes 48 to 83 to select annunciators in 96/2 mode, which does not support annunciators), the corresponding output bit is always low (segment or grid OFF).

If the map RAM entry corresponds to a nonexistent font segment (no action in Table 30) when the digit data is processed through the character font, then the result again is zero (segment or grid OFF).

The output map data is indirectly accessed by an autoincrementing output map address pointer in the MAX6853 at address 0x06. The output map address pointer can be written (i.e., set to an address between 0x00 and 0x79) but cannot be read back. The output map data is written and read back through the output map address pointer.

Table 32 shows how to set the output map address pointer to a value within the acceptable range. Bit D7 is set to denote that the user is writing the output map address pointer. If the user attempts to set the output map address to one of the out-of-range addresses by writing data in range 0xFA to 0xFF, then address 0x00 is set instead.

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**MAX6853**

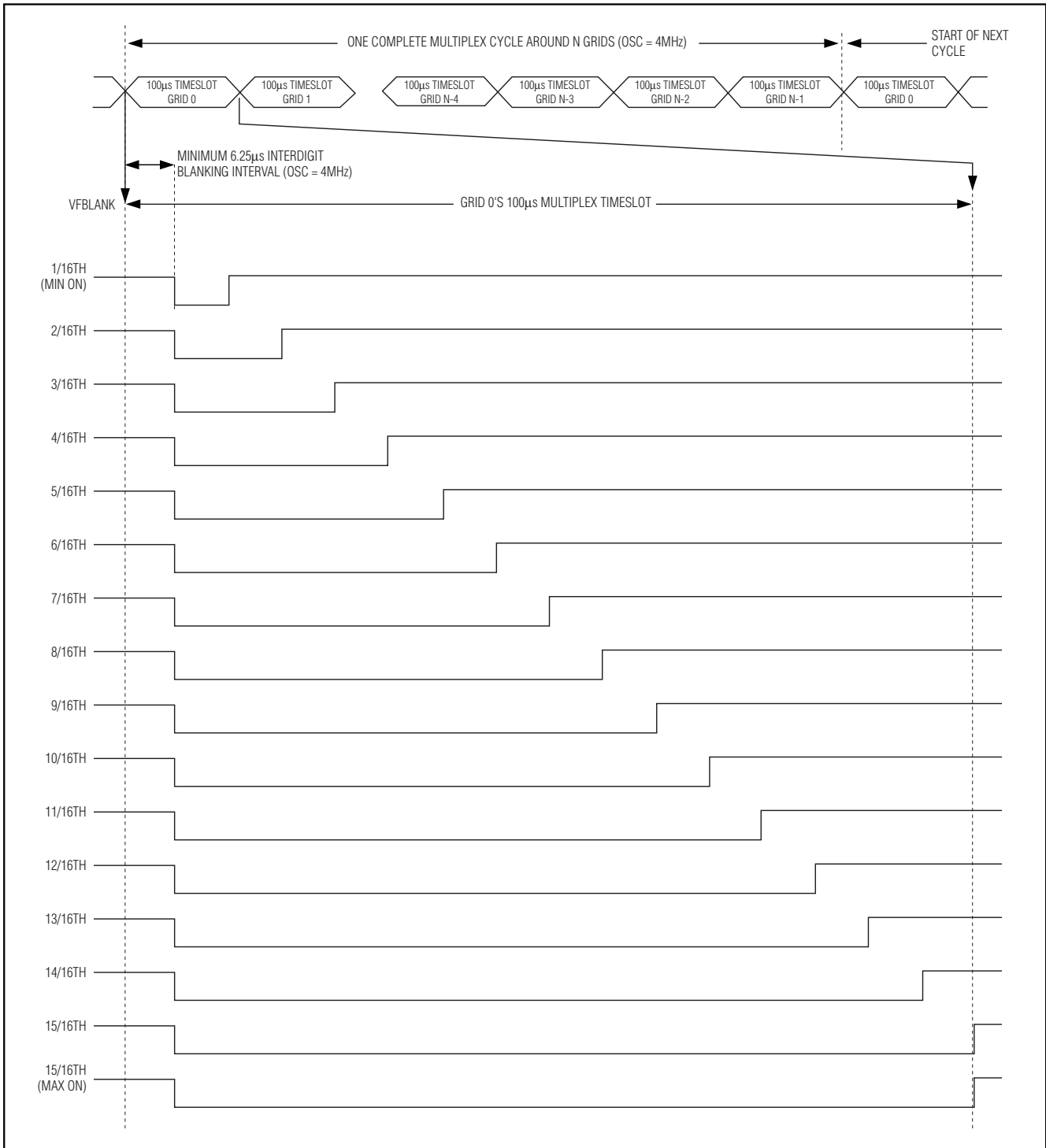


Figure 16. BLANK and Intensity Timing Diagram

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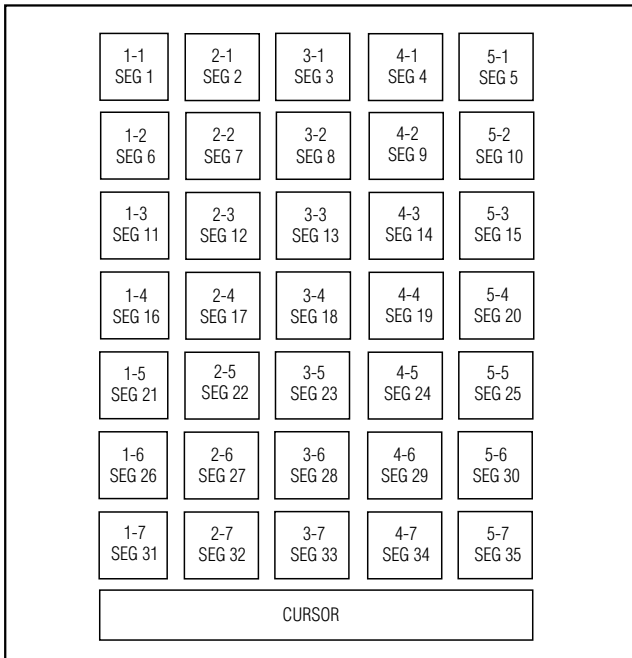


Figure 17. Relationship Between Segment Output and VFD Tube 5 × 7 Matrix Dots

After the last data location 0xF9 has been written, further output map data entries are ignored until the output map address pointer is reset.

The output map data can be written to the address set by the output map address pointer. Bit D7 is clear to denote that the user is writing actual output map data. The output map address pointer is autoincremented after the output map data has been written to the current location. If the user writes the output map data in the RAM order, then the output map address pointer need only be set once, or even not at all as the address is set to 0x00 as power-up default (Table 33).

The output map data can be read by reading address 0x86. The 7-bit output map data at the address set by the output map address pointer is read back, with the MSB clear. The output map address pointer is autoincremented after the output map data has been read from the current location, in the same way as for a write (Table 34).

### Filament Drive

The VFD filament is typically driven with an AC waveform, supplied by a center-tapped 50Hz or 60Hz power transformer as part of the system power supply. However, if the system has only DC supplies available,

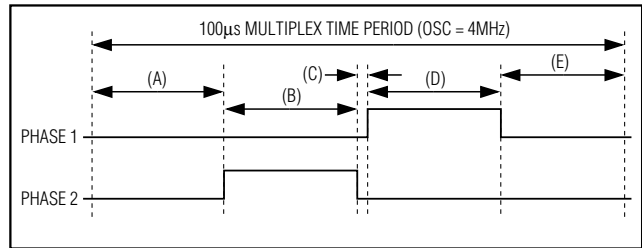


Figure 18. Filament Bridge Driver Timing Waveforms

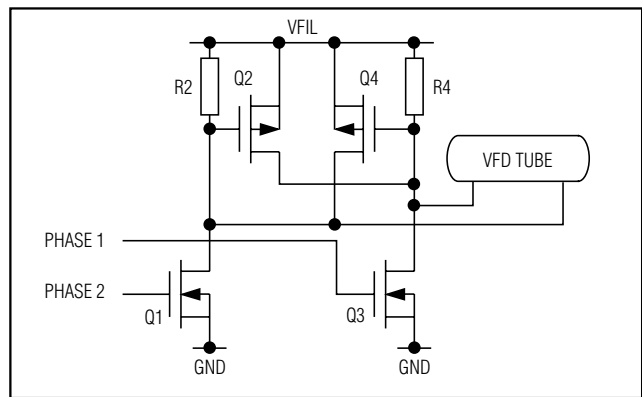


Figure 19. Filament Bridge Driver (MOSFET)

the filament must be powered by a DC-to-AC or DC-to-DC converter.

The MAX6853 can generate the waveforms on the PHASE1 and PHASE2 outputs to drive the VFD filament using a full bridge (push-pull drive). The PHASE1 and PHASE2 outputs can be used as general-purpose outputs if the filament drive is not required. The bridge drive transistors are external, but the waveforms are generated by the MAX6853.

The waveform generation uses PWM to set the effective RMS voltage across the filament, as a fraction of the external supply voltage (Figure 18) (Table 35). The filament switching frequency is synchronized to the multiplex scan clock, eliminating beating artifacts due to differing filament and multiplex frequencies.

The PWM duty cycle is controlled by the filament duty-cycle register (Table 36). The effective RMS voltage across the filament is given by the expression:

$$V_{RMS} = FilOn \times (VFIL - V_{LO-BRIDGE} - V_{HI-BRIDGE}) / 200$$

or, rearranged:

$$Duty = 200 \times V_{RMS} / (VFIL - V_{LO-BRIDGE} - V_{HI-BRIDGE})$$

where:

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FilOn is the number to store in the filament duty-cycle register, address 0x09.

VFIL is the supply voltage to the filament driver bridge (V).

VRMS is the specified nominal filament supply voltage (V).

VLO-BRIDGE is the voltage drop across a low-side bridge driver (V).

VHI-BRIDGE is the voltage drop across a high-side bridge driver (V).

The minimum commutation time, shown at (C) in Figure 18, is set by (2/OSC)s (500ns when OSC = 4MHz) to ensure that shoot-through currents cannot flow during phase reversal. Otherwise, the duty cycle of the bridge sets the RMS voltage across the filament. This technique provides a low-cost AC filament supply when using a regulated supply higher than the RMS voltage rating of the filament.

Figure 19 shows the external components required for the filament driver using a FET bridge.

## PHASE1 and PHASE2 Outputs

PHASE1 and PHASE2 can be individually programmed as one of four output types (Tables 37, 38).

When using the filament drive, first ensure that the filament duty-cycle register 0x09 is set to the correct value before configuring the PHASE1 and PHASE2 outputs to be filament drives. To stop the filament drive, program either PHASE1 or PHASE2 (or both) to be logic-low general-purpose outputs. Both PHASE1 and PHASE2 outputs come out of power-on-reset in logic-low condition.

## PORT0 and PORT1 Outputs

PORT0 and PORT1 can be individually programmed as one of eight output types (Tables 39, 40). The PORT1 choices are similar to the PORT0 choices, except that the last four items are invert logic. PORT0 output comes out of power-on-reset in logic-low condition, whereas PORT1 output initializes high.

The PORT0 and PORT1 shutdown outputs allow external hardware (for example, a DC-to-DC converter power supply for VFD) to be disabled by the MAX6853 when the MAX6853 is shut down.

The 625Hz, 1250Hz, and 2500Hz outputs can drive a piezo sounder either from PORT0 or PORT1 alone, or by both ports together as bridge drive. For bridge drive, the sounder is connected between PORT0 and PORT1, taking advantage of the PORT1 output being inverted with respect to PORT0. Select different frequencies for PORT0 and PORT1 to obtain a wider range of sounds when bridge drive is used.

## PUMP Output

Program the PUMP output as one of four output types (Table 41).

## Multiplex Clock and Blink Timing

The OSC1 and OSC2 inputs set the multiplex and blink timing for the display driver. Connect an external resistor from OSC2 to GND and an external capacitor C<sub>OSC</sub> from OSC1 to GND to set the frequency of the internal RC oscillator. Alternatively, overdrive OSC1 with an external TTL or CMOS clock. Use an external clock ranging between 2MHz and 8MHz to drive OSC1 to produce an exact blink rate or multiplier period.

The multiplex clock frequency determines the multiplex scan rate and the blink timing. The display scan rate is {OSC / 400 / (1 + grids register value)}. There are 400 OSC cycles per digit multiplex period. For example, with OSC = 4MHz, each display digit is enabled for 100μs. For a 40-grid display tube (grids register value = 39 or 0x27), the display scan rate is 250Hz.

The BLINK output is the selectable blink period clock. It is nominally 0.5Hz or 1Hz (OSC = 4MHz). It is low during the first half of the blink period, and high during the second half. The PORT0 and PORT1 general-purpose outputs may be programmed to be BLINK output. Synchronize the BLINK timing if desired by setting the T bit in the configuration register (Table 21).

The RC oscillator uses an external resistor R<sub>OSC</sub> and an external capacitor C<sub>OSC</sub> to set the oscillator frequency. R<sub>OSC</sub> connects from OSC2 to ground. C<sub>OSC</sub> connects from OSC1 to ground. The following values of R<sub>OSC</sub> and C<sub>OSC</sub> set the oscillator to 4MHz, which makes the BLINK frequencies 0.5Hz and 1 Hz:

$$f_{OSC} = K_F / (R_{OSC} \times [C_{OSC} + C_{STRAY}]) \text{ MHz}$$

where:

$$K_F = 2320$$

R<sub>OSC</sub> = external resistor in kΩ (allowable range 8kΩ to 80kΩ)

C<sub>OSC</sub> = external capacitor in pF

C<sub>STRAY</sub> = stray capacitance from OSC1 to GND in pF, typically 2pF

For OSC = 4MHz, R<sub>OSC</sub> is 10kΩ and C<sub>OSC</sub> is 56pF.

The effective value of C<sub>OSC</sub> includes not only the actual external capacitor used, but also the stray capacitance from OSC1 to GND. This capacitance is usually in the 1pF to 5pF range, depending on the layout used.

The allowed range of f<sub>OSC</sub> is 2MHz to 8MHz. If f<sub>OSC</sub> is set too high, the internal oscillator can stop working. An internal fail-safe circuit monitors the multiplex clock and

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detects a slow or nonworking multiplex clock. When a slow or nonworking multiplex clock is detected, an internal fail-safe oscillator generates a replacement clock of about 200kHz. This backup clock ensures that the VFD is not damaged by the multiplex operation halting inadvertently. The scan rate for 16 digits is about 15Hz in fail-safe mode, and the display flickers. A flickering display is a good indication that there is a problem with the multiplex clock.

### Power Supplies

The MAX6853 operates from a single 2.7V to 3.6V power supply. Bypass the power supply to GND with a 0.1μF capacitor as close to the device as possible. Add a bulk capacitor (such as a low-cost electrolytic 1μF to 22μF) if the MAX6853 is driving high current from any of the general-purpose output ports.

**Table 10. Memory Mapping of User-Defined Font Register 0x05**

| COMMAND ADDRESS | REGISTER DATA | READ OR WRITE | FUNCTION                                                                                                                                                    |
|-----------------|---------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x05            | 0x00–0x7F     | Read          | Read 7-bit user-definable font data entry from current font address. MSB of the register data is clear. Font address pointer is incremented after the read. |
| 0x05            | 0x00–0x7F     | Write         | Write 7-bit user-definable font data entry to current font address. Font address pointer is incremented after the write.                                    |
| 0x05            | 0x80–0xFF     | Write         | Write font address pointer with the register data.                                                                                                          |

**Table 11. Font Pointer Address Behavior**

| FONT POINTER ADDRESS | ACTION                                                                                                                                            |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x80 to 0xF6         | Valid range to set the font address pointer. Pointer autoincrements after a font data read or write, while pointer address remains in this range. |
| 0xF7                 | Further font data is ignored after a font data read or write to this pointer address.                                                             |
| 0xF8 to 0xFF         | Invalid range to set the font address pointer. Pointer is set to 0x80.                                                                            |

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**Table 12. User-Definable Font Pointer Base Address Table**

| FONT CHARACTER | COMMAND ADDRESS | REGISTER DATA | REGISTER DATA |    |    |    |    |    |    |    |
|----------------|-----------------|---------------|---------------|----|----|----|----|----|----|----|
|                |                 |               | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RAM00          | 0x05            | 0x80          | 1             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| RAM01          | 0x05            | 0x85          | 1             | 0  | 0  | 0  | 0  | 1  | 0  | 1  |
| RAM02          | 0x05            | 0x8A          | 1             | 0  | 0  | 0  | 1  | 0  | 1  | 0  |
| RAM03          | 0x05            | 0x8F          | 1             | 0  | 0  | 0  | 1  | 1  | 1  | 1  |
| RAM04          | 0x05            | 0x94          | 1             | 0  | 0  | 1  | 0  | 1  | 0  | 0  |
| RAM05          | 0x05            | 0x99          | 1             | 0  | 0  | 1  | 1  | 0  | 0  | 1  |
| RAM06          | 0x05            | 0x9E          | 1             | 0  | 0  | 1  | 1  | 1  | 1  | 0  |
| RAM07          | 0x05            | 0xA3          | 1             | 0  | 1  | 0  | 0  | 0  | 1  | 1  |
| RAM08          | 0x05            | 0xA8          | 1             | 0  | 1  | 0  | 1  | 0  | 0  | 0  |
| RAM09          | 0x05            | 0xAD          | 1             | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| RAM10          | 0x05            | 0xB2          | 1             | 0  | 1  | 1  | 0  | 0  | 1  | 0  |
| RAM11          | 0x05            | 0xB7          | 1             | 0  | 1  | 1  | 0  | 1  | 1  | 1  |
| RAM12          | 0x05            | 0xBC          | 1             | 0  | 1  | 1  | 1  | 1  | 0  | 0  |
| RAM13          | 0x05            | 0xC1          | 1             | 1  | 0  | 0  | 0  | 0  | 0  | 1  |
| RAM14          | 0x05            | 0xC6          | 1             | 1  | 0  | 0  | 0  | 1  | 1  | 0  |
| RAM15          | 0x05            | 0xCB          | 1             | 1  | 0  | 0  | 1  | 0  | 1  | 1  |
| RAM16          | 0x05            | 0xD0          | 1             | 1  | 0  | 1  | 0  | 0  | 0  | 0  |
| RAM17          | 0x05            | 0xD5          | 1             | 1  | 0  | 1  | 0  | 1  | 0  | 1  |
| RAM18          | 0x05            | 0xDA          | 1             | 1  | 0  | 1  | 1  | 0  | 1  | 0  |
| RAM19          | 0x05            | 0xDF          | 1             | 1  | 0  | 1  | 1  | 1  | 1  | 1  |
| RAM20          | 0x05            | 0xE4          | 1             | 1  | 1  | 0  | 0  | 1  | 0  | 0  |
| RAM21          | 0x05            | 0xE9          | 1             | 1  | 1  | 0  | 1  | 0  | 0  | 1  |
| RAM22          | 0x05            | 0xEE          | 1             | 1  | 1  | 0  | 1  | 1  | 1  | 0  |
| RAM23          | 0x05            | 0xF3          | 1             | 1  | 1  | 1  | 0  | 0  | 1  | 1  |

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**Table 13. User-Definable Character Storage Example**

| FONT CHARACTER | FONT ADDRESS POINTER | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    |
|----------------|----------------------|-----------------|---------------|----|----|----|----|----|----|----|
|                |                      |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RAM00          | 0x00                 | 0x05            | 0             | 0  | 1  | 1  | 1  | 1  | 1  | 0  |
| RAM00          | 0x01                 | 0x05            | 0             | 1  | 0  | 1  | 0  | 0  | 0  | 1  |
| RAM00          | 0x02                 | 0x05            | 0             | 1  | 0  | 0  | 1  | 0  | 0  | 1  |
| RAM00          | 0x03                 | 0x05            | 0             | 1  | 0  | 0  | 0  | 1  | 0  | 1  |
| RAM00          | 0x04                 | 0x05            | 0             | 0  | 1  | 1  | 1  | 1  | 1  | 0  |
| RAM01          | 0x05                 | 0x05            | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| RAM01          | 0x06                 | 0x05            | 0             | 1  | 0  | 0  | 0  | 0  | 1  | 0  |
| RAM01          | 0x07                 | 0x05            | 0             | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| RAM01          | 0x08                 | 0x05            | 0             | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| RAM01          | 0x09                 | 0x05            | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| RAM02          | 0x0A                 | 0x05            | 0             | 1  | 0  | 0  | 0  | 0  | 1  | 0  |
| RAM02          | 0x0B                 | 0x05            | 0             | 1  | 1  | 0  | 0  | 0  | 0  | 1  |
| RAM02          | 0x0C                 | 0x05            | 0             | 1  | 0  | 1  | 0  | 0  | 0  | 1  |
| RAM02          | 0x0D                 | 0x05            | 0             | 1  | 0  | 0  | 1  | 0  | 0  | 1  |
| RAM02          | 0x0E                 | 0x05            | 0             | 1  | 0  | 0  | 0  | 1  | 1  | 0  |

**Table 14. Setting a Font Character to RAM Example**

| COMMAND ADDRESS | REGISTER DATA | ACTION BEING PERFORMED                                                                              |
|-----------------|---------------|-----------------------------------------------------------------------------------------------------|
| 0x05            | 0x8A          | Set font address pointer to the base address of font character RAM02.                               |
| 0x05            | 0x42          | 1st 7 bits of data: 1000010 goes to font address 0x8A; pointer then autoincrements to address 0x8B. |
| 0x05            | 0x61          | 2nd 7 bits of data: 1100001 goes to font address 0x8B; pointer then autoincrements to address 0x8C. |
| 0x05            | 0x51          | 3rd 7 bits of data: 1010001 goes to font address 0x8C; pointer then autoincrements to address 0x8D. |
| 0x05            | 0x49          | 4th 7 bits of data: 1001001 goes to font address 0x8D; pointer then autoincrements to address 0x8E. |
| 0x05            | 0x46          | 5th 7 bits of data: 1000110 goes to font address 0x8E; pointer then autoincrements to address 0x8F. |

**Table 15. Cursor Register Format**

| MODE                                                                   | COMMAND ADDRESS | REGISTER DATA |                        |    |    |    |    |    |    |  |
|------------------------------------------------------------------------|-----------------|---------------|------------------------|----|----|----|----|----|----|--|
|                                                                        |                 | D7            | D6                     | D5 | D4 | D3 | D2 | D1 | D0 |  |
| Cursor register.                                                       | 0x0F            | <b>BLINK</b>  | <b>CURSOR POSITION</b> |    |    |    |    |    |    |  |
| Digit 1's cursor is lit continuously.                                  | 0x0F            | 0             | 0                      | 0  | 0  | 0  | 0  | 0  | 0  |  |
| Digit 1's cursor is lit only for the first half of each blink period.  | 0x0F            | 1             | 0                      | 0  | 0  | 0  | 0  | 0  | 0  |  |
| <b>UP TO</b>                                                           | 0x0F            | <b>UP TO</b>  |                        |    |    |    |    |    |    |  |
| Digit 96's cursor is lit continuously.                                 | 0x0F            | 0             | 1                      | 0  | 1  | 1  | 1  | 1  | 1  |  |
| Digit 96's cursor is lit only for the first half of each blink period. | 0x0F            | 1             | 1                      | 0  | 1  | 1  | 1  | 1  | 1  |  |
| No cursor is lit.                                                      | 0x0F            | X             | 1                      | 1  | X  | X  | X  | X  | X  |  |



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**Table 16. Annunciator Registers Format**

| ANNUNCIATOR BYTE                                                     | REGISTER DATA  |    |                |    |                |    |                |    |
|----------------------------------------------------------------------|----------------|----|----------------|----|----------------|----|----------------|----|
|                                                                      | D7             | D6 | D5             | D4 | D3             | D2 | D1             | D0 |
| BIT ALLOCATIONS                                                      | ANNUNCIATOR A4 |    | ANNUNCIATOR A3 |    | ANNUNCIATOR A2 |    | ANNUNCIATOR A1 |    |
| Annunciator A1 is off.                                               | X              | X  | X              | X  | X              | X  | 0              | 0  |
| Annunciator A1 is lit only for the first half of each blink period.  | X              | X  | X              | X  | X              | X  | 0              | 1  |
| Annunciator A1 is lit only for the second half of each blink period. | X              | X  | X              | X  | X              | X  | 1              | 0  |
| Annunciator A1 is lit continuously.                                  | X              | X  | X              | X  | X              | X  | 1              | 1  |
| Annunciator A2 is off.                                               | X              | X  | X              | X  | 0              | 0  | X              | X  |
| Annunciator A2 is lit only for the first half of each blink period.  | X              | X  | X              | X  | 0              | 1  | X              | X  |
| Annunciator A2 is lit only for the second half of each blink period. | X              | X  | X              | X  | 1              | 0  | X              | X  |
| Annunciator A2 is lit continuously.                                  | X              | X  | X              | X  | 1              | 1  | X              | X  |
| Annunciator A3 is off.                                               | X              | X  | 0              | 0  | X              | X  | X              | X  |
| Annunciator A3 is lit only for the first half of each blink period.  | X              | X  | 0              | 1  | X              | X  | X              | X  |
| Annunciator A3 is lit only for the second half of each blink period. | X              | X  | 1              | 0  | X              | X  | X              | X  |
| Annunciator A3 is lit continuously.                                  | X              | X  | 1              | 1  | X              | X  | X              | X  |
| Annunciator A4 is off.                                               | 0              | 0  | X              | X  | X              | X  | X              | X  |
| Annunciator A4 is lit only for the first half of each blink period.  | 0              | 1  | X              | X  | X              | X  | X              | X  |
| Annunciator A4 is lit only for the second half of each blink period. | 1              | 0  | X              | X  | X              | X  | X              | X  |
| Annunciator A4 is lit continuously.                                  | 1              | 1  | X              | X  | X              | X  | X              | X  |

**Table 17. Configuration Register Format**

| MODE                   | REGISTER DATA |    |    |    |    |    |    |    |
|------------------------|---------------|----|----|----|----|----|----|----|
|                        | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Configuration register | P             | M  | R  | T  | X  | B  | L  | S  |

**Table 18. Shutdown Control (S Data Bit D0) Format**

| MODE             | REGISTER DATA |    |    |    |    |    |    |    |
|------------------|---------------|----|----|----|----|----|----|----|
|                  | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Shutdown         | P             | M  | R  | T  | X  | B  | L  | 0  |
| Normal operation | P             | M  | R  | T  | X  | B  | L  | 1  |

**Table 19. Configuration Lock (L Data Bit D1) Format**

| MODE     | REGISTER DATA |    |    |    |    |    |    |    |
|----------|---------------|----|----|----|----|----|----|----|
|          | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Unlocked | P             | M  | R  | T  | X  | B  | 0  | S  |
| Locked   | P             | M  | R  | T  | X  | B  | 1  | S  |

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**Table 20. Blink Rate Selection (B Data Bit D2) Format**

| MODE                                                                                    | REGISTER DATA |    |    |    |    |    |    |    |
|-----------------------------------------------------------------------------------------|---------------|----|----|----|----|----|----|----|
|                                                                                         | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Slow blinking (cursor and annunciators blink on for 1s, off for 1s, for OSC = 4MHz)     | P             | M  | R  | T  | X  | 0  | L  | S  |
| Fast blinking (cursor and annunciators blink on for 0.5s, off for 0.5s, for OSC = 4MHz) | P             | M  | R  | T  | X  | 1  | L  | S  |

**Table 21. Global Blink Timing Synchronization (T Data Bit D4) Format**

| MODE                                                                       | REGISTER DATA |    |    |    |    |    |    |    |
|----------------------------------------------------------------------------|---------------|----|----|----|----|----|----|----|
|                                                                            | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Blink timing counters are unaffected.                                      | P             | M  | R  | 0  | X  | B  | L  | S  |
| Blink timing counters are cleared during the I <sup>2</sup> C acknowledge. | P             | M  | R  | 1  | X  | B  | L  | S  |

**Table 22. Global Clear Digit Data (R Data Bit D5) Format**

| MODE                                                                                                           | REGISTER DATA |    |    |    |    |    |    |    |
|----------------------------------------------------------------------------------------------------------------|---------------|----|----|----|----|----|----|----|
|                                                                                                                | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Segment and annunciator data are unaffected.                                                                   | P             | M  | 0  | T  | X  | B  | L  | S  |
| Segment and annunciator data (address range 0x20 to 0x7F) are cleared during the I <sup>2</sup> C acknowledge. | P             | M  | 1  | T  | X  | B  | L  | S  |

**Table 23. Display Mode (M Data Bit D6) Format**

| MODE | DISPLAY TYPE                       | REGISTER DATA |    |    |    |    |    |    |    |
|------|------------------------------------|---------------|----|----|----|----|----|----|----|
|      |                                    | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 48/1 | Up to 48 digits, 1 digit per grid  | P             | 0  | R  | T  | X  | B  | L  | S  |
| 96/2 | Up to 96 digits, 2 digits per grid | P             | 1  | R  | T  | X  | B  | L  | S  |

**Table 24. Blink Phase Readback (P Data Bit D7) Format**

| MODE           | REGISTER DATA |    |    |    |    |    |    |    |
|----------------|---------------|----|----|----|----|----|----|----|
|                | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| P1 blink phase | 0             | M  | R  | T  | X  | B  | L  | S  |
| P0 blink phase | 1             | M  | R  | T  | X  | B  | L  | S  |

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**Table 25. Grids Register Format**

| GRIDS                           | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|---------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                 |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| Display has 1 grid: G0          | 0x03            | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x00     |
| Display has 2 grids: G0 and G1  | 0x03            | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0x01     |
| Display has 3 grids: G0 to G2   | 0x03            | 0             | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0x02     |
| Display has 4 grids: G0 to G3   | 0x03            | 0             | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0x03     |
| <b>UP TO</b>                    | 0x03            | 0             | 0  | —  | —  | —  | —  | —  | —  | —        |
| Display has 45 grids: G0 to G44 | 0x03            | 0             | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 0x2C     |
| Display has 46 grids: G0 to G45 | 0x03            | 0             | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0x2D     |
| Display has 47 grids: G0 to G46 | 0x03            | 0             | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 0x2E     |
| Display has 48 grids: G0 to G47 | 0x03            | 0             | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 0x2F     |

**Table 26. Intensity Register Format**

| DUTY CYCLE     | VFBLANK BEHAVIOR<br>(OSC = 4MHz)                  | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|----------------|---------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                |                                                   |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| 1/16 (min on)  | High for 6.25µs, low for 6.25µs, high for 87.5µs  | 0x02            | X             | X  | X  | X  | 0  | 0  | 0  | 0  | 0xX0     |
| 2/16           | High for 6.25µs, low for 12.5µs, high for 81.25µs | 0x02            | X             | X  | X  | X  | 0  | 0  | 0  | 1  | 0xX1     |
| 3/16           | High for 6.25µs, low for 18.75µs, high for 75µs   | 0x02            | X             | X  | X  | X  | 0  | 0  | 1  | 0  | 0xX2     |
| 4/16           | High for 6.25µs, low for 25µs, high for 68.75µs   | 0x02            | X             | X  | X  | X  | 0  | 0  | 1  | 1  | 0xX3     |
| 5/16           | High for 6.25µs, low for 31.25µs, high for 62.5µs | 0x02            | X             | X  | X  | X  | 0  | 1  | 0  | 0  | 0xX4     |
| 6/16           | High for 6.25µs, low for 37.5µs, high for 56.25µs | 0x02            | X             | X  | X  | X  | 0  | 1  | 0  | 1  | 0xX5     |
| 7/16           | High for 6.25µs, low for 43.75µs, high for 50µs   | 0x02            | X             | X  | X  | X  | 0  | 1  | 1  | 0  | 0xX6     |
| 8/16           | High for 6.25µs, low for 50µs, high for 43.75µs   | 0x02            | X             | X  | X  | X  | 0  | 1  | 1  | 1  | 0xX7     |
| 9/16           | High for 6.25µs, low for 56.25µs, high for 37.5µs | 0x02            | X             | X  | X  | X  | 1  | 0  | 0  | 0  | 0xX8     |
| 10/16          | High for 6.25µs, low for 62.5µs, high for 31.25µs | 0x02            | X             | X  | X  | X  | 1  | 0  | 0  | 1  | 0xX9     |
| 11/16          | High for 6.25µs, low for 68.75µs, high for 25µs   | 0x02            | X             | X  | X  | X  | 1  | 0  | 1  | 0  | 0xXA     |
| 12/16          | High for 6.25µs, low for 75µs, high for 18.75µs   | 0x02            | X             | X  | X  | X  | 1  | 0  | 1  | 1  | 0xXB     |
| 13/16          | High for 6.25µs, low for 81.25µs, high for 12.5µs | 0x02            | X             | X  | X  | X  | 1  | 1  | 0  | 0  | 0xXC     |
| 14/16          | High for 6.25µs, low for 87.5µs, high for 6.25µs  | 0x02            | X             | X  | X  | X  | 1  | 1  | 0  | 1  | 0xXD     |
| 15/16          | High for 6.25µs, low for 93.75µs                  | 0x02            | X             | X  | X  | X  | 1  | 1  | 1  | 0  | 0xXE     |
| 15/16 (max on) | High for 6.25µs, low for 93.75µs                  | 0x02            | X             | X  | X  | X  | 1  | 1  | 1  | 1  | 0xFF     |

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**Table 27. VFBLANK Polarity Register Format**

| GRIDS                                   | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|-----------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                         |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| VFBLANK is high to disable the display. | 0x01            | X             | X  | X  | X  | X  | X  | 0  | 0  | 0xX0     |
| VFBLANK is low to disable the display.  | 0x01            | X             | X  | X  | X  | X  | X  | 1  | 0  | 0xX2     |

**Table 28. Display-Test and Device ID Register Format**

| MODE                                           | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    |
|------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|
|                                                |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Normal operation                               | 0x07            | X             | X  | X  | X  | X  | X  | X  | 0  |
| Display test                                   | 0x07            | X             | X  | X  | X  | X  | X  | X  | 1  |
| Read MAX6853 device ID and display test status | 0x07            | 0             | 0  | 0  | 0  | 0  | 1  | 1  | DT |

**Table 29. Shift-Limit Register Format**

| SHIFT LIMIT                           | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|---------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                       |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| Minimum setting example (01)          | 0x0E            | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0x01     |
| Maximum setting example (121 or 0x79) | 0x0E            | 0             | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 0x79     |

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**Table 30. Output Map RAM Codes**

| OUTPUT MAP RAM CODE (DECIMAL) | APPLICATION                                                                                                                                                                                         | FUNCTION MAPPED BY OUTPUT MAP RAM CODE                  |
|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|
| 0 to 47                       | 48 grids                                                                                                                                                                                            | Grids G0 to G47                                         |
| 48, 49, 50, 51, 52            | 5 x 7 matrix character segments<br><br>Digits 0 to 47 only<br><br>Use character registers 0x20 to 0x4F<br><b>(Figure 12)</b>                                                                        | 5 x 7 matrix character segments 1-1, 2-1, 3-1, 4-1, 5-1 |
| 53, 54, 55, 56, 57            |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-2, 2-2, 3-2, 4-2, 5-2 |
| 58, 59, 60, 61, 62            |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-3, 2-3, 3-3, 4-3, 5-3 |
| 63, 64, 65, 66, 67            |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-4, 2-4, 3-4, 4-4, 5-4 |
| 68, 69, 70, 71, 72            |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-5, 2-5, 3-5, 4-5, 5-5 |
| 73, 74, 75, 76, 77            |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-6, 2-6, 3-6, 4-6, 5-6 |
| 78, 79, 80, 81, 82            |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-7, 2-7, 3-7, 4-7, 5-7 |
| 83                            |                                                                                                                                                                                                     | 5 x 7 matrix character segment DP                       |
| 84, 85, 86, 87, 88            | 5 x 7 matrix character segments<br><br>Digits 48 to 95 only<br><br>Use character registers 0x50 to 0x7F<br><b>(Figure 12)</b><br><b>Only valid for 96/2 mode</b><br>(display mode select bit M = 1) | 5 x 7 matrix character segments 1-1, 2-1, 3-1, 4-1, 5-1 |
| 89, 90, 91, 92, 93            | —                                                                                                                                                                                                   | 5 x 7 matrix character segments 1-2, 2-2, 3-2, 4-2, 5-2 |
| 94, 95, 96, 97, 98            | —                                                                                                                                                                                                   | 5 x 7 matrix character segments 1-3, 2-3, 3-3, 4-3, 5-3 |
| 99, 100, 101, 102, 103        |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-4, 2-4, 3-4, 4-4, 5-4 |
| 104, 105, 106, 107, 108       |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-5, 2-5, 3-5, 4-5, 5-5 |
| 109, 110, 111, 112, 113       |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-6, 2-6, 3-6, 4-6, 5-6 |
| 114, 115, 116, 117, 118       |                                                                                                                                                                                                     | 5 x 7 matrix character segments 1-7, 2-7, 3-7, 4-7, 5-7 |
| 119                           |                                                                                                                                                                                                     | —                                                       |
| 120 to 123                    | 4 annunciators<br><br><b>Only valid for 48/1 mode</b><br>(display mode select bit M = 0)                                                                                                            | Annunciator A1 to annunciator A4                        |
| 124                           | Cursor                                                                                                                                                                                              | Cursor segment for digits 0 to 47 only                  |
| 125                           | Cursor<br><br><b>Only valid for 96/2 mode</b><br>(display mode select bit M = 1)                                                                                                                    | Cursor segment for digits 48 to 95 only                 |
| 126, 127                      | Unused                                                                                                                                                                                              | No action                                               |

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**Table 31. Output Map RAM Initial Power-Up Status**

| OUTPUT MAP RAM ADDRESS       | OUTPUT MAP RAM CODE ON POWER-UP (DECIMAL) | FUNCTION MAPPED BY OUTPUT MAP RAM CODE                  |
|------------------------------|-------------------------------------------|---------------------------------------------------------|
| 0x00 to 0x27                 | 0–39                                      | Grids 0–39                                              |
| 0x28, 0x29, 0x2A, 0x2B, 0x2C | 48, 49, 50, 51, 52                        | 5 × 7 matrix character segments 1-1, 2-1, 3-1, 4-1, 5-1 |
| 0x2D, 0x2E, 0x2F, 0x30, 0x31 | 53, 54, 55, 56, 57                        | 5 × 7 matrix character segments 1-2, 2-2, 3-2, 4-2, 5-2 |
| 0x32, 0x33, 0x34, 0x35, 0x36 | 58, 59, 60, 61, 62                        | 5 × 7 matrix character segments 1-3, 2-3, 3-3, 4-3, 5-3 |
| 0x37, 0x38, 0x39, 0x3A, 0x3B | 63, 64, 65, 66, 67                        | 5 × 7 matrix character segments 1-4, 2-4, 3-4, 4-4, 5-4 |
| 0x3C, 0x3D, 0x3E, 0x3F, 0x40 | 68, 69, 70, 71, 72                        | 5 × 7 matrix character segments 1-5, 2-5, 3-5, 4-5, 5-5 |
| 0x41, 0x42, 0x43, 0x44, 0x45 | 73, 74, 75, 76, 77                        | 5 × 7 matrix character segments 1-6, 2-6, 3-6, 4-6, 5-6 |
| 0x46, 0x47, 0x48, 0x49, 0x4A | 78, 79, 80, 81, 82                        | 5 × 7 matrix character segments 1-7, 2-7, 3-7, 4-7, 5-7 |
| 0x4B                         | 83                                        | 5 × 7 matrix character segment DP                       |
| 0x4C, 0x4D, 0x4E, 0x4F, 0x50 | 84, 85, 86, 87, 88                        | 5 × 7 matrix character segments 1-1, 2-1, 3-1, 4-1, 5-1 |
| 0x51, 0x52, 0x53, 0x54, 0x55 | 89, 90, 91, 92, 93                        | 5 × 7 matrix character segments 1-2, 2-2, 3-2, 4-2, 5-2 |
| 0x56, 0x57, 0x58, 0x59, 0x5A | 94, 95, 96, 97, 98                        | 5 × 7 matrix character segments 1-3, 2-3, 3-3, 4-3, 5-3 |
| 0x5B, 0x5C, 0x5D, 0x5E, 0x5F | 99, 100, 101, 102, 103                    | 5 × 7 matrix character segments 1-4, 2-4, 3-4, 4-4, 5-4 |
| 0x60, 0x61, 0x62, 0x63, 0x64 | 104, 105, 106, 107, 108                   | 5 × 7 matrix character segments 1-5, 2-5, 3-5, 4-5, 5-5 |
| 0x65, 0x66, 0x67, 0x68, 0x69 | 109, 110, 111, 112, 113                   | 5 × 7 matrix character segments 1-6, 2-6, 3-6, 4-6, 5-6 |
| 0x6A, 0x6B, 0x6C, 0x6D, 0x6E | 114, 115, 116, 117, 118                   | 5 × 7 matrix character segments 1-7, 2-7, 3-7, 4-7, 5-7 |
| 0x6F                         | 119                                       | 5 × 7 matrix character segment DP                       |
| 0x70                         | 124                                       | Cursor segment for digits 0 to 47, 1st row              |
| 0x71                         | 125                                       | Cursor segment for digits 0 to 47, 2nd row              |
| 0x72 to 0x79                 | 127                                       | No action                                               |

**Table 32. Setting Output Map Address Pointer**

| MODE                                                                                                            | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    |
|-----------------------------------------------------------------------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|
|                                                                                                                 |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Set output map address to minimum (0x00) with data 0x80. (Note that this address is set as a power-up default.) | 0x06            | 1             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Set output map address to maximum 0x79 with data 0xF9.                                                          | 0x06            | 1             | 1  | 1  | 1  | 1  | 0  | 0  | 1  |

**Table 33. Writing Output Map Data**

| MODE                                                                                                                                     | COMMAND ADDRESS | REGISTER DATA |                           |    |    |    |    |    |    |
|------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------|---------------------------|----|----|----|----|----|----|
|                                                                                                                                          |                 | D7            | D6                        | D5 | D4 | D3 | D2 | D1 | D0 |
| Write output map data; output map address pointer is autoincremented after the output map data has been written to the current location. | 0x06            | 0             | 7 bits of output map data |    |    |    |    |    |    |

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**Table 34. Reading Output Map Data**

| MODE                                                                                                                                   | COMMAND ADDRESS | REGISTER DATA |                           |    |    |    |    |    |    |  |
|----------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------|---------------------------|----|----|----|----|----|----|--|
|                                                                                                                                        |                 | D7            | D6                        | D5 | D4 | D3 | D2 | D1 | D0 |  |
| Read output map data; output map address pointer is autoincremented after the output map data has been read from the current location. | 0x06            | 0             | 7 bits of output map data |    |    |    |    |    |    |  |

**Table 35. Filament Bridge Driver Timing**

| TIMING POINT                          | PHASE1 BEHAVIOR              | PHASE2 BEHAVIOR              | EXAMPLE 1 DUTY = 1 (MIN)  | EXAMPLE 2 DUTY = 100      | EXAMPLE 3 DUTY = 198      |
|---------------------------------------|------------------------------|------------------------------|---------------------------|---------------------------|---------------------------|
| (A)                                   | Low for (199 - FilOn) cycles | Low for (199 - FilOn) cycles | 198                       | 99                        | 1                         |
| (B)                                   | Low for (FilOn) cycles       | High for (FilOn) cycles      | 1                         | 100                       | 198                       |
| (C)                                   | Low for (2) cycles           | Low for (2) cycles           | 2                         | 2                         | 2                         |
| (D)                                   | High for (FilOn) cycles      | Low for (FilOn) cycles       | 1                         | 100                       | 198                       |
| (E)                                   | Low for (199 - FilOn) cycles | Low for (199 - FilOn) cycles | 198                       | 99                        | 1                         |
| <b>Total 4MHz cycles (OSC = 4MHz)</b> | <b>400 cycles = 100µs</b>    | <b>400 cycles = 100µs</b>    | <b>400 cycles = 100µs</b> | <b>400 cycles = 100µs</b> | <b>400 cycles = 100µs</b> |

**Table 36. Filament Duty-Cycle Register Format**

| FILAMENT DUTY CYCLE                   | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|---------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                       |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| Minimum setting example (01)          | 0x09            | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0x01     |
| Maximum setting example (199 or 0xC7) | 0x09            | 1             | 1  | 0  | 0  | 0  | 1  | 1  | 1  | 0xC7     |

**Table 37. PHASE1 Register Format**

| PHASE1 BEHAVIOR                                                            | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|----------------------------------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                                                            |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| General-purpose output, logic 0.<br><b>This is the power-up condition.</b> | 0x0A            | X             | X  | X  | X  | X  | X  | 0  | 0  | 0xX0     |
| General-purpose output, logic 1.                                           | 0x0A            | X             | X  | X  | X  | X  | X  | 0  | 1  | 0xX1     |
| Output gives blink status:<br>zero if blink phase P0; 1 if blink phase P1. | 0x0A            | X             | X  | X  | X  | X  | X  | 1  | 0  | 0xX2     |
| Filament drive PHASE1 (logic 0 during shutdown).                           | 0x0A            | X             | X  | X  | X  | X  | X  | 1  | 1  | 0xX3     |

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**Table 38. PHASE2 Register Format**

| PHASE2 BEHAVIOR                                                            | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|----------------------------------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                                                            |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| General-purpose output, logic 0.<br><b>This is the power-up condition.</b> | 0x0B            | X             | X  | X  | X  | X  | X  | 0  | 0  | 0xX0     |
| General-purpose output, logic 1.                                           | 0x0B            | X             | X  | X  | X  | X  | X  | 0  | 1  | 0xX1     |
| Output gives blink status: zero if blink phase P0; 1 if blink phase P1.    | 0x0B            | X             | X  | X  | X  | X  | X  | 1  | 0  | 0xX2     |
| Filament drive PHASE2 (logic 0 during shutdown).                           | 0x0B            | X             | X  | X  | X  | X  | X  | 1  | 1  | 0xX3     |

**Table 39. PORT0 Register Format**

| PORT0 PORT BEHAVIOR                                                        | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|----------------------------------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                                                            |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| General-purpose output, logic 0.<br><b>This is the power-up condition.</b> | 0x0C            | X             | X  | X  | X  | X  | 0  | 0  | 0  | 0xX0     |
| General-purpose output, logic 1.                                           | 0x0C            | X             | X  | X  | X  | X  | 0  | 0  | 1  | 0xX1     |
| Output gives blink status: zero if blink phase P0; 1 if blink phase P1.    | 0x0C            | X             | X  | X  | X  | X  | 0  | 1  | 0  | 0xX2     |
| Output blink status: 1 if blink phase P0; zero if blink phase P1.          | 0x0C            | X             | X  | X  | X  | X  | 0  | 1  | 1  | 0xX3     |
| 625Hz square-wave output zero in shutdown.                                 | 0x0C            | X             | X  | X  | X  | X  | 1  | 0  | 0  | 0xX4     |
| 1250Hz square-wave output zero in shutdown.                                | 0x0C            | X             | X  | X  | X  | X  | 1  | 0  | 1  | 0xX5     |
| 2500Hz square-wave output zero in shutdown.                                | 0x0C            | X             | X  | X  | X  | X  | 1  | 1  | 0  | 0xX6     |
| Output gives shutdown status: zero if shutdown mode; 1 if operating mode.  | 0x0C            | X             | X  | X  | X  | X  | 1  | 1  | 1  | 0xX7     |



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**Table 40. PORT1 Register Format**

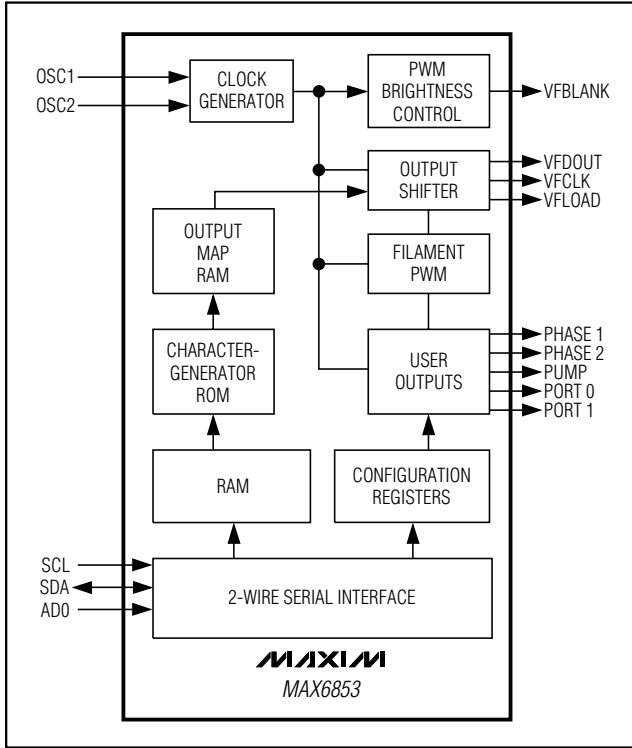
| PORT1 PORT BEHAVIOR                                                                | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|------------------------------------------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                                                                    |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| General-purpose output, logic 0.                                                   | 0x0D            | X             | X  | X  | X  | X  | 0  | 0  | 0  | 0xX0     |
| General-purpose output, logic 1.<br><b>This is the power-up condition.</b>         | 0x0D            | X             | X  | X  | X  | X  | 0  | 0  | 1  | 0xX1     |
| Output gives blink status: zero if blink phase P0; 1 if blink phase P1.            | 0x0D            | X             | X  | X  | X  | X  | 0  | 1  | 0  | 0xX2     |
| Output blink status: 1 if blink phase P0; zero if blink phase P1.                  | 0x0D            | X             | X  | X  | X  | X  | 0  | 1  | 1  | 0xX3     |
| Inverted 625Hz square-wave output 1 in shutdown.                                   | 0x0D            | X             | X  | X  | X  | X  | 1  | 0  | 0  | 0xX4     |
| Inverted 1250Hz square-wave output 1 in shutdown.                                  | 0x0D            | X             | X  | X  | X  | X  | 1  | 0  | 1  | 0xX5     |
| Inverted 2500Hz square-wave output 1 in shutdown.                                  | 0x0D            | X             | X  | X  | X  | X  | 1  | 1  | 0  | 0xX6     |
| Output gives inverted shutdown status: 1 if shutdown mode; zero if operating mode. | 0x0D            | X             | X  | X  | X  | X  | 1  | 1  | 1  | 0xX7     |

**Table 41. PUMP Register Format**

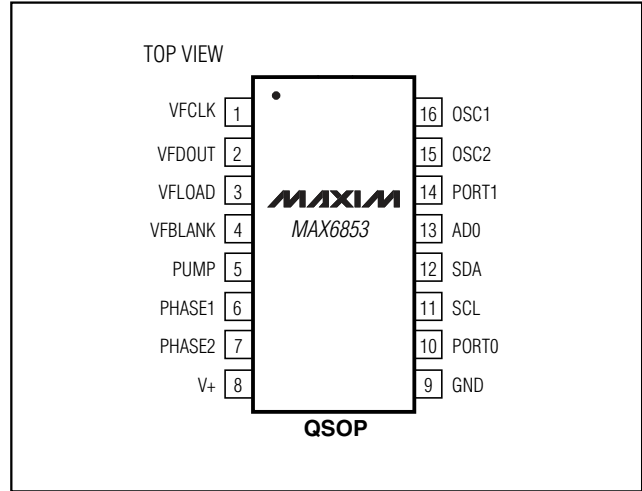
| PUMP PORT BEHAVIOR                                                         | COMMAND ADDRESS | REGISTER DATA |    |    |    |    |    |    |    | HEX CODE |
|----------------------------------------------------------------------------|-----------------|---------------|----|----|----|----|----|----|----|----------|
|                                                                            |                 | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| General-purpose output, logic 0.<br><b>This is the power-up condition.</b> | 0x08            | X             | X  | X  | X  | X  | X  | 0  | 0  | 0xX0     |
| General-purpose output, logic 1.                                           | 0x08            | X             | X  | X  | X  | X  | X  | 0  | 1  | 0xX1     |
| 80kHz square-wave output (OSC = 4MHz)<br>(logic 0 during shutdown).        | 0x08            | X             | X  | X  | X  | X  | X  | 1  | 0  | 0xX2     |
| 80kHz square-wave output (OSC = 4MHz)<br>(logic 1 during shutdown).        | 0x08            | X             | X  | X  | X  | X  | X  | 1  | 1  | 0xX3     |

# 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

**Functional Diagram**



**Pin Configuration**



**Chip Information**

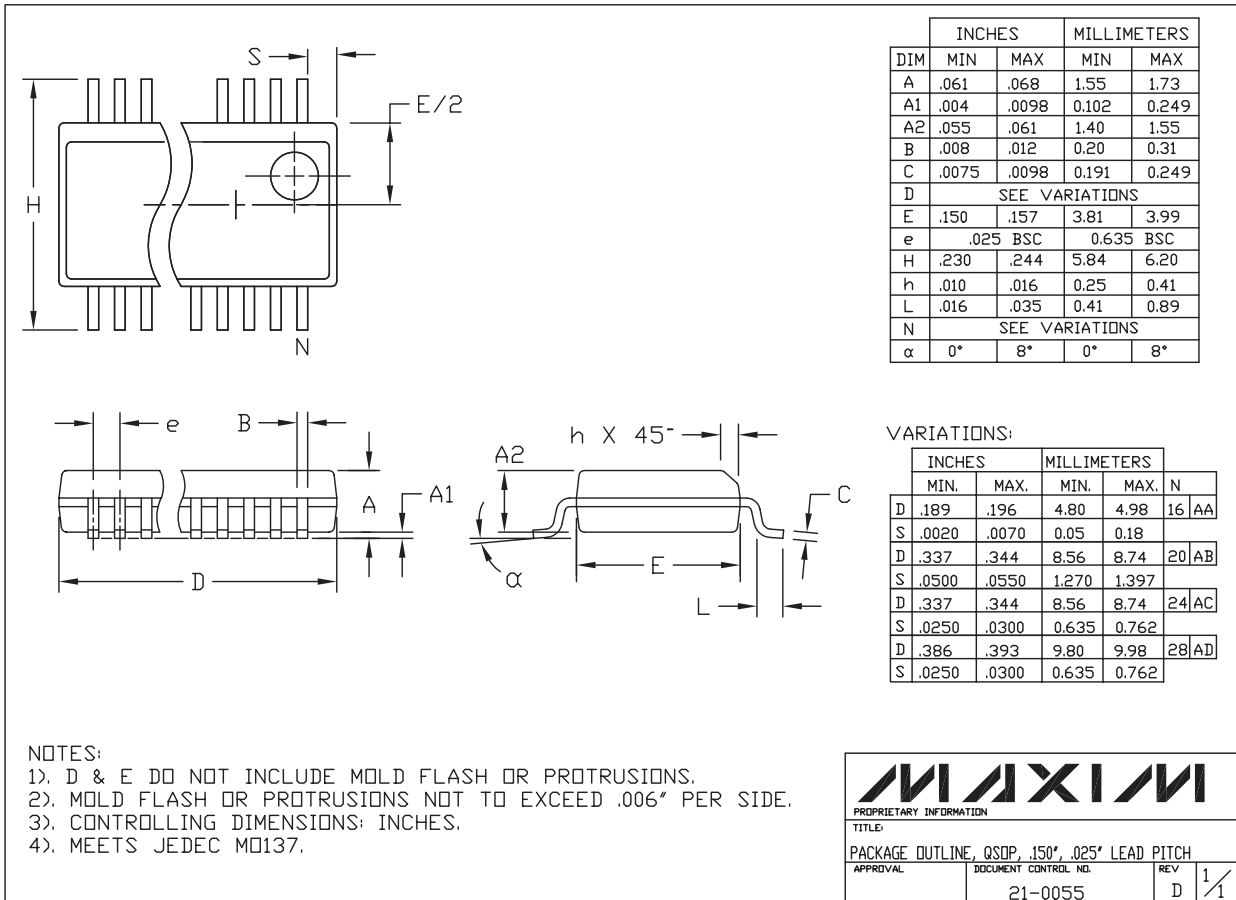
TRANSISTOR COUNT: 199,083  
 PROCESS: CMOS

# 2-Wire Interfaced, 5 × 7 Matrix Vacuum-Fluorescent Display Controller

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

**MAX6853**



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