User's Guide
SLUU266–January 2007

Using the TPS40040EVM-001: A 12-V Input, 1.8-V Output, 10-A Synchronous Buck Converter

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1 Introduction

The TPS40040EVM-001 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.8-V output at up to 10 A from a 5-V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for startup. The module uses the TPS40040 reduced pin count, low-voltage, synchronous buck controller.

1.1 Description

TPS40040EVM-001 is designed to use a regulated 5-V (4.5 V to 5.5 V) bus to produce a regulated 1.8-V output at up to 10 A of load current. The TPS40040EVM-001 is designed to demonstrate the TPS40040 in a typical 5-V bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40040 in a given application. The EVM can be modified to support output voltages from 0.9 V to 3.3 V by changing a single set resistor.

1.2 Applications

- Non-isolated medium current point of load and low-voltage bus converters.
- Networking equipment
- Telecommunications equipment
- Computer peripherals
- Digital set top box

1.3 Features

- 4.5-V to 5.5-V input range
- 1.8-V fixed output, adjustable with single resistor
- 10-Adc steady-state output current
- 300-kHz switching frequency (fixed by TPS40040)
- Single main switch MOSFET for both main switch and synchronous rectifier
- Double-sided 2 active layer PCB with all components on top side
- Active converter area of less than 1.5 in.^{2} (i.e., <1.4 in. × 1.0 in.)
- Convenient test points for probing switching waveforms and noninvasive loop response testing

2 TPS40040EVM-001 Electrical Performance Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		4.5	5	5.5	V
I_{IN}	Input current	V_{IN} = Min, I_{OUT} = Max		4.4	4.8	A
	No-load input current	V_{IN} = NOM, I_{OUT} = 0 A		100	130	mA
VIN_UVLO	Input UVLO	I_{OUT} = Min to Max	1.95	2.05	2.15	V
VIN_OV	Input OV	I_{OUT} = Min to Max		NA		V
OUTPUT CHARACTERISTICS						
VOUT	Output voltage	VIN = NOM, IOUT = NOM	1.86	1.8	1.84	V
	Line regulation	V_{IN} = Min to Max, I_{OUT} = NOM			0.5%	
	Load regulation	V_{IN} = NOM, I_{OUT} = Min to Max			0.5%	
VOUT_ripple	Output voltage ripple	VIN = Nom, IOUT = Max			40	mVpp
IOUT	Output load current	V_{IN} = Min to Max	0	6	10	A
IOCP	Output over current inception point	VIN = Nom, VOUT = VOUT–5%				A
VOVP	Output OVP	IOUT = Min to Max		NA		V
	Transient Response					
ΔI	Load step	0.75 × IOUT_Max to 0.25 × IOUT_Max		5		A
	Load slew rate			5		A/µs
	Overshoot				50	mV
	Settling time					ms
SYSTEM CHARACTERISTICS						
FSW	Switching frequency		250	300	350	kHz
ηpk	Peak efficiency	VIN = Nom, I_{OUT} = Min to Max		93%		
η	Full-load efficiency	VIN = Nom, I_{OUT} = Max		91%		
Top	Operating temperature range	VIN = Min to Max, IOUT = Min to Max	–40	25	60	°C
MECHANICAL CHARACTERISTICS						
W	Dimensions (Active Area)	Width		1.4		inch
L		Length		1		inch

3 Schematic

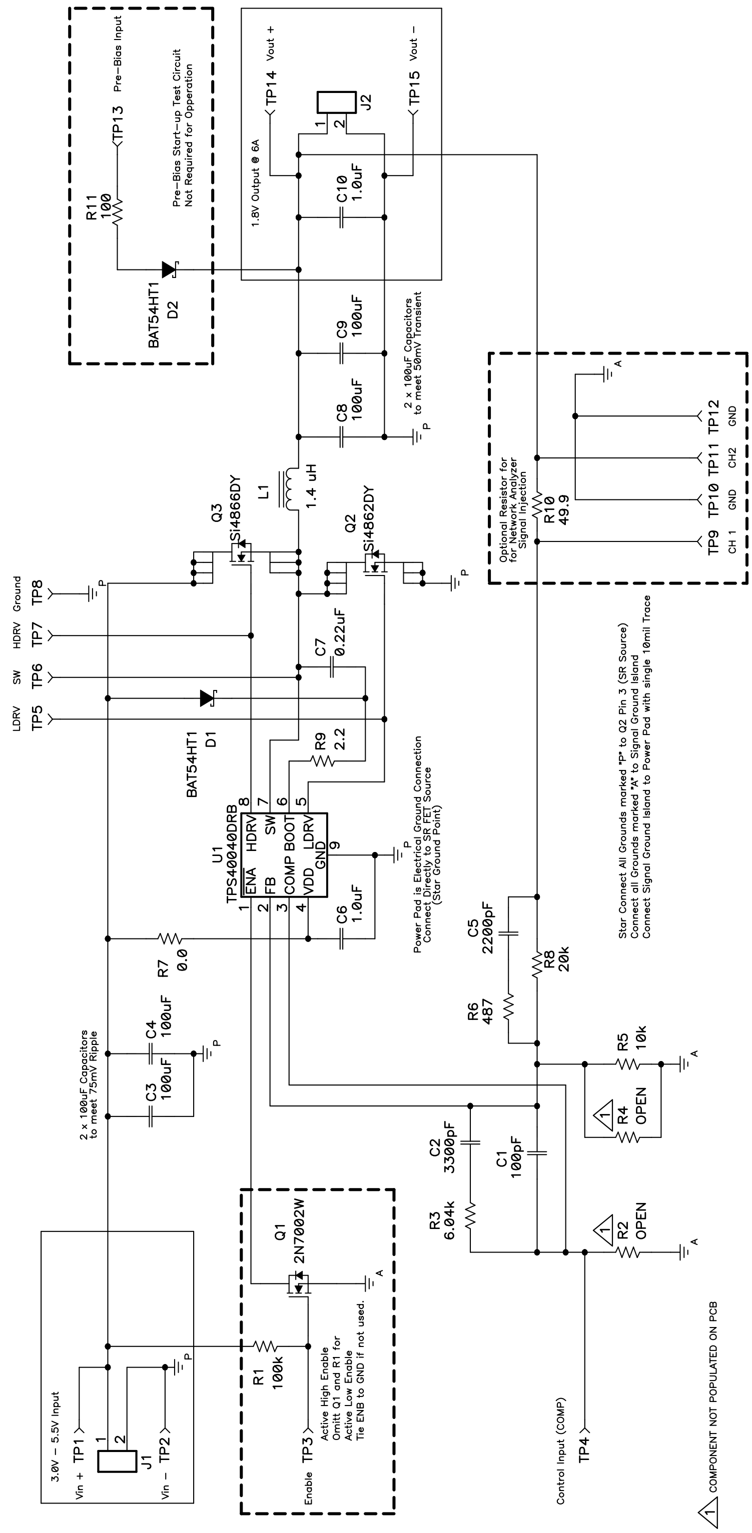

Figure 1. TPS40040EVM-001 Power Stage/Control Schematic Reference Only, See Table 4: Bill of Materials for Specific Values

3.1 Adjusting Output Voltage (R5)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R5). The output voltage is given by the formula

$$V_{VOUT} = V_{VREF} \times \frac{R8 + R5}{R5} \quad (1)$$

Where V_{VREF} = 0.600 V and R8 = 20 kΩ

Table 1 contains common values for R5 to generate popular output voltages. TPS40040EVM-001 is stable through these output voltages but the efficiency can suffer as the power stage is optimized for the 1.8-V output.

Table 1. Adjusting V_{OUT} With R7

V_{OUT} (V)	R5 (kΩ)
2.5	3.64
2.25	7.32
2.0	8.66
1.8	10
1.5	13.3
1.2	20
1.0	30
0.9	40

The values in Table 1 provide less than 1% nominal set-point error in the output voltage. If a tighter nominal value is required, R4 can be used in parallel with R5 to obtain a wider range of resistor values using commonly available E96 resistors.

3.2 Adjusting Short-Circuit Protection (R2)

The TPS40040 uses a selectable current limit for short-circuit protection. The current limit is selected from three levels by placing a resistor at R2. The TPS40040 compares the voltage drop across the high-side FET (VDD to SW) to an internal reference voltage selected during start-up. The voltage levels are shown in Table 2.

Table 2. Adjusting V_{SCP} With R9

V_{SCP} (mV)	R2 (kΩ)
105	402
180	OPEN
300	12

The current before declaring short-circuit protection can be determined by dividing the V_{SCP} by the $R_{DS(ON)}$ of the high-side FET (Q2).

3.3 Test Point Descriptions

Table 3. Test Point Descriptions

TEST POINT	LABEL	USE	SECTION
TP1	Vin+	Monitor input voltage to the module	3.3.1
TP2	Vin–	Monitor input voltage to the module	3.3.1
TP3	Enable	Active-high enable – pull to ground to disable	3.3.2
TP4	COMP	Monitor COMP voltage	3.3.2
TP5	LDRV	Monitor low-side gate drive (Q3)	NA

Table 3. Test Point Descriptions (continued)

TEST POINT	LABEL	USE	SECTION
TP6	SW	Monitor switch node	3.3.3 and 3.3.5
TP7	HDRV	Monitor high-side gate drive (Q2)	3.3.4
TP8	GND	Ground point for LDRV, SW, and HDRV probes	3.3.4
TP9	CH1	Loop injection point and iInjection monitoring point	3.3.4
TP10	GND	Ground for loop monitoring probe	3.3.4
TP11	CH2	Loop injection point and output response monitoring point	3.3.5
TP12	GND	Ground for loop monitoring probe	3.3.5
TP13	Pre-Bias	Injection point to test prebias load compliance	3.3.5
TP14	Vout	Monitor output voltage from the module	3.3.5
TP15	GND	Monitor output voltage from the module	3.3.6

3.3.1 Input Voltage Monitoring (TP1 and TP2)

TPS40040EVM-001 provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connector losses. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and negative terminal to TP2.

3.3.2 Disable (TP3)

TPS40040EVM-001 defaults to the Enabled state. Short TP3 to ground to disable the TPS40040 controller. TP4 also can be used as a disable input driven by a 5-V logic input from an external circuit. The Enable test point uses a 100-kΩ pullup resistor so that the TPS40040EVM-001 turns on if the Enable test point is left floating.

3.3.3 Compensation and Initialization (TP4)

TPS40040EVM-001 provides a test-point connection to the COMP pin of the TPS40040 controller. This test point can be used to monitor the COMP voltage during the controller's Power On initialization that sets the controllers short-circuit protection (SCP) threshold. The test point also can be used to monitor the PWM comparator input voltage (COMP) during operation or to measure the power stage gain by following the loop analysis directions by moving the channel A probe from TP10 to TP6.

3.3.4 Switching Waveforms (TP5, TP6, TP7, and TP8)

TPS40040EVM-001 provides three test points and a local ground connection (TP8) for the monitoring of the main switching waveforms. Connect an oscilloscope probe to TP7 to monitor the high-side gate drive applied to the gate of Q2. Connect an oscilloscope probe to TP6 to monitor the switch node voltage. The gate-to-source voltage (VGS) of the high-side FET can be determined by an oscilloscope math function TP7–TP6, if both channels use the same scale. Connect an oscilloscope probe to TP5 to monitor the low-side gate drive applied to the gate of Q3. Because the source of Q3 is connected directly to ground, no math function is required to determine the gate-to-source voltage of the low-side FET.

3.3.5 Loop Analysis (TP9, TP10, TP11, and TP12)

TPS40040EVM-001 contains a 49.9-Ω series resistor in the feedback loop to allow for matched impedance signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (30-mV or less) signal across R10 through TP9 and TP11. By monitoring the AC injection level at TP9 and the returned AC level at TP11, the power-supply loop response can be determined.

By moving channel A from TP9 to TP4 (COMP), the control-to-output response of the power stage (also referred to as the power stage transfer function) can be directly measured. See Section 3.9 for a detailed procedure of loop response measurements.

3.3.6 Prebias Input (TP13)

TPS40040EVM-001 contains a prebias injection circuit with 100-Ω resistor and series diode to allow testing and evaluation of the TPS40040's prebias support compatibility. Apply a voltage less than the target output voltage to TP13. Monitoring the output voltage during start-up demonstrates the TPS40040's ability to power up without drawing current from a prebiased output. D2 prevents the output voltage from back-driving the prebias source.

3.3.7 Output Voltage Monitoring (TP14 and TP15)

TPS40040EVM-001 provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connector losses. All output voltage measurements should be made between TP14 and TP15. To use TP14 and TP15, connect a voltmeter positive terminal to TP14 and negative terminal to TP15. For output ripple measurements, TP14 and TP15 allow a user to limit the ground loop area by using the Tip and Barrel measurement technique shown in Figure 3. All output ripple measurements should be made using the Tip and Barrel measurement.

4 Test Setup

4.1 Equipment

4.1.1 Voltage Source

V_{IN}
The input voltage source (V_{IN}) should be a 0-V to 6-V variable DC source capable of 5 Adc. Connect V_{IN} to J1 as shown in Figure 3.

4.1.2 Meters

- A1: 0-A to 5-A dc ammeter
- V1: V_{IN}, 0-V to 6-V voltmeter
- V2: V_{OUT} 0-V to 5-V voltmeter

4.1.3 Loads

LOAD1
The output load (LOAD1) should be an electronic constant-current mode load capable of 0-A to 10-A dc at 1.8 V.

4.1.4 Oscilloscope

OSCILLOSCOPE
A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 1-µs/division horizontal resolution, 10-mV/division vertical resolution for taking output ripple measurements. TP15 and TP16 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP15 and holding the ground barrel to TP16 as shown in Figure 3. For a hands-free approach, the loop in TP16 can be cut and opened to cradle the probe barrel. Using a leaded ground connection can induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

V_{IN} to J1

The connection between the source voltage, V_{IN} and J1 of TPS40040EVM-001 can carry as much as 5 Adc. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J2 to LOAD1 (Power)

The power connection between J2 of TPS40040EVM-001 and LOAD1 can carry as much as 10 Adc. The minimum recommended wire size is 2 × AWG #16, with the total length of wire less than 2 feet (1 feet output, 1 feet return).

4.1.6 Other

FAN

This evaluation module includes components that can become hot to the touch. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of between 200–400 LFM is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed if the fan is not running.

4.2 Equipment Setup

Shown in Figure 3 is the basic test setup recommended to evaluate the TPS40040EVM-001. Note that although the return for J1 and J2 are the same, the connections should remain separate as shown in Figure 2.

4.2.1 Procedure

1. While working at an ESD workstation, the user should ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before applying power to the EVM. Electrostatic smock and safety glasses also should be worn.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 5 A maximum. Ensure that V_{IN} is initially set to 0 V and connected as shown in Figure 2.
3. Connect the ammeter A1 (0-A to 5-A range) between V_{IN} and J1 as shown in Figure 2.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
5. Connect LOAD1 to J2 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 Adc before V_{IN} is applied.
6. Connect voltmeter, V2 across TP14 and TP15 as shown inFigure 2.
7. Place fan as shown in Figure 2. and turn on, ensuring that air is flowing across the EVM.

4.2.2 Diagram

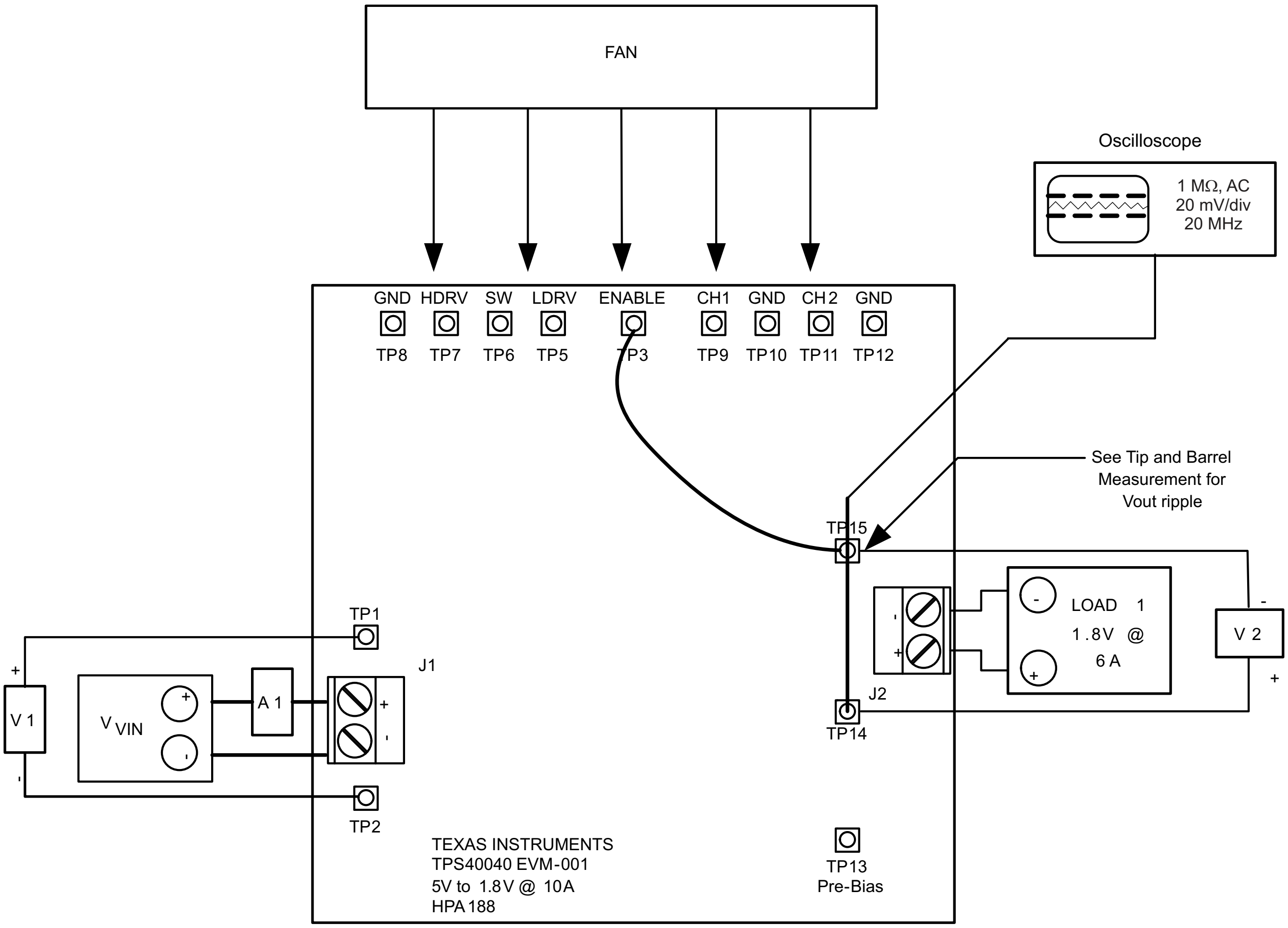

Figure 2. TPS40040EVM-001 Recommended Test Set-Up

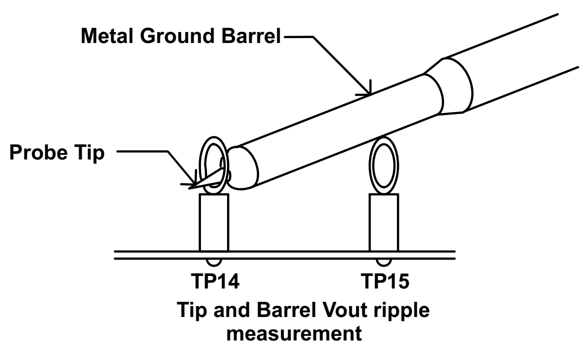

Figure 3. Output Ripple Measurement – Tip and Barrel using TP14 and TP15

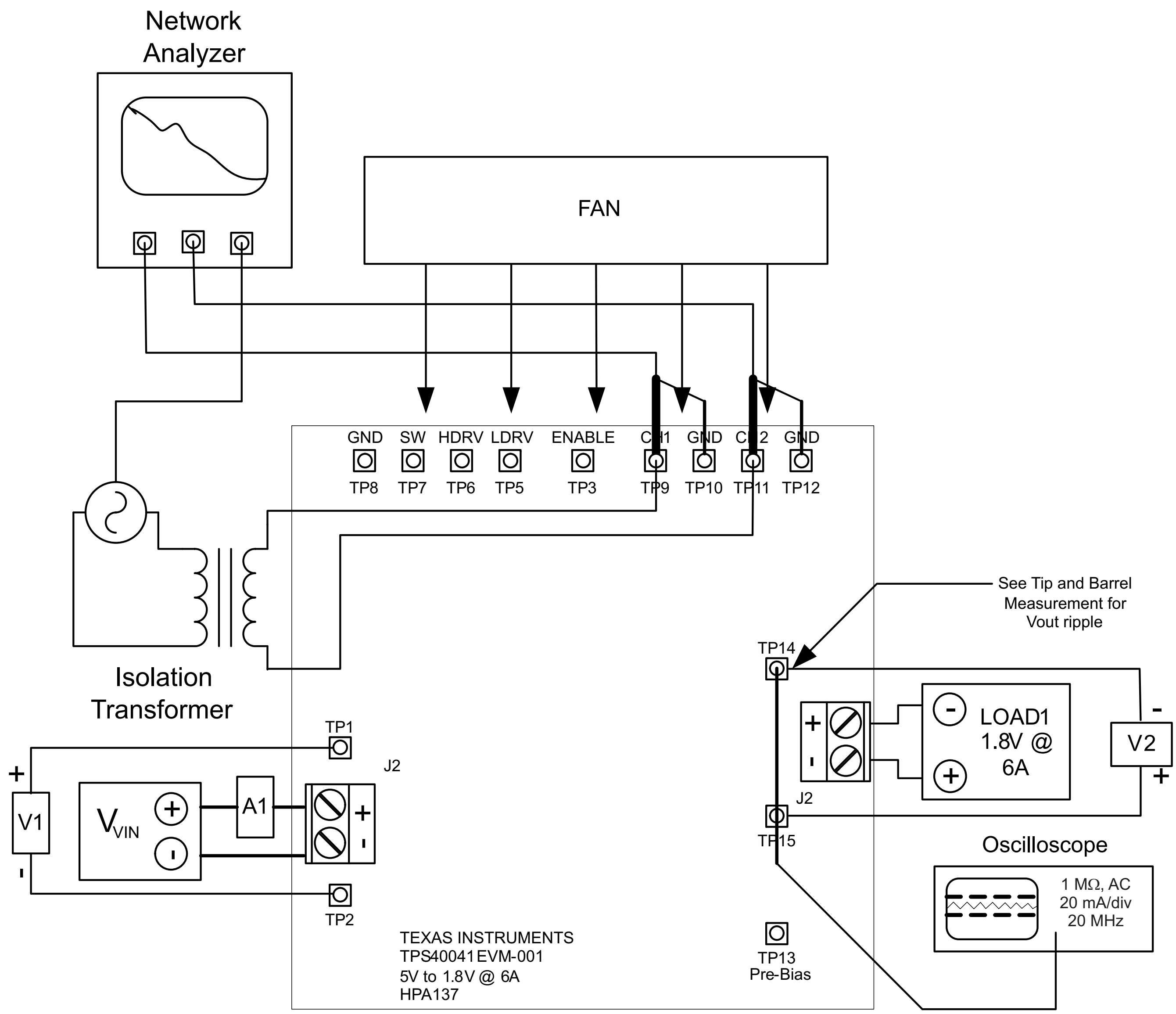

Figure 4. Control Loop Measurement Setup

4.3 *Startup/Shutdown Procedure*

1. Increase V_{IN} (V1) from 0 V to 5 Vdc.
2. Vary LOAD1 from 0 A tp 10 Adc
3. Vary V_{IN} from 4.5 Vdc to 5.5 Vdc
4. Short TP21 to TP19 to disable switching and 3-state output.
5. Decrease LOAD1 to 0 A.
6. Decrease V_{IN} to 0 Vdc.

4.4 *Output Ripple Voltage Measurement Procedure*

1. Increase VIN from 0 V to 5 Vdc.
2. Adjust LOAD1 to desired load between 0 Adc and 10 Adc.
3. Adjust V_{IN} to desired load between 4.5 Vdc and 5.5 Vdc.
4. Connect oscilloscope probe to TP15 and TP16 as shown in Figure 3.

5. Measure output ripple.
6. Decrease LOAD1 to 0 A.
7. Decrease V_{IN} to 0 Vdc.

4.5 Control Loop Gain and Phase Measurement Procedure

1. Connect 1-kHz to 1-MHz isolation transformer to TP12 and TP13 as show in Figure 4.
2. Connect input signal amplitude measurement probe (channel A) to TP12 as shown in Figure 4.
3. Connect output signal amplitude measurement probe (channel B) to TP13 as shown in Figure 4.
4. Connect ground lead of channel A and channel B to TP11 and TP14 as shown in Figure 4.
5. Increase V_{IN} from 0 V to 5 Vdc.
6. Adjust LOAD1 to desired load between 0 Adc and 10 Adc.
7. Adjust V_{IN} to desired load between 4.5 Vdc and 5.5 Vdc.
8. Inject 30-mV or less signal across R14 through isolation transformer.
9. Sweep frequency from 1 kHz to 1 MHz with 10 Hz or lower post filter.
10. Control loop gain can be measured by $20 \times \text{LOG}\left(\frac{\text{ChannelB}}{\text{ChannelA}}\right)$
11. Control loop phase is measured by the phase difference between channel A and channel B.
12. Control-to-output response (power stage transfer function) can be measured by connecting channel A probe to TP6 (COMP) and channel B probe to TP13.
13. Output-to-control response (error amplifier transfer function) can be measured by connecting channel B probe to TP6 (COMP) and channel A probe to TP12.
14. Disconnect isolation transformer from TP12 and TP13 before making other measurements (signal injection into feedback may interfere with accuracy of other measurements).
15. Decrease LOAD1 to 0 A.
16. Decrease V_{IN} to 0 Vdc.

5 TPS40040EVM Typical Performance Data and Characteristic Curves

Figure 5 and Figure 10 present typical performance curves for the TPS40040EVM-001. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

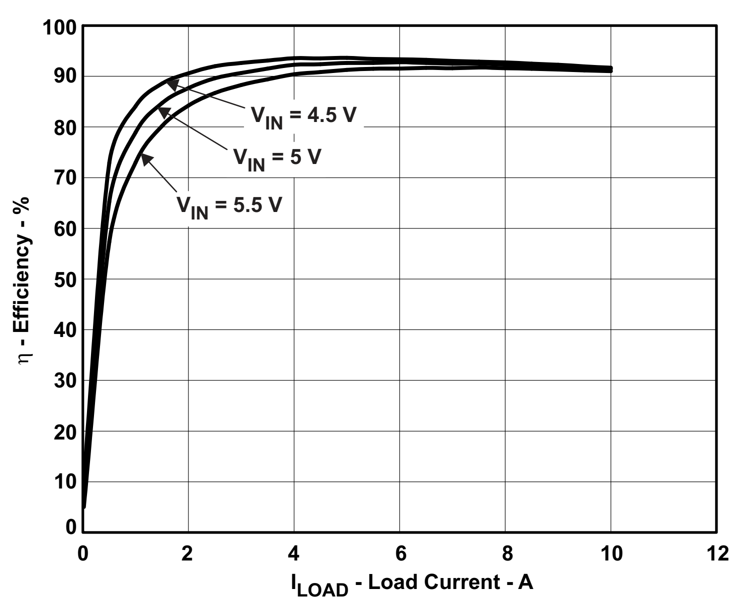

Figure 5. TPS40040EVM-001 Efficiency Curves

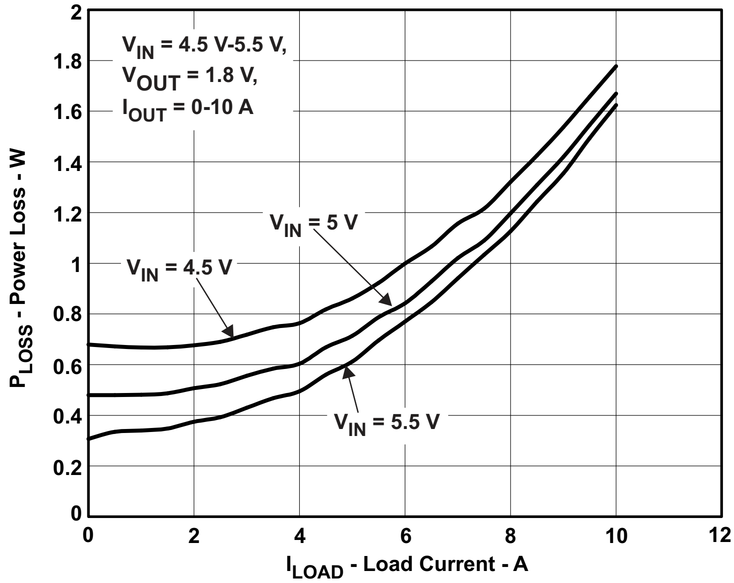

Figure 6. Power Loss – TPS40040EVM-001 Line and Load Regulation

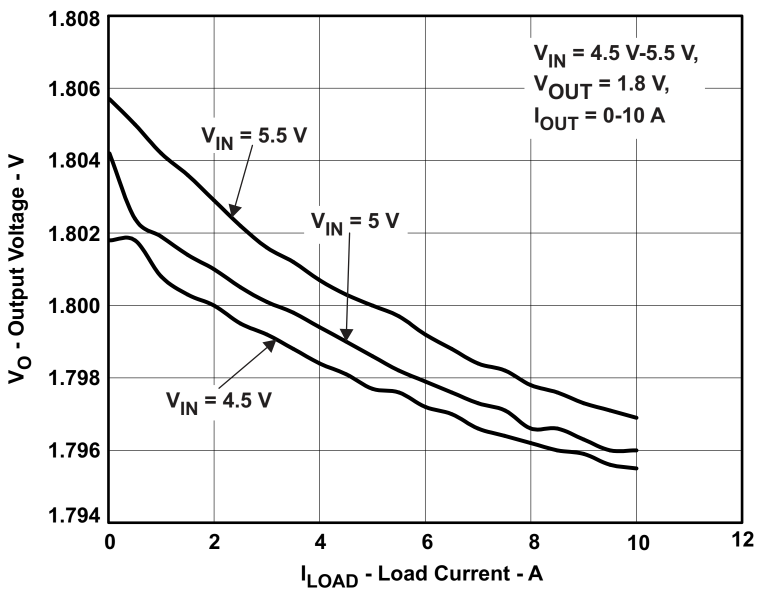

Figure 7. TPS40040EVM-001 Line and Load Regulation

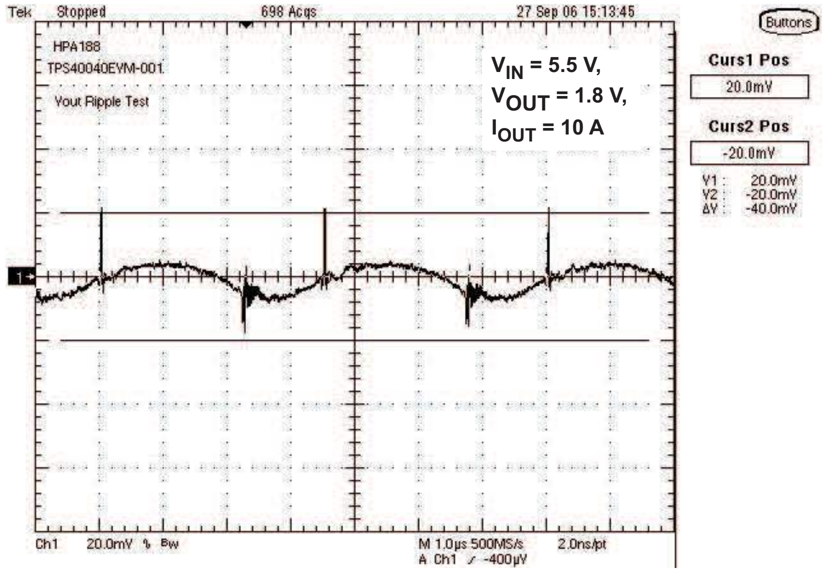

Figure 8. TPS40040EVM-001 Output Voltage Ripple

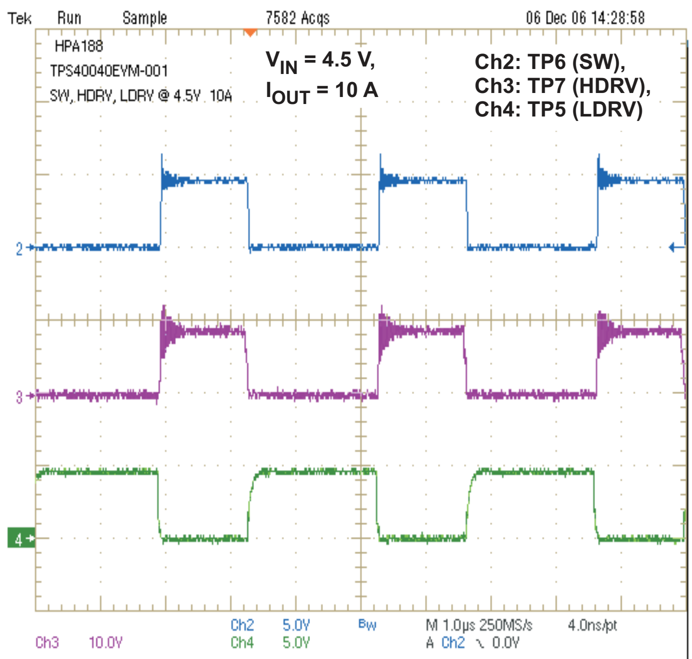

Figure 9. TPS40040EVM-001 Switch Node – Switching Waveforms

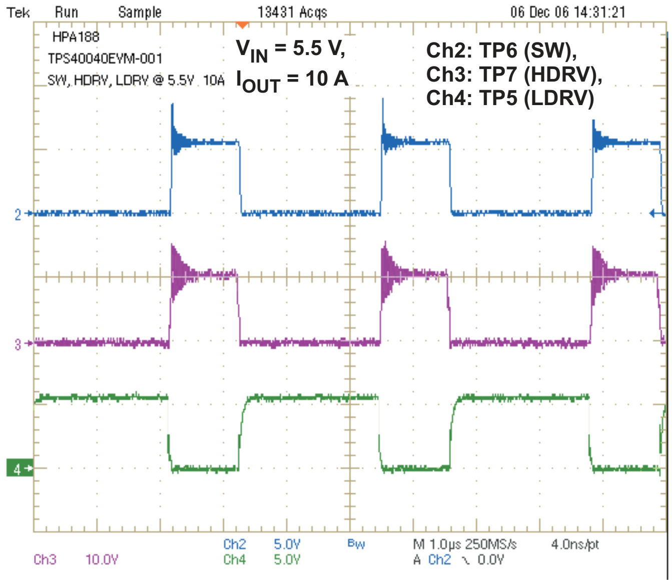

Figure 10. TPS40040EVM-001 Switching Waveforms

6 EVM Assembly Drawings and Layout

Figure 11 through Figure 13 show the design of the TPS40040EVM-001 printed-circuit board. The EVM has been designed using double-sided, 2-oz. copper-clad circuit board 2.5 in. × 2.5 in. with all components in a 1.40 in. × 1.0 in. active area on the top side to allow the user to easily view, probe, and evaluate the TPS40040 control IC in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

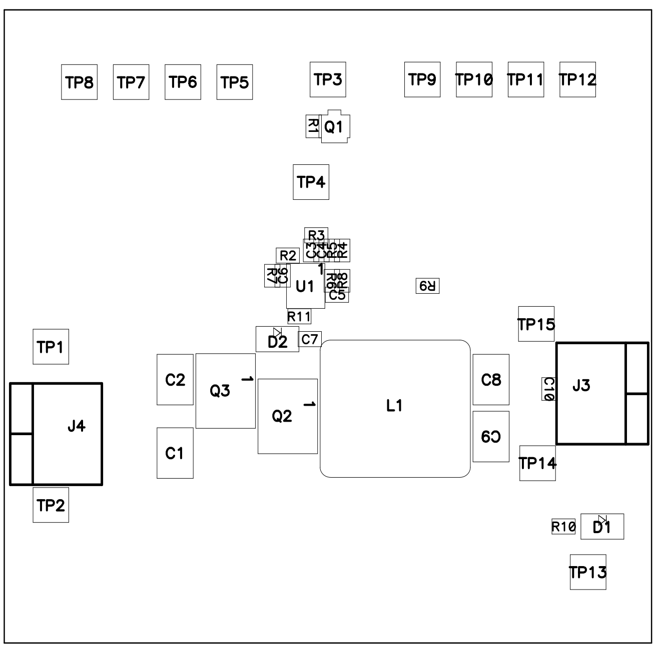

Figure 11. TPS40040EVM-001 Component Placement (Viewed From Top)

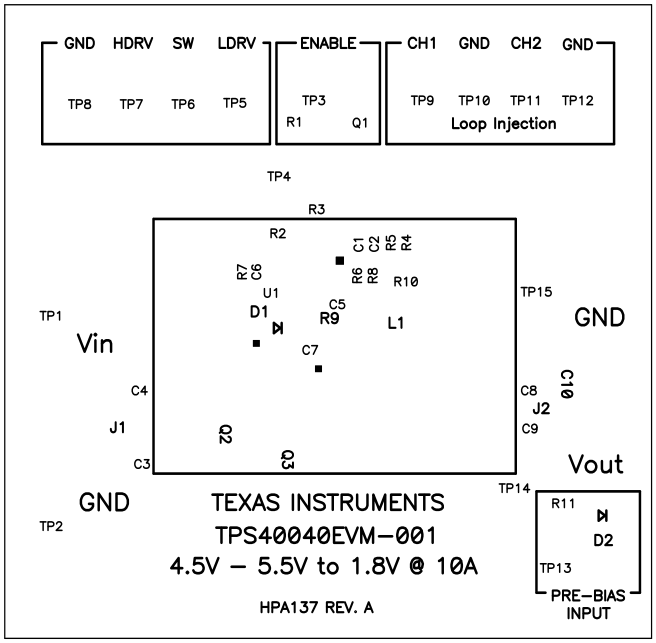

Figure 12. TPS40040EVM-001 Silkscreen (Viewed From Top)

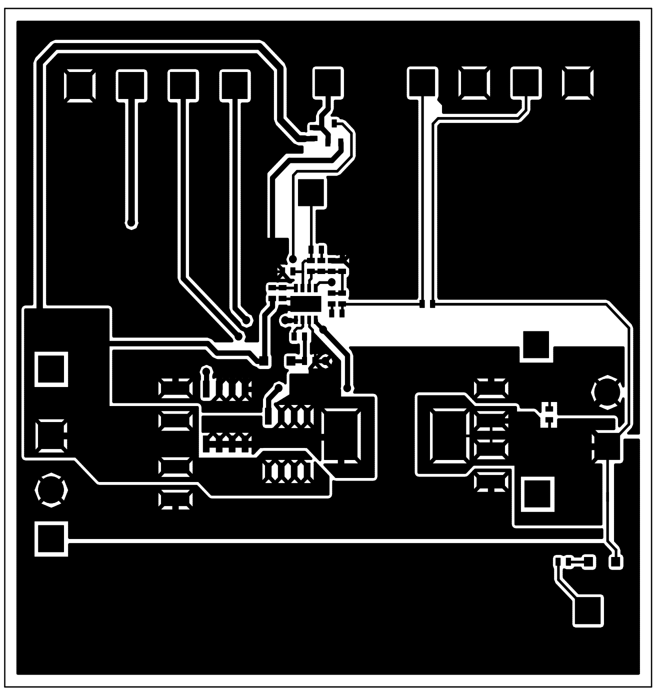

Figure 13. TPS40040EVM-001 Top Copper (Viewed From Top)

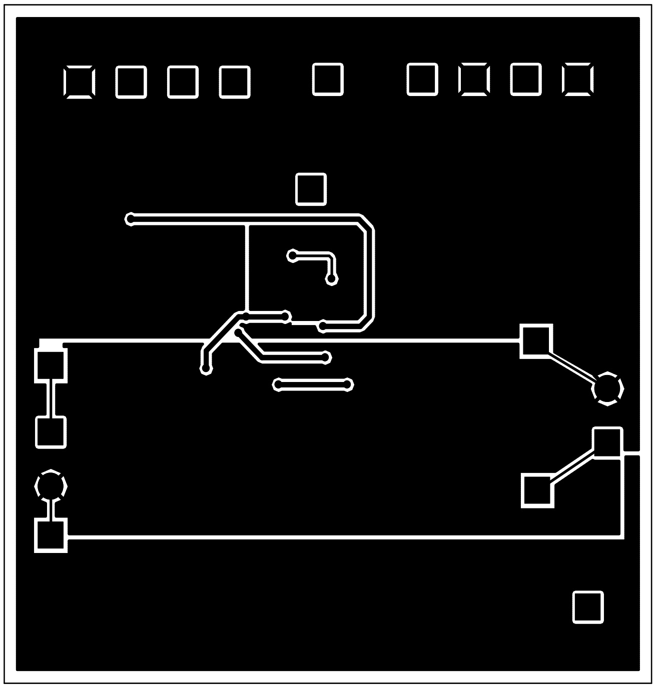

Figure 14. TPS40040EVM Bottom Copper (X-Ray View From Top)

7 List of Materials

Table 4 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 4. TPS40040EVM-001 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C1	100 pF	Capacitor, Ceramic, 50V, X7R, 20%	0402	C1005X7R1H101M	TDK
1	C2	3300 pF	Capacitor, Ceramic, 50V, X7R, 20%	0402	C1005X7R1H332M	TDK
4	C3, C4, C8, C9	100 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	C3225X5R0J107M	TDK
1	C5	2200 pF	Capacitor, Ceramic, 50V, X7R, 20%	0402	C1005X7R1H222M	TDK
2	C6, C10	1.0 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0402	C1005X5R0J105M	TDK
1	C7	0.22 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0402	C1005X5R0J224M	TDK
2	D1, D2	BAT54HT1	Diode, Schottky, 200-mA, 30-V	SOD323	BAT54HT1	On Semi
2	J1, J2	ED1609-ND	Terminal Block, 2-pin, 15-A, 5,1 mm	0.40 × 0.35 inch	ED1609	OST
1	L1	1.4 µH	Inductor, SMT, 26 A	0.512 × 0.550 inch	PG0077.142	Pulse
1	Q1	2N7002W	MOSFET, N-Ch, VDS 60V, RDS 2 Ω, ID 115 mA	SOT-323 (SC-70)	2N7002W-7	Diodes Inc
1	Q2	Si4862DY	MOSFET, N-ch, 16V, 25A, 3.3 mΩ	SO8	Si4862DY	Siliconix
1	Q3	Si4866DY	MOSFET, N-ch, 12V, 17A, 5.5 mΩ	SO8	Si4866DY	Siliconix
1	R1	100k	Resistor, Chip, 1/16W, 5%	0402	Std	Std
1	R10	49.9	Resistor, Chip, Ohms 1/16W, 5%	0402	Std	Std
1	R11	100	Resistor, Chip, 1/16W, 5%	0402	Std	Std
0	R2	OPEN	Resistor, Chip, 1/16W, 5%	0402	Std	Std
1	R3	6.04k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
0	R4	OPEN	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R5	10k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R6	487	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R7	0	Resistor, Chip, 1/16W, 5%	0402	Std	Std
1	R8	20k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R9	2.2	Resistor, Chip, 1/16W, 5%	0402	Std	Std
2	TP1, TP14	5010	Test Point, Red, Thru Hole	0.125 × 0.125	5010	
5	TP2, TP8, TP10, TP12, TP15	5011	Test Point, Black, Thru Hole	0.125 × 0.125	5011	
8	TP3–TP7, TP9, TP11, TP13	5012	Test Point, White, Thru Hole	0.125 × 0.125	5012	
1	U1	TPS40040DRB	IC, Low Voltage DC/DC Synchronous Buck Controller	QFN-8P	TPS40040DRB	TI
1	—		PCB, 2.5 In × 2.5 In × 0.062 In		HPA188	Any

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FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4.5 V to 18 V and the output voltage range of 0.6 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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