DAC-Q56DD-2Q56-XM-C

Dell® Compatible and TAA Compliant 400GBase-CU QSFP-DD 400G to 2xQSFP56 200G PAM-4 Direct Attach Cable (Passive Twinax, Up to 2.5m)

Features

- Compliant with QSFP-DD MSA Specification Rev 3.4
- SFF-8679 electrical interface compliant
- SFF-8636 management interface support
- Compatible with IEEE 802.3bj, IEEE 802.3by, IEEE 802.3cd
- Supports aggregate data rates of 100 and 400Gbps
- I2C for EEPROM communication
- Pull-to-release slide latch design
- 28AWG through 32AWG cable
- Excellent EMI/EMC performance 360-degree cable shield termination
- Advantage dual side pre-solder automated assembly technologies
- Low loss, stronger mechanical features, more flexible
- ROHS-6 Compliant

Applications

- Switches, Servers and Routers
- Data Center Networks
- Storage Area Networks
- High Performance Computing
- Telecommunications and wireless infrastructure

Product Description

This is a Dell® compatible TAA compliant 400GBase-CU QSFP-DD 400G to 2xQSFP56 200G PAM-4 direct attach cable that operates over passive copper with a maximum reach of up to 2.5m (8.2ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This direct attach cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' direct attach cables are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

Order Information

Part Number	Description
DAC-Q56DD-2Q56-1M-C	Dell® DAC-Q56DD-2Q56-1M Compatible and TAA Compliant 400GBase-CU QSFP-DD 400G to 2xQSFP56 200G PAM-4 Direct Attach Cable (Passive Twinax, 1m)
DAC-Q56DD-2Q56-2M-C	Dell® DAC-Q56DD-2Q56-2M Compatible and TAA Compliant 400GBase-CU QSFP-DD 400G to 2xQSFP56 200G PAM-4 Direct Attach Cable (Passive Twinax, 2m)
DAC-Q56DD-2Q56-2-5M-C	Dell® DAC-Q56DD-2Q56-2-5M Compatible and TAA Compliant 400GBase-CU QSFP-DD 400G to 2xQSFP56 200G PAM-4 Direct Attach Cable (Passive Twinax, 2.5m)

Regulatory Compliance

Certification	Standard
Laser Eye Safety	IEC: 60825-1, 3rd Edition FDA: CFR-21 Sections 1040.10 and 1040.11
Product Safety	TUV: EN62368-1 UL/CSA 60950-1
EMC/EMI	FCC: Part 15 sb.B EN: 55032/55024

Mechanical Characteristics

Length	Wire Gauge	Cable OD	Cable Jacket Material	Flammability Rating
1m	32 AWG	3.8mm	PVC	VW-1
2m	28AWG	4.93mm	PVC	VW-1
2.5m	28AWG	4.93mm	PVC	VW-1

Electrical Characteristics

Parameter	Specification
Impedance	100 ohm
Data Rate	56Gbps per lane (PAM4)
Voltage	3.3V DC
Current (signal application only)	0.75A
Operating Temperature	-10°C to 55°C
Storage Temperature	-10°C to 55°C
High Speed Compliant	IEEE 802.3cd

QSFP-DD to 2xQSFP Wiring Schematic

P3 QSFP-DD			P1 QSFP28	
GND	1		20	GND
TX2-	**2**	◁⟷▷	**21**	RX2-
TX2+	**3**	◁⟷▷	**22**	RX2+
GND	4		23	GND
TX4-	**5**	◁⟷▷	**24**	RX4-
TX4+	**6**	◁⟷▷	**25**	RX4+
GND	7		26	GND
ModselL	8		27	ModPrsL
ResetL	9		28	IntL
VccRx	10		29	VccTx
SCL	11		30	Vcc1
SDA	12		31	Reserved
GND	13		32	GND
RX3+	**14**	◁⟷▷	**33**	TX3+
RX3-	**15**	◁⟷▷	**34**	TX3-
GND	16		35	GND
RX1+	**17**	◁⟷▷	**36**	TX1+
RX1-	**18**	◁⟷▷	**37**	TX1-
GND	19		38	GND
GND	20		1	GND
RX2-	**21**	◁⟷▷	**2**	TX2-
RX2+	**22**	◁⟷▷	**3**	TX2+
GND	23		4	GND
RX4-	**24**	◁⟷▷	**5**	TX4-
RX4+	**25**	◁⟷▷	**6**	TX4+
GND	26		7	GND
ModPrsL	27		8	ModselL
intL	28		9	ResetL
VccTx	29		10	VccRx
Vcc1	30		11	SCL
InitMode	31		12	SDA
GND	32		13	GND
TX3+	**33**	◁⟷▷	**14**	RX3+
TX3-	**34**	◁⟷▷	**15**	RX3-
GND	35		16	GND
TX1+	**36**	◁⟷▷	**17**	RX1+
TX1-	**37**	◁⟷▷	**18**	RX1-
GND	38		19	GND

P3 QSFP-DD			P2 QSFP28	
GND	39		20	GND
TX6-	**40**	◁⟷▷	**21**	RX2-
TX6+	**41**	◁⟷▷	**22**	RX2+
GND	42		23	GND
TX8-	**43**	◁⟷▷	**24**	RX4-
TX8+	**44**	◁⟷▷	**25**	RX4+
GND	45		26	GND
Reserved	46		27	ModPrsL
VS1	47		28	IntL
VccRx1	48		29	VccTx
VS2	49		30	Vcc1
VS3	50		31	Reserved
GND	51		32	GND
RX7+	**52**	◁⟷▷	**33**	TX3+
RX7-	**53**	◁⟷▷	**34**	TX3-
GND	54		35	GND
RX5+	**55**	◁⟷▷	**36**	TX1+
RX5-	**56**	◁⟷▷	**37**	TX1-
GND	57		38	GND
GND	58		1	GND
RX6-	**59**	◁⟷▷	**2**	TX2-
RX6+	**60**	◁⟷▷	**3**	TX2+
GND	61		4	GND
RX8-	**62**	◁⟷▷	**5**	TX4-
RX8+	**63**	◁⟷▷	**6**	TX4+
GND	64		7	GND
NC	65		8	ModselL
Reserved	66		9	ResetL
VccTx1	67		10	VccRx
Vcc2	68		11	SCL
Reserved	69		12	SDA
GND	70		13	GND
TX7+	**71**	◁⟷▷	**14**	RX3+
TX7-	**72**	◁⟷▷	**15**	RX3-
GND	73		16	GND
TX5+	**74**	◁⟷▷	**17**	RX1+
TX5-	**75**	◁⟷▷	**18**	RX1-
GND	76		19	GND

QSFP-DD Pin Descriptions

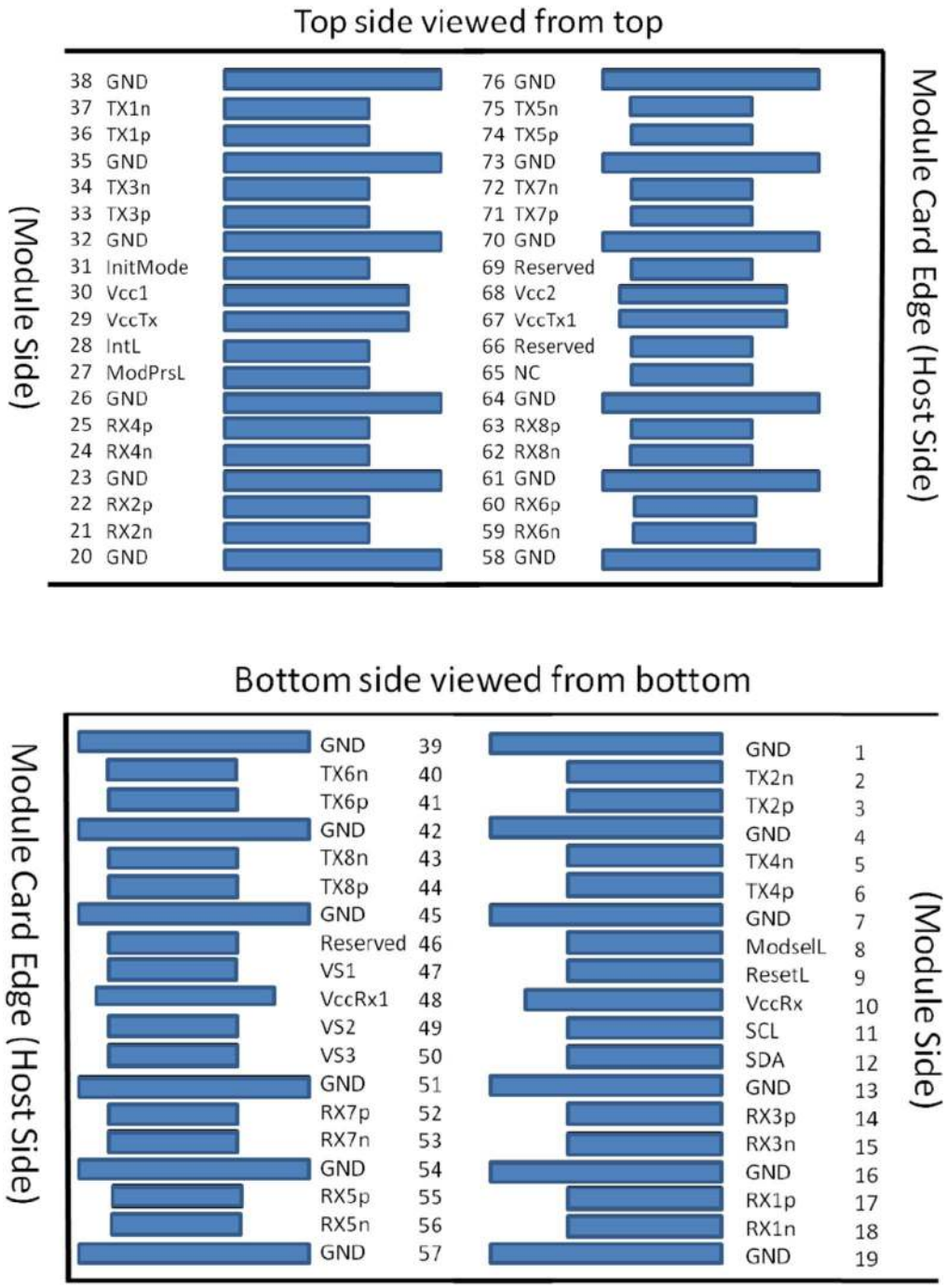
PIN	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vccl	+3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

PIN		Symbol	Description	Notes
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VSl	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

QSFP-DD Electrical Pin-out Details



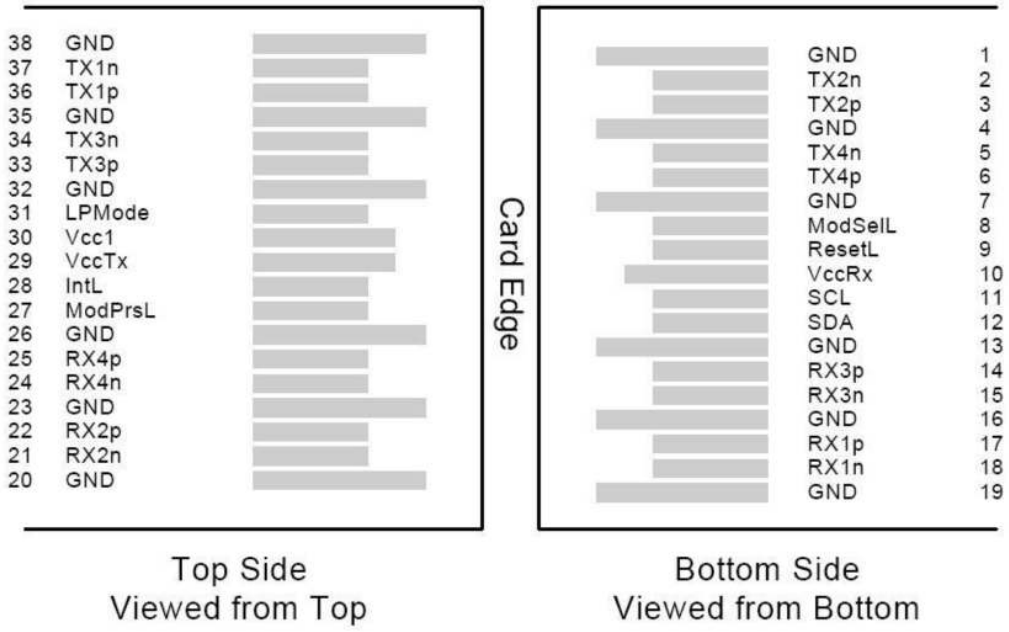
QSFP56 Pin Definitions

Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:

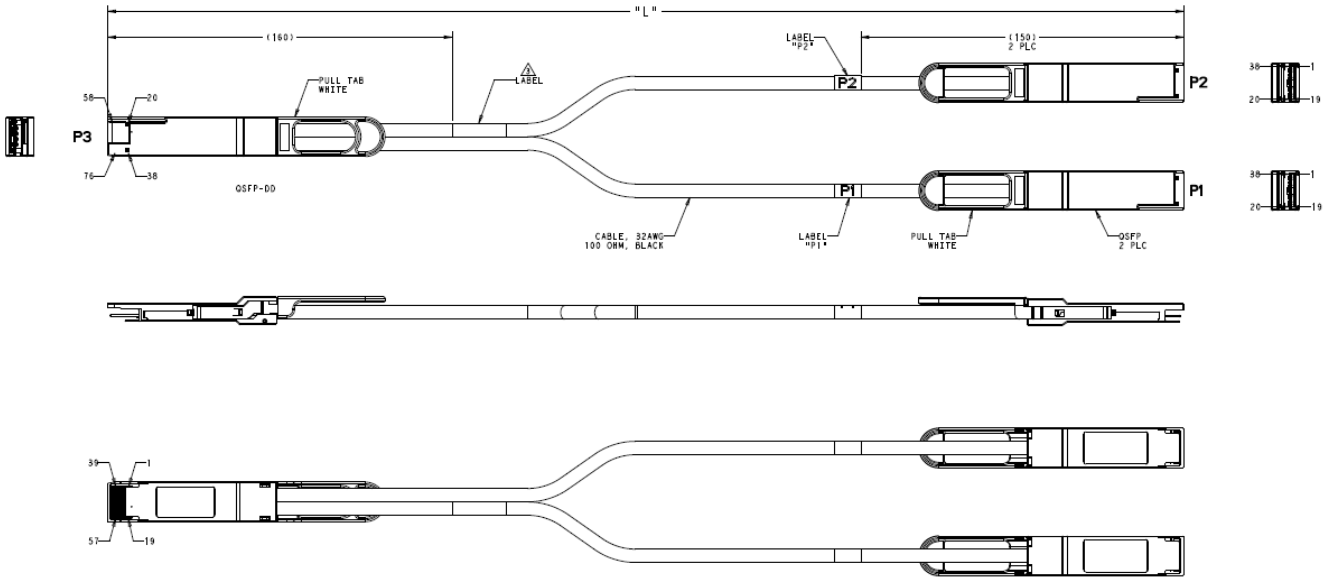
1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

QSFP56 Electrical Pin-out Details

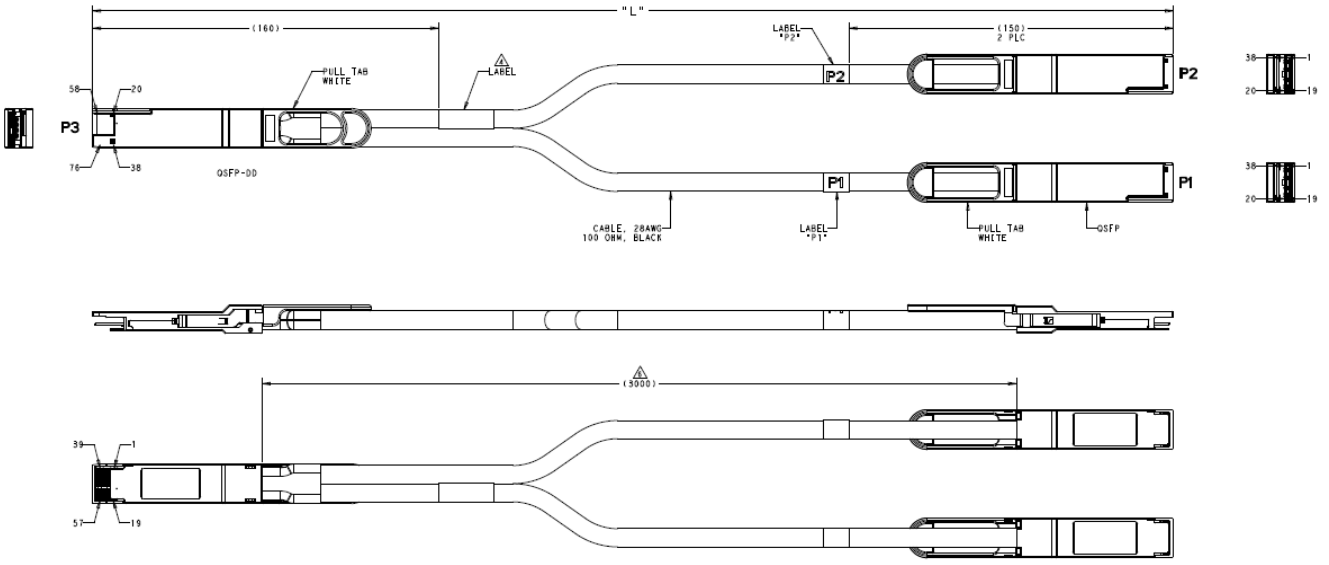


Mechanical Specifications

QSFP-DD to 2xQSFP 1m



QSFP-DD to 2xQSFP 2m, 2.5m



About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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