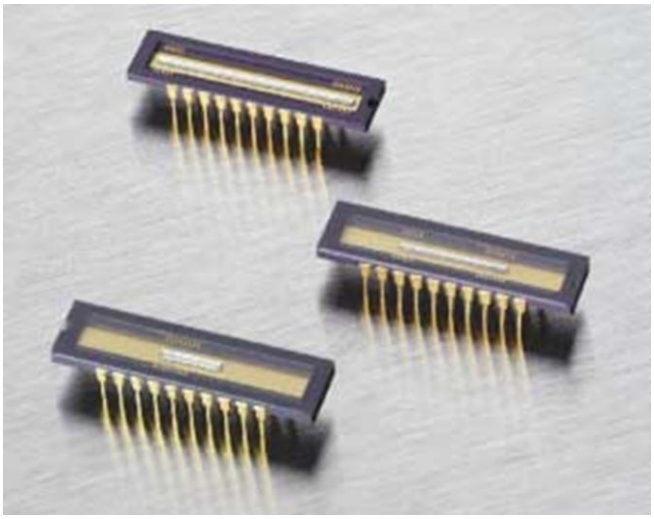
P-Series CCD Sensors

Linear Photodiode Array Imager
14µm, single-output, 512, 1024, 2048 elements



The P-Series imager is available in standard array lengths of 512, 1024, and 2048 elements with either glass or UV-enhanced fused silica windows.

Excelita P-series linear imager combines high-sensitivity photodiode array detection and high-speed charge coupled scanning to offer an uncompromising solution to the increasing demands of advanced imaging applications.

These high performance imagers feature low noise, high sensitivity, impressive charge-storage capacity, and lag-free dynamic imaging in a convenient single-output architecture. The 14 µm square contiguous pixels in these imagers reproduce images with minimum information loss and artifact generation, while their unique photo diode structure provides excellent blue response extending below 250 nm and into the ultraviolet.

The two-phase CCD readout register requires only 5 volts for clocking, yet achieves excellent charge transfer efficiency. Additional electrodes provide independent control of exposure and antiblooming. Finally, the high-sensitivity readout amplifier provides a large output signal to relax noise requirements on the camera electronics that follow. These versatile imagers are widely used in high-speed document reading, web inspection, mail sorting, production measurement and gauging, position sensing, spectroscopy, and other industrial and scientific applications requiring peak imager performance.

Key Features

- Extended spectral range – 200 to 1000 nm
- 40 MHz pixel readout rate with line rates to 70 kHz
- >2500:1 dynamic range
- 5-volt clocking
- 14µm square pixels with 100% fill factor
- Ultra-low image lag
- Electronic exposure and anti-blooming controls
- ROHS Compliant

Applications

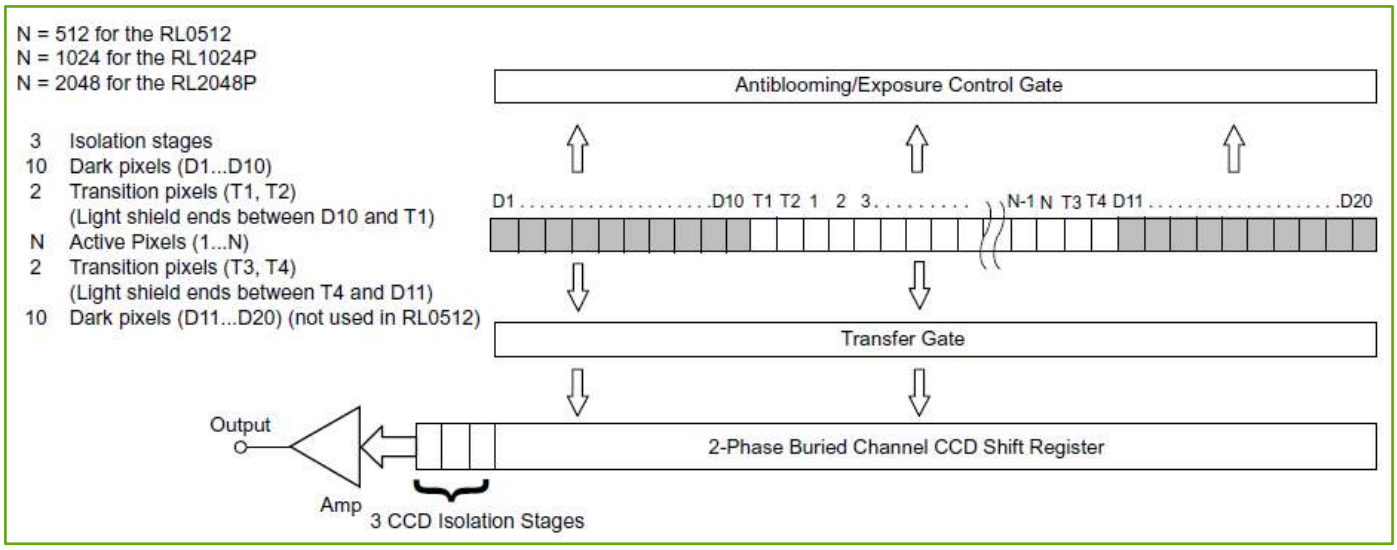
- High-speed document reading
- Mail sorting
- Web inspection
- Production measurement and gauging
- Position sensing
- Spectroscopy
- Ophthalmological Laser Scanning

EXCELITAS TECHNOLOGIES®

Light Detection Area

The light detection area in P-Series imagers is a linear array of contiguous pinned photodiodes on 14 µm centers. These photodiodes are constructed using Excelitas' advanced photodiode design that extends short-wavelength sensitivity into the deep UV below 250 nm, while preserving 100% fill factor and delivering extremely low image lag. This unique design also avoids polysilicon layers in the light detection area that reduces the quantum efficiency of most CCD imagers. The P-Series imagers are supplied with glass windows for general visible use, or fused silica windows for use in the UV below 250nm. On a custom basis, P-Series imagers can be supplied without an affixed window. See Figures 2a and 2b for sensitivity and window transmission curves.

Figure 1. Imager Functional Diagram



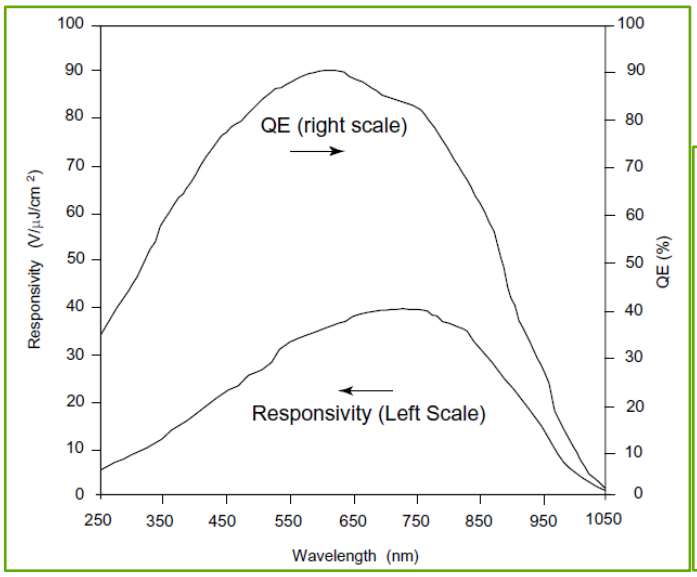
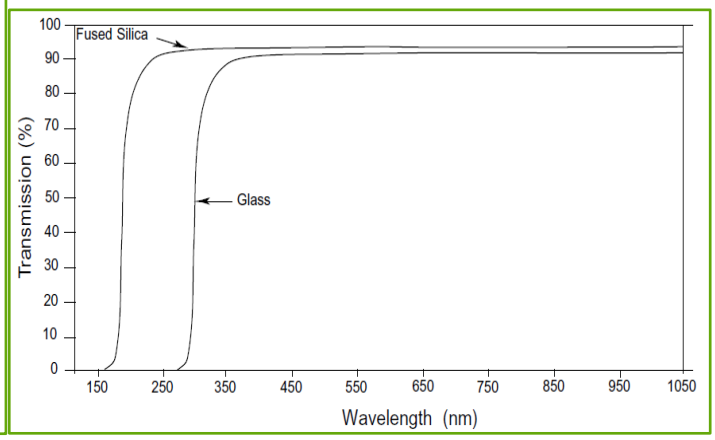


Figure 2a: Spectral Sensitivity Curve

Figure 2b: Window Transmission Curve



Due to the potential for light leakage, the two dark pixels nearest the transition pixels should not be used as a dark reference. For lowest lag, all P-Series imagers feature pinned photodiodes. Pinning, which requires a special semiconductor process step, provides a uniform internal voltage reference for the charge stored in every photodiode. This stable reference assures that every photodiode is fully discharged after every scan. Photodiodes covered with light shields included at one or both ends of the imager provide a dark-current reference for clamping. These are separated from the active photodiodes by two unshielded transition pixels that assure uniform response out to the last active photodiode.

Horizontal Shift Registers

Charge packets, collected in the photodiodes as light is received, are converted to a serialized output stream through a buried channel, two-phase CCD shift register that provides high charge transfer efficiency at shift frequencies up to 40 MHz. The Excelitas 5-volt CCD process used in this design enables low-power, high-speed operation with inexpensive, readily available driver devices.

The transfer gate (ØTG) controls the movement of charge packets from the photodiodes to the CCD shift register. During charge integration, the voltage controlling the ØTG is held in its low state to isolate the photodiodes from the shift register. When transfer of charge to the shift register is desired, ØTG is switched to its high state to create a transfer channel between the photodiodes and the shift register. The charge transfer sequence, detailed in Figure 4, proceeds as follows:

After readout of a particular image line (n), the shift register is empty of charge and ready to accept new charge packets from the photodiode representing image line n+1. To begin the transfer sequence, the horizontal clock pulses (ØH1 and ØH2) are stopped with ØH1 held in its high state, and ØH2 in its low state. ØTG is then switched high to start the transfer of charge to the shift register. Once the ØTG reaches its high state, the photo gate voltage (ØPG) is set to high to complete the transfer.
It is recommended that the photo gate voltage be held in the high state for at least 0.1 µs to ensure complete transfer. After this interval, the photo gate voltage is returned to its low state, and when this is completed, the transfer gate is also returned to its low state. The details of the transfer timing are shown in Figure 3 with ranges and tolerances in Table 1.

Table 1. Transfer Timing Requirements at Operating Voltage - Vop

Parameter Description	Symbol	Minimum	Typical	Maximum
Delay of $Ø_{TG}$ falling edge from $Ø_{PG}$ falling edge	t_1	5 ns	20 ns	--
Delay of $Ø_{TG}$ rising edge from end of $Ø_{H1}$ and $Ø_{H2}$ clocks	t_2	0 ns	10 ns	--
Delay of $Ø_{AB}$ rising edge from: $Ø_{PG}$ falling edge $Ø_{TG}$ pulse width $Ø_{PG}$ pulse width	 t_3 t_4 t_5	 5 ns 100ns 100ns	 5 ns 500ns 400ns	--
Rise/fall time	t_6	10 ns	20 ns	--
Integration time	t_7	0 ns	-	--
$Ø_{AB}$ pulse width	t_8	-	750ns [1]	--

Note 1: 750ns is the typical time to fully reset the photodiode

After transfer, the charge is transported along the shift register by the alternate action of two horizontal phase voltages ØH1 and ØH2. While the two-phase CCD shift register architecture allows relaxed timing tolerances over those required in three- or four-phase, optimum charge transfer efficiency (CTE) and lowest power dissipation is obtained when the overlap of the two-phase CCD clocks occurs around the 50% transition level. Additionally, the phase difference between signals ØH1 and ØH2 should be maintained near 180° and the duty cycle should be set near to 50% to prevent loss of full well charge storage capacity and charge transfer efficiency. Readout timing details are shown in Figure 4 with ranges and tolerances in Table 2.

Timing Requirements

In high-speed applications, fast waveform transitions allow maximum settling time of the output signal. However, it is generally advisable to use the slowest rise and fall times consistent with required video performance because fast edges tend to introduce more transition noise into the video waveform. When the highest speeds are required, careful smoothing of the waveform transitions may improve the balance between speed and video quality.

Table 2. Readout Timing Requirements

Parameter Description	Symbol	Minimum	Typical	Maximum
$Ø_{H1}$, $Ø_{H2}$ clock period	t_1	25ns	--	--
$Ø_{H1}$, $Ø_{H2}$ rise/fall time	t_2	--	5ns	--
$Ø_{RG}$ rise/fall time	t_3	--	5ns	--
$Ø_{RG}$ clock - high duration	t_4	5ns	--	--
Delay of $Ø_{H1}$ high –low transition from $Ø_{RG}$ low	t_5	0ns	--	--

Note: The cross over point for $Ø_{H1}$ and $Ø_{H2}$ clock transitions should occur within the 10 - 90% level of the clock amplitude.

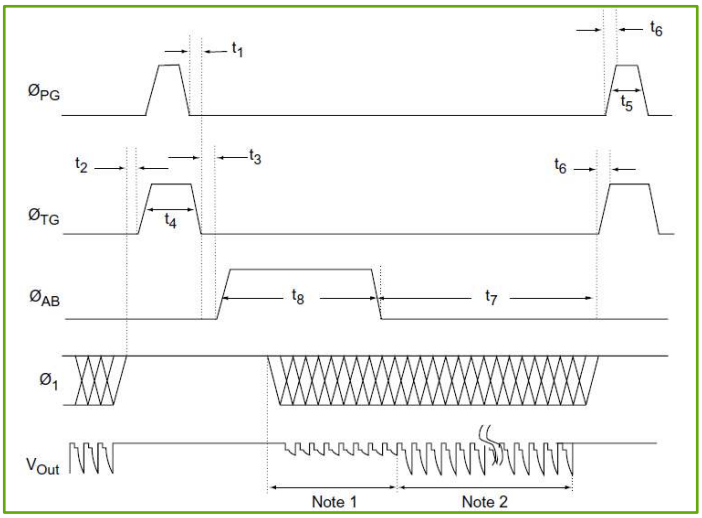
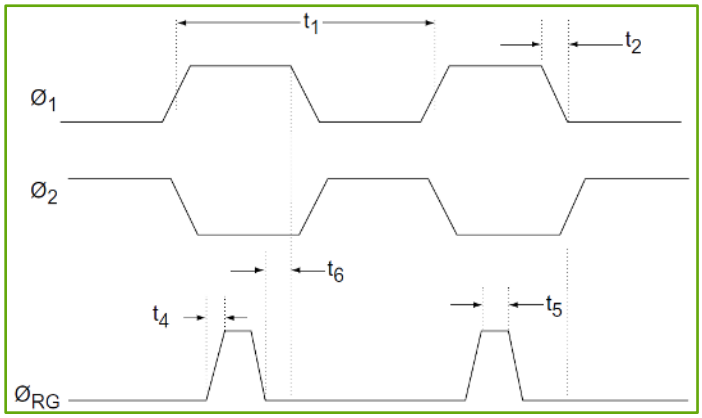


Figure 3: Transfer Timing Diagram

Figure 4: Readout Timing Waveforms



Output Amplifier

Charge emerging from the last stage of the shift register is converted to a voltage signal by a charge integrator and video amplifier. The integrator, a capacitor created by a floating diffusion, is initially set to a DC reference voltage (VRD) by setting the reset transistor voltage (ØRG) to its high state. To read out the charge, ØRG is pulsed low turning the reset transistor off and isolating the integrator from VRD. The next time ØH1 goes low, the charge packet is transferred to the integrator, where it generates a voltage proportional to the packet size. The reset transistor voltage, ØRG, must reach its low state prior to the high-to-low transition of ØH1. An apparent clipping of the video signal will result if this condition is not satisfied. Figure 4 details the clock waveform requirements and overlap tolerances.

The video amplifier buffers the signal from the integrator for output from the imager. Care must be taken to keep the load on this amplifier within its ability to drive highly reactive or low-impedance loads. The half-power bandwidth into an external load of 10 pF is 150 MHz. It is recommended that the output video signal be buffered with a wide bandwidth follower or other appropriate amplifier to provide a large Z_{in} to the output amplifier. Keep the external amplifier close to the output pins to minimize stray inductive and capacitive coupling of the output signal that can harm signal quality.

Imager Configuration

All P-Series imagers are constructed using ceramic packages and optically flat windows. Imager die are secured to precision lead frames by thermal silver-filled epoxy. Packages are baked before sealing to eliminate moisture and tested for seal integrity.

Table 3. Imager Performance (Typical)

Parameter Description	Performance
Pixel count	512 elements (RL0512P) 1024 elements (RL1024P) 2048 elements (RL2048P)
Pixel size	14 µm x 14 µm
Exposure control	yes
Horizontal clocking	2Ø (5V clock amplitude)
Number of outputs	1
Dynamic range[1]	>2500:1
Readout noise (rms) amplifier reset transistor total noise without CDS	 18 electrons 45 electrons 50 electrons
Saturation exposure[2]	27 nJ/cm2
Noise equivalent exposure	8.1 pJ/cm2
Amplifier sensitivity	6.6 µV/electron
Saturation output voltage	1100 mV
Saturation charge capacity	167,000 electrons
Charge Transfer Efficiency	>0.99995
Peak responsivity	41 V/µJ/cm2
PRNU	±5%
Dead pixels	0
Lag	1. 5%
Spectral Response Range	200 nm to 1000 nm
Data Range	40 MHz

Notes:
1. Defined as Qsat/rms noise (total)
2. For illumination at 750 nm

Exposure Control and Antiblooming

An exposure control feature in the P-Series imagers supports variable charge accumulation time in the photodiode. When the antiblooming gate voltage ($Ø_{AB}$) is set to its high state, charge is drained from the pixel storage gate to the exposure control drain. During normal charge collection in the photodiode, $Ø_{AB}$ is set to its low state. Due to the timing requirements of the exposure control mode, charge is always accumulated at the end of the period just before the charge is transferred to the read out register. Figure 3 includes the timing requirements for exposure control with the antiblooming gate. The exposure control timing shown will act on the charge packets that emerge as video data on the next readout cycle.

Imager Performance

In P-Series imagers each element performs its own function admirably while integrating smoothly with the other elements on the team. The photodiodes efficiently transform light to charge, the readout registers accurately transport the charge to the amplifier, and the amplifier delivers a clean, robust signal for use in image processing electronics. While the actual performance of these imagers depends strongly on the details of the electronics and timing of the camera, their straight-forward implementation requirements facilitate optimum designs.

Operating Conditions

For optimum performance and longest life, carefully follow the operational requirements of these imagers. Provide stable voltage sources which are free of noise and variation, and clean waveforms with controlled edges. Protect the imager from electrostatic discharge (ESD) and excessive voltages and temperatures. Do not violate the limits on output register speed or reduce timing margins below the minimums.

Table 4. Operating Voltages

Signal	Function	State	Voltage	Tolerance
$Ø_{H1}$, $Ø_{H2}$	Horizontal Clocks	High Low	5 0	+5%
$Ø_{TG}$	Transfer Gate	High Low	8 0	±10%
$Ø_{PG}$	Photo Gate	High Low	8 -4	+5% ±5%
$Ø_{AB}$	Antiblooming Gate	High Low	4 -4	+5% ±5%
V_{OG}	Output Gate		3	±5%
$Ø_{RG}$	Reset Gate	High Low	8 0	±10%
V_{DD}	Amplifier Voltage Supply		12	±5%
V_{RD}	Amplifier Reset Drain		9.5	±5%
V_{SS}/LS	Amplifier Return / Light Shield		0	

Figure 5. Pinout Configuration

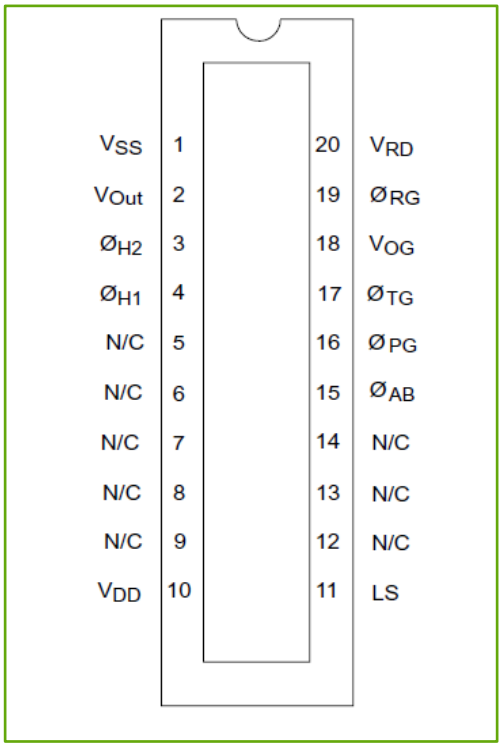


Table 5. Absolute Maximum Ratings (above which useful life may be impaired)

	Minimum	Maximum	Unit
Storage Temperature	-25	+85	°C
Operating Temperature	-25	+55	°C
Voltage (with respect to GND)			
Pins 3, 4, 17-19	-0.3	+18	V
Pins 2, 10, 20	-0.3	+18	V
Pins 1, 11	-0.3	0	V
Pins 15, 16	-4.3	+18	V

Precautionary Note: The CCD output in (pin#2) must never be shorted to either VSS or VDD while power is applied to the device. Catastrophic device failure will result.

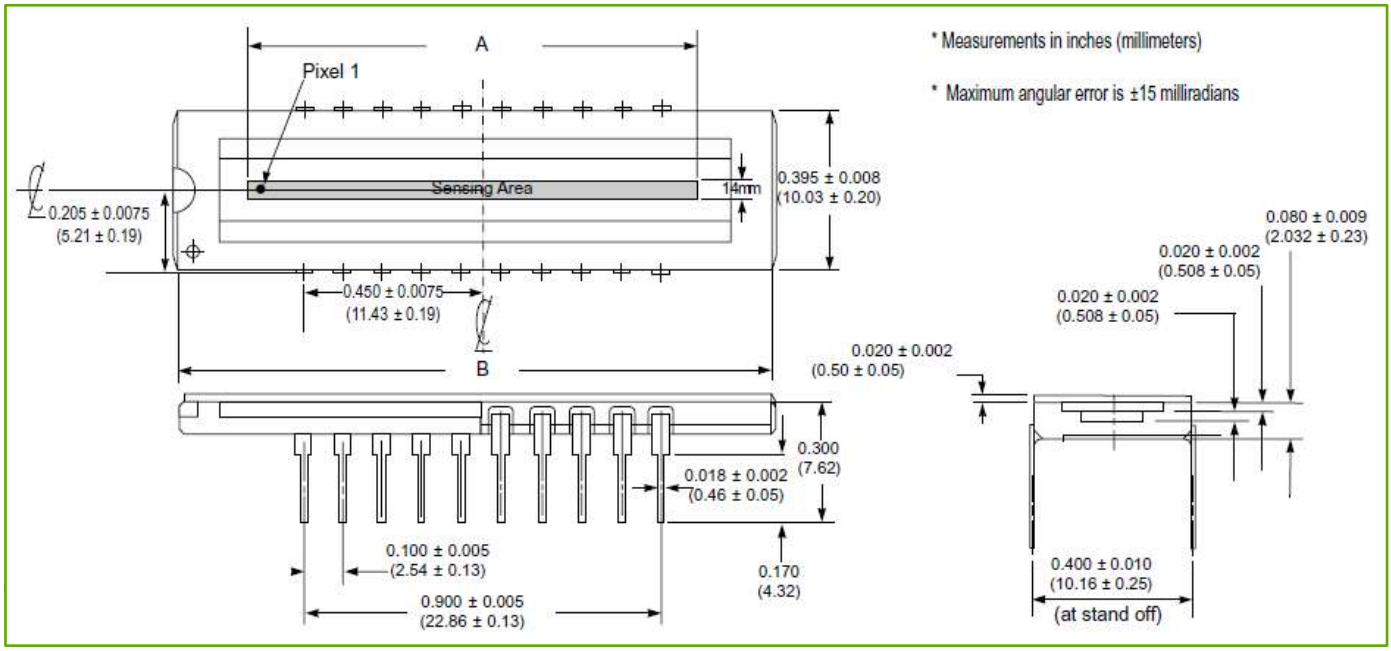
Table 7. Package Dimensions and Tolerances

Device	A		B	
	mm	Inches	mm	Inches
RL0512P	7.22	0.28	38.1±0.38	1.50±0.15
RL1024P	14.39	0.57	38.1±0.38	1.50±0.15
RL2048P	28.73	1.13	38.1±0.38	1.50±0.15

Table 6. Pinout Description and Capacitance Values

Pin	Symbol	Function	Typical Capacitance (pF)		
			Pixels		
			2048	1024	512
1	V_{SS}	Amplifier return	50	30	20
2	V_{OUT}	Signal output	75	45	30
3	$Ø_{H2}$	CCD horizontal phase 2	320	150	70
4	$Ø_{H1}$	CCD horizontal phase 1	350	190	90
5	N/C	No connection	-	-	-
6	N/C	No connection	-	-	-
7	N/C	No connection	-	-	-
8	N/C	No connection	-	-	-
9	N/C	No connection	-	-	-
10	V_{DD}	Amplifier drain supply	-	-	-
11	LS	Light shield	-	-	-
12	N/C	No connection	-	-	-
13	N/C	No connection	-	-	-
14	N/C	No connection	-	-	-
15	$Ø_{AB}$	Antiblooming gate	70	35	20
16	$Ø_{PG}$	Photo gate	100	50	25
17	$Ø_{TG}$	Transfer gate	90	50	25
18	V_{OG}	Output gate	8	8	8
19	$Ø_{RG}$	Reset gate	7	2	2
20	V_{RD}	Reset drain	-	-	-

Figure 6. Outline Drawing



The RL0512P, RL1024P and RL2048P are available with either glass or fused silica windows. On special orders, Excelitas can supply anti-reflective coated windows or windowless packages. Imagers are packed in electrostatic-resistant boxes and identified by lot numbers for tracking.

Table 8. Ordering Guide

Window	Active Pixels		
	512	**1024**	**2048**
Glass	RL0512PAG-021	RL1024PAG-021	R2048PAG-021
Fused Silica	RL0512PAQ-021	RL1024PAQ-021	RL2048PAQ-021

RoHS Compliance

The P-series linear imager is designed and built to be fully compliant with the European Union Directive 2011/65/EU – Restriction of the use of certain Hazardous Substances (RoHS) in Electrical and Electronic equipment.

Warranty

A standard 12-month warranty following shipment applies.

About Excelitas Technologies

Excelitas Technologies is a global technology leader focused on delivering innovative, customized solutions to meet the lighting, detection and other high-performance technology needs of OEM customers.

Excelitas has a long and rich history of serving our OEM customer base with optoelectronic sensors and modules for more than 45 years beginning with Excelitas, EG&G, and RCA. The constant throughout has been our innovation and commitment to delivering the highest quality solutions to our customers worldwide.

From aerospace and defense to analytical instrumentation, clinical diagnostics, medical, industrial, and safety and security applications, Excelitas Technologies is committed to enabling our customers' success in their specialty end-markets. Excelitas Technologies has approximately 5,000 employees in North America, Europe and Asia, serving customers across the world.

Excelitas Technologies
22001 Dumberry Road
Vaudreuil-Dorion, Quebec
Canada J7V 8P7
Telephone: (+1) 450.424.3300
Toll-free: (+1) 800.775.6786
Fax: (+1) 450.424.3345
detection.na@excelitas.com

Excelitas Technologies GmbH & Co. KG
Wenzel-Jaksch-Str. 31
D-65199 Wiesbaden
Germany
Telephone: (+49) 611 492 430
Fax: (+49) 611 492 165
detection.europe@excelitas.com

Excelitas Technologies Singapore, Pte. Ltd.
8 Tractor Road
Singapore 627969
Telephone: (+65) 6775 2022 (Main number)
Telephone: (+65) 6770 4366 (Customer Service)
Fax: (+65) 6778-1752
detection.asia@excelitas.com

For a complete listing of our global offices, visit www.excelitas.com/locations