

# TYPES SN54490, SN54LS490, SN74490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

OCTOBER 1976—REVISED DECEMBER 1983

- Dual Versions of Popular SN5490A, SN54LS90, SN7490A, and SN74LS90 Counters
- Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter
- Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%
- Maximum Count Frequency . . . 35 MHz Typical
- Buffered Outputs Reduce Possibility of Collector Commutation

## description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single '490 or 'LS490. Buffering on each output is provided to ensure that susceptibility to collector commutation is reduced significantly. All inputs are diode-clamped to reduce the effects of line ringing. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

The SN54490 and SN54LS490 are characterized for operation over the full military temperature range of -55°C to 125°C; the SN74490 and SN74LS490 are characterized for use in industrial systems operating from 0°C to 70°C.

BCD COUNT SEQUENCE  
(EACH COUNTER)

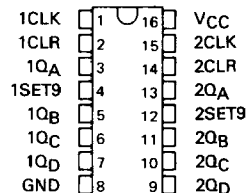
COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

CLEAR/SET-TO-9  
FUNCTION TABLE  
(EACH COUNTER)

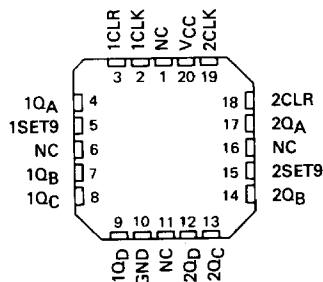
INPUTS		OUTPUTS			
CLEAR SET-TO-9		Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
H	L	L	L	L	L
L	H	H	L	L	H
L	L	COUNT			

H = high level, L = low level

SN54490, SN54LS490 . . . J OR W PACKAGE  
SN74490 . . . J OR N PACKAGE  
SN74LS490 . . . D, J OR N PACKAGE  
(TOP VIEW)

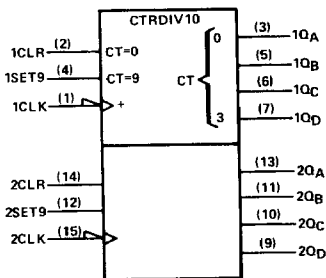


SN54LS490 . . . FK PACKAGE  
SN74LS490 . . . FN PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol

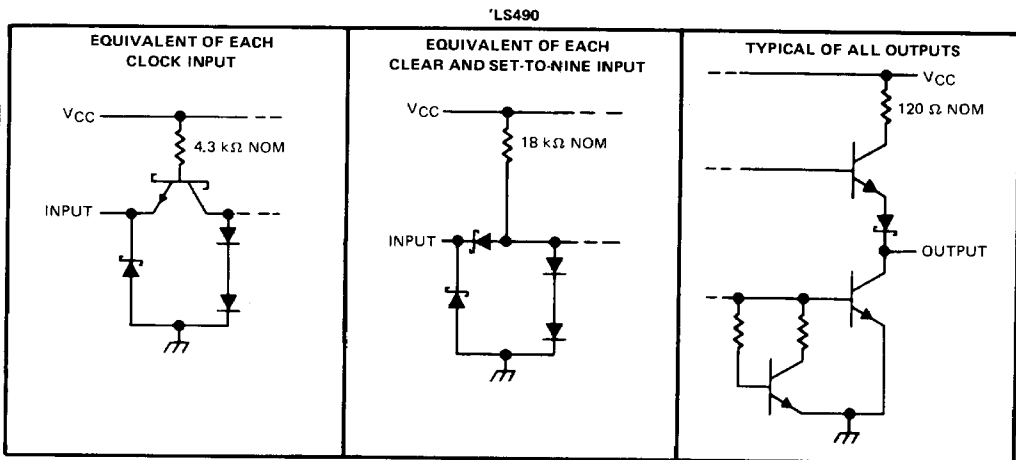
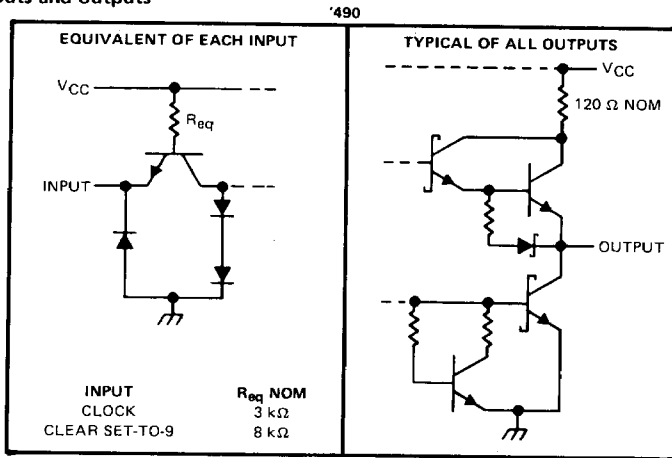


Pin numbers shown on logic notation are for D, J or N packages.  
NC - No internal connection



**TYPES SN54490, SN54LS490, SN74490, SN74LS490**  
**DUAL 4-BIT DECADE COUNTERS**

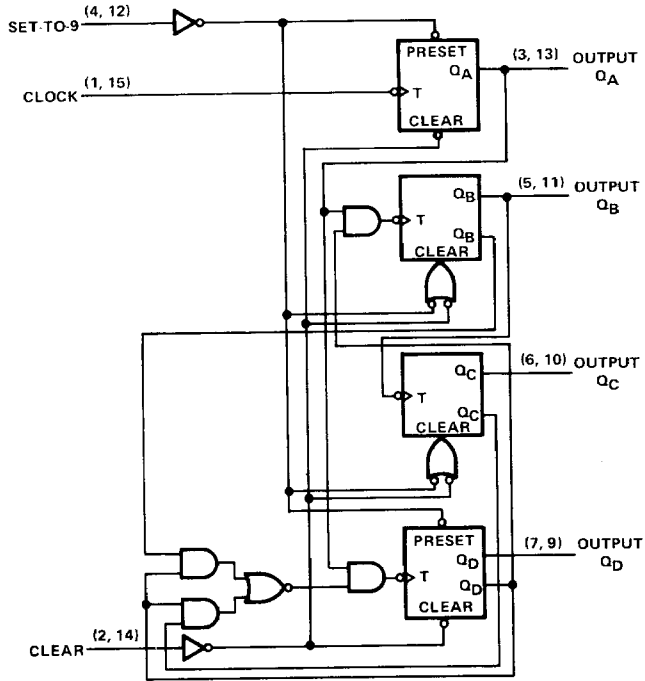
schematics of inputs and outputs



**3 TTL DEVICES**

TYPES SN54490, SN54LS490, SN74490, SN74LS490  
DUAL 4-BIT DECADE COUNTERS

logic diagram (each counter)



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

# TYPES SN54490, SN74490 DUAL 4-BIT DECADE COUNTERS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54490	-55°C to 125°C
SN74490	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54490			SN74490			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Count frequency, $f_{count}$	0		25	0		25	MHz
Pulse width, $t_w$ (any input)		20			20		ns
Clear or set-to-9 inactive-state setup time, $t_{su}$	25			25			ns
Operating free-air temperature, $T_A$	-55		125	0		70	°C

†The arrow indicates that the falling edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High-level input current	Clear, set-to-9			40	$\mu$ A
		Clock	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		80	
$I_{IL}$	Low-level input current	Clear, set-to-9			-1	mA
		Clock	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-3.2	
$I_{OS}$	Short-circuit output current §	$V_{CC} = \text{MAX}$				mA
		SN54490	-20		-57	
		SN74490	-18		-57	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , See Note 2		45	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

3

TTL DEVICES

**TYPES SN54490, SN74490  
DUAL 4-BIT DECADE COUNTERS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{ C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{max}}$	Clock	$Q_A$	$C_L = 15\text{ pF}$ , $R_L = 400\ \Omega$ , See Figure 1 and Note 3	25	35		MHz
$t_{\text{PLH}}$	Clock	$Q_A$		12	20		ns
$t_{\text{PHL}}$				13	20		
$t_{\text{PLH}}$	Clock	$Q_B, Q_D$		24	39		ns
$t_{\text{PHL}}$				26	39		
$t_{\text{PLH}}$	Clock	$Q_C$		32	54		ns
$t_{\text{PHL}}$				36	54		
$t_{\text{PHL}}$	Clear	Any		24	39		ns
$t_{\text{PLH}}$	Set-to-9	$Q_A, Q_D$		24	39		ns
$t_{\text{PHL}}$		$Q_B, Q_C$		20	36		

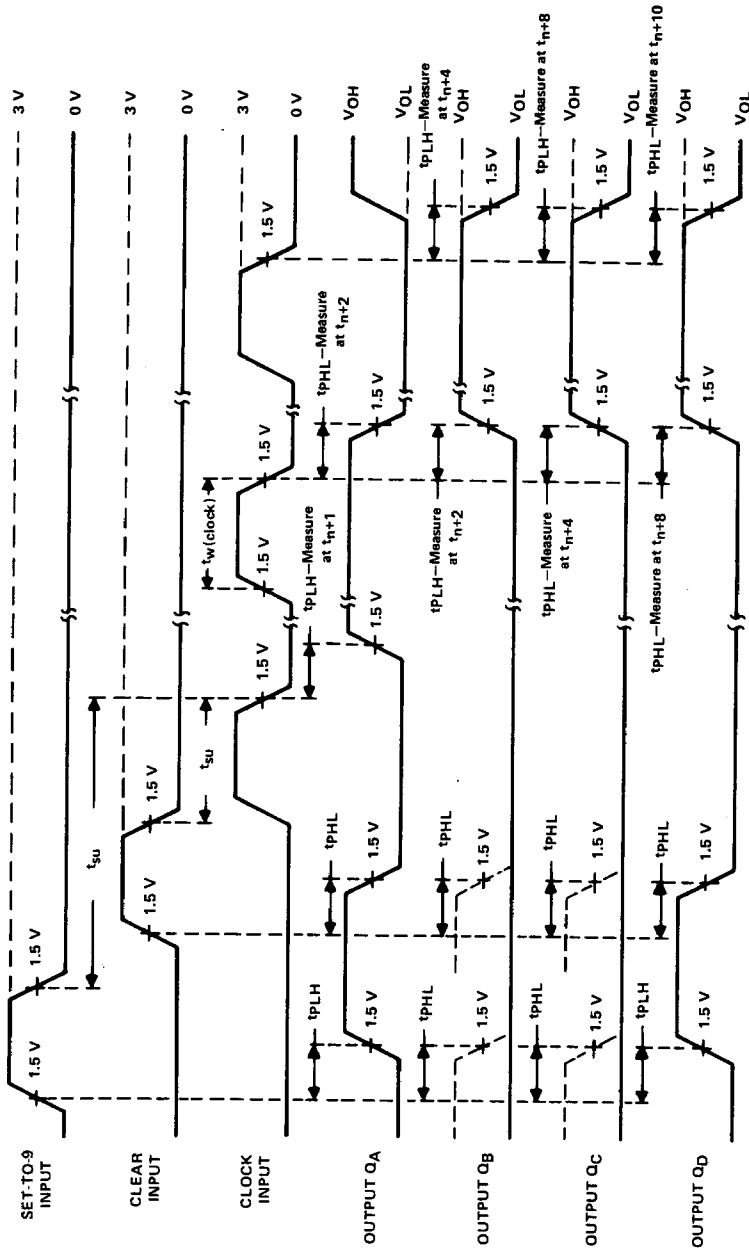
†  $f_{\text{max}}$  ≡ maximum count frequency  
 $t_{\text{PLH}}$  ≡ propagation delay time, low-to-high-level output  
 $t_{\text{PHL}}$  ≡ propagation delay time, high-to-low-level output  
 NOTE 3: See General Information Section for load circuits and voltage waveforms.

**3**

**TTL DEVICES**

TYPES SN54490, SN74490  
DUAL 4-BIT DECADE COUNTERS

3 TTL DEVICES



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics:  $t_r \leq 5$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.

FIGURE 1

# TYPES SN54LS490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Clear and set-to-9 input voltage	7 V
Clock input voltage	5.5 V
Operating free-air temperature range: SN54LS490	-55°C to 125°C
SN74LS490	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54LS490			SN74LS490			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	-400			-400			$\mu$ A
Low-level output current, $I_{OL}$	4			8			mA
Count frequency, $f_{count}$	0	25		0	25		MHz
Pulse width, $t_w$ (any input)	20			20			ns
Clear or set-to-9 inactive-state setup time, $t_{SU}$	25 $\downarrow$			25 $\downarrow$			ns
Operating free-air temperature, $T_A$	-55	125		0	70		°C

$\downarrow$ The arrow indicates that the falling edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS490			SN74LS490			UNIT	
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX		
$V_{IH}$	High-level input voltage		2			2			V	
$V_{IL}$	Low-level input voltage		0.7			0.8			V	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$	2.5	3.4		2.7	3.4		V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	V	
			$I_{OL} = 8 \text{ mA}$				0.35	0.5		
$I_I$	input current at maximum input voltage	Clear, set-to-9 Clock $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1		0.1		mA	
			$V_I = 5.5 \text{ V}$		0.2		0.2			
$I_{IH}$	High-level input current	Clear, set-to-9 Clock $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20		20		$\mu$ A	
					100		100			
$I_{IL}$	Low-level input current	Clear, set-to-9 Clock $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4		-0.4		mA	
					-1.6		-1.6			
$I_{OS}$	Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20		-100		-20		mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX},$ See Note 2	15		26		15		26	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

3

TTL DEVICES

# TYPES SN54LS490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER <sup>†</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$	Clock	$Q_A$	$C_L = 15\text{ pF}$ , $R_L = 2\text{ k}\Omega$ See Figure 2 and Note 3	25	35		MHz
$t_{PLH}$	Clock	$Q_A$			12	20	ns
$t_{PHL}$					13	20	
$t_{PLH}$	Clock	$Q_B, Q_D$			24	39	ns
$t_{PHL}$					26	39	
$t_{PLH}$	Clock	$Q_C$			32	54	ns
$t_{PHL}$					36	54	
$t_{PHL}$	Clear	Any			24	39	ns
$t_{PLH}$	Set-to-9	$Q_A, Q_D$			24	39	ns
$t_{PHL}$		$Q_B, Q_C$			20	36	

<sup>†</sup> $f_{\max}$  = maximum count frequency

$t_{PLH}$  = Propagation delay time, low-to-high-level output

$t_{PHL}$  = Propagation delay time, high-to-low-level output

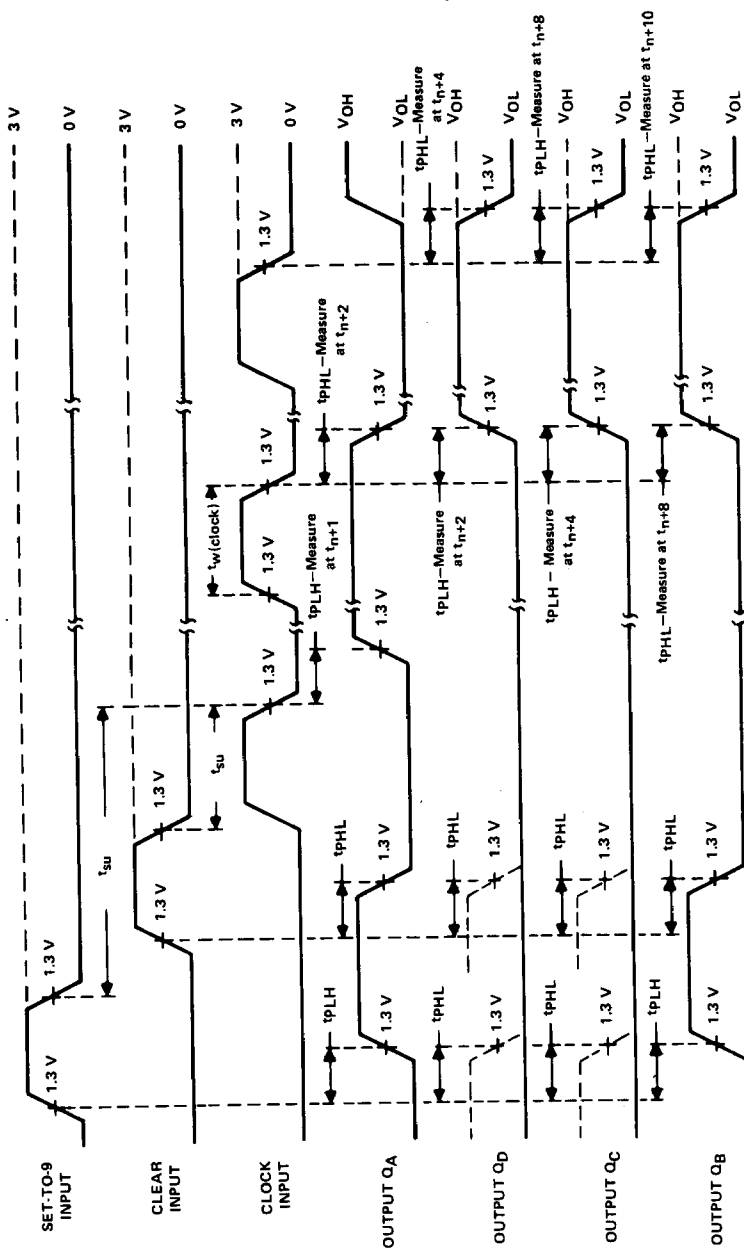
NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES



**TYPES SN54LS490, SN74LS490  
DUAL 4-BIT DECADE COUNTERS**



**VOLTAGE WAVEFORMS**

NOTES: A. Input pulses are supplied by a generator having the following characteristics:  $t_r \leq 15$  ns,  $t_f \leq 6$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.

**FIGURE 2**



**TTL DEVICES**