Datasheet

Multi-Channel Power Supply LSI Series for Car Electronics

Multi-channel Power Supply IC for Car Audio Systems

BD49101ARFS-M

General Description

The BD49101ARFS-M LSI is a multi-channel power supply IC that can provide all necessary supply voltages for automobile audio systems. The IC has two Switching Power Supplies (DCDC), five Regulators (REG) and a High Side switch. This single power supply system can provide the required voltages to all systems including the MCU, CD, tuner, USB, illumination, audio circuits and others.
The IC system is based on switching regulator which has high efficiency then you can suppress heat of IC than before. And it has low power mode operation or voltage control function so that you can get ①High Efficiency ②Low IQ and ③easiness of power supply design.

Features

- AEC-Q100 Qualified(Note1)
- Integrated 7 channels of Power Supply for Car Audio
  - ・2 DCDC (Integrated 1 Controller)
  - ・5 REG
- 1 High Side Switch channel
- Integrated Low Power Standby REG for MCU Power Supply
- REG4 Cable Impedance Compensation
- I^2C Interface
- Selectable Oscillator Frequency using External Resistance
- External Clock Synchronization
- Power Supply Control Function (Power on/off Sequencer).
- Low Voltage, Over Voltage and REG4 Over Current Detect Flag
- Integrated Protection Circuitry:
  - ・Over Voltage Input Protection
  - ・Over Current Protection
  - ・Thermal Shutdown

(Note1:Grade3)

Applications

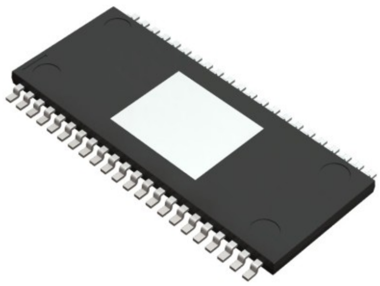
- Car Audio and Infotainment

Key Specifications

Input Voltage Range:	5.5V to 25V(VIN0=BCAP)
DCDC1(controller):	
DCDC2(with low power mode for MCU):	1A
REG1(output voltage variable):	500mA
REG2(output voltage variable):	100mA
REG3(output voltage variable):	300mA
REG4(output voltage variable for USB):	1.5A
REG5(output voltage variable):	50mA
High side SW:	500mA
Standby Current:	100µA(Typ)
REG4 Over Current Detect Accuracy:	±20%
Operating Temperature Range:	-40°C to +85°C
DCDC Switching Frequency:	200kHz to 500kHz

Package

Package	W(Typ) x D(Typ) x H(Max)
HTSSOP-A44R	18.50mm x 9.50mm x 1.00mm



HTSSOP-A44R

○Product structure:Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

Pin Configuration

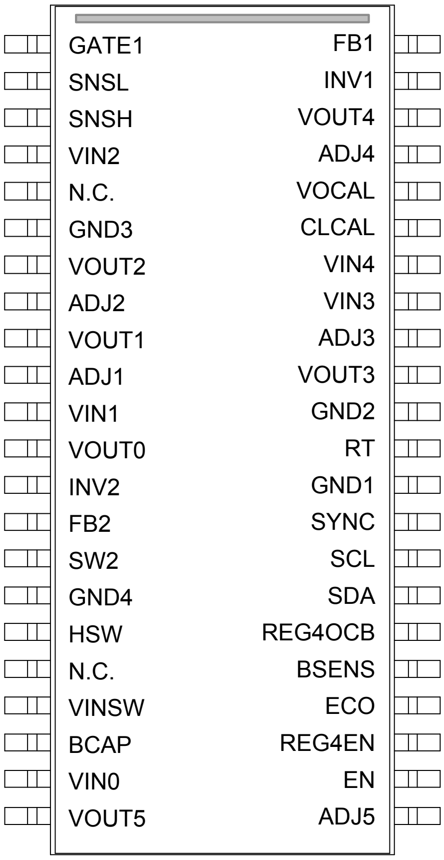


Figure 1. Pin Configuration(s)

Pin Description

Pin NO	Symbol	Function	Pin NO	Symbol	Function
1	GATE1	DCDC1 outside FET gate drive	23	ADJ5	REG5 output voltage adjustment
2	SNSL	DCDC1 current detection	24	EN	Enable
3	SNSH	DCDC1 current detection	25	REG4EN	REG4 Enable
4	VIN2	Power supply for built-in FET REG2	26	ECO	Low power mode switch
5	N.C.	―	27	BSENS	Error flag output
6	GND3	Ground	28	REG4OCB	Error flag output
7	VOUT2	REG2 voltage output	29	SDA	I^2C-bus data input
8	ADJ2	REG2 output voltage adjustment	30	SCL	I^2C-bus clock input
9	VOUT1	REG1 voltage output	31	SYNC	External synchronization signal input
10	ADJ1	REG1 output voltage adjustment	32	GND1	Ground
11	VIN1	Power supply for built-in FET REG1	33	RT	Oscillator frequency setting
12	VOUT0	STBREG voltage output	34	GND2	Ground
13	INV2	DCDC2 Error Amp Input	35	VOUT3	REG3 voltage output
14	FB2	DCDC2 Error Amp output	36	ADJ3	REG3output voltage adjustment
15	SW2	DCDC2 switching output	37	VIN3	Power supply for built-in FET REG3
16	GND4	Ground	38	VIN4	Power supply for built-in FET REG4
17	HSW	High side switch output	39	CLCAL	REG4 over current protection setting
18	N.C.	―	40	VOCAL	REG4 output USB cable impedance calibration setting
19	VINSW	Power supply for high side switch	41	ADJ4	REG4 output voltage adjustment
20	BCAP	Back-up capacity connection pin	42	VOUT4	REG4 voltage output
21	VIN0	Battery power supply connection pin	43	INV1	DCDC1 Error Amp Input
22	VOUT5	REG5 voltage output	44	FB1	DCDC1 Error Amp output

"N.C" pins are not connected into internal circuits.

Block Diagram

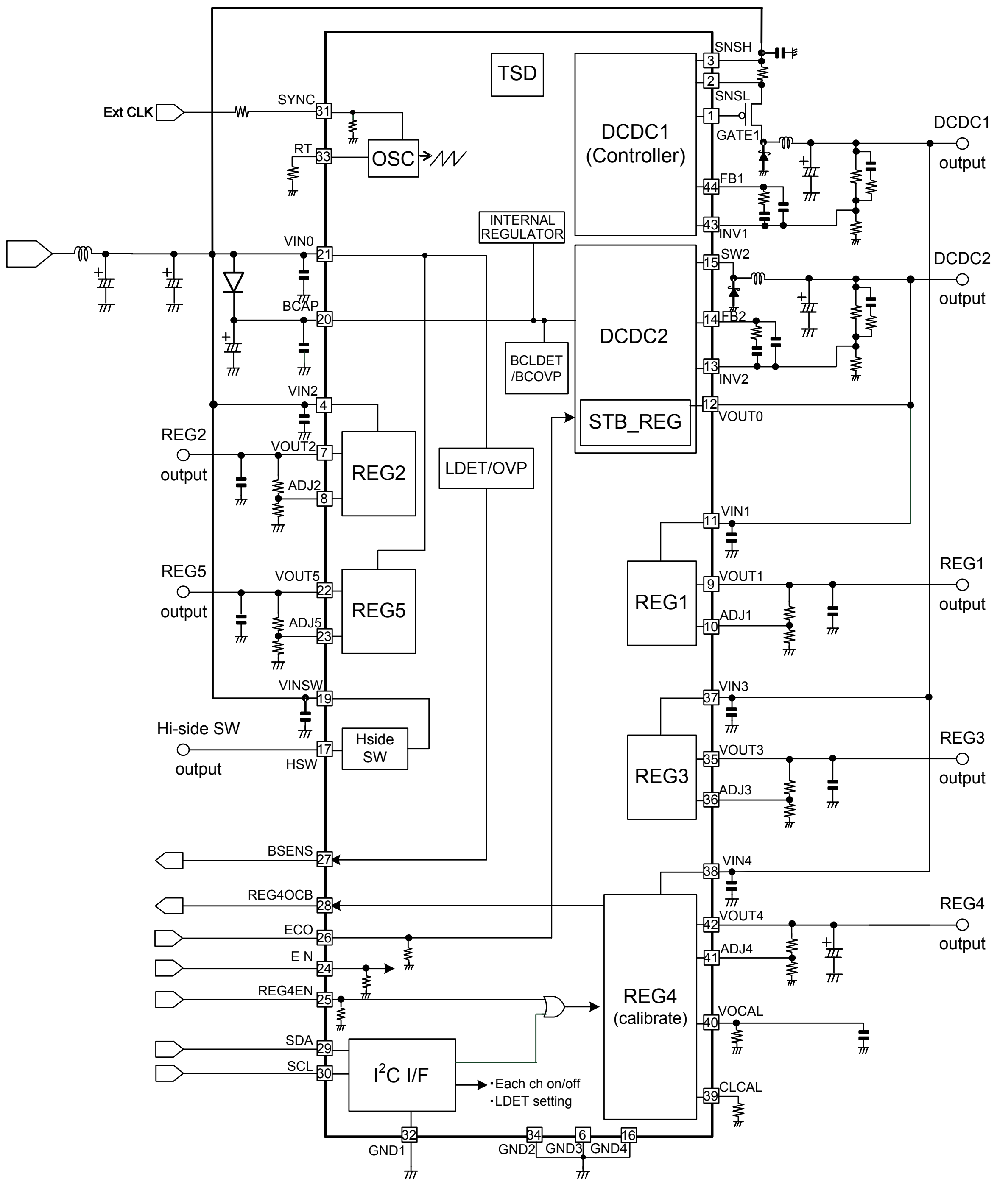


Figure 2. Block Diagram

Description of Blocks

・DCDC2 – STBREG Switch Function

The ECO input is used to switch between operating mode and low power standby mode.
(This function is for a 3.3V I/O microcomputer because of the 3.3V fixed STBREG output)
The function of the ECO input is as follows:

- ECO = H – Normal Operating Mode (DCDC2 operating).
- ECO = L – Low Power Standby Mode (STBREG operating).

・Sequence of VIN0 start up, Low Power Standby mode

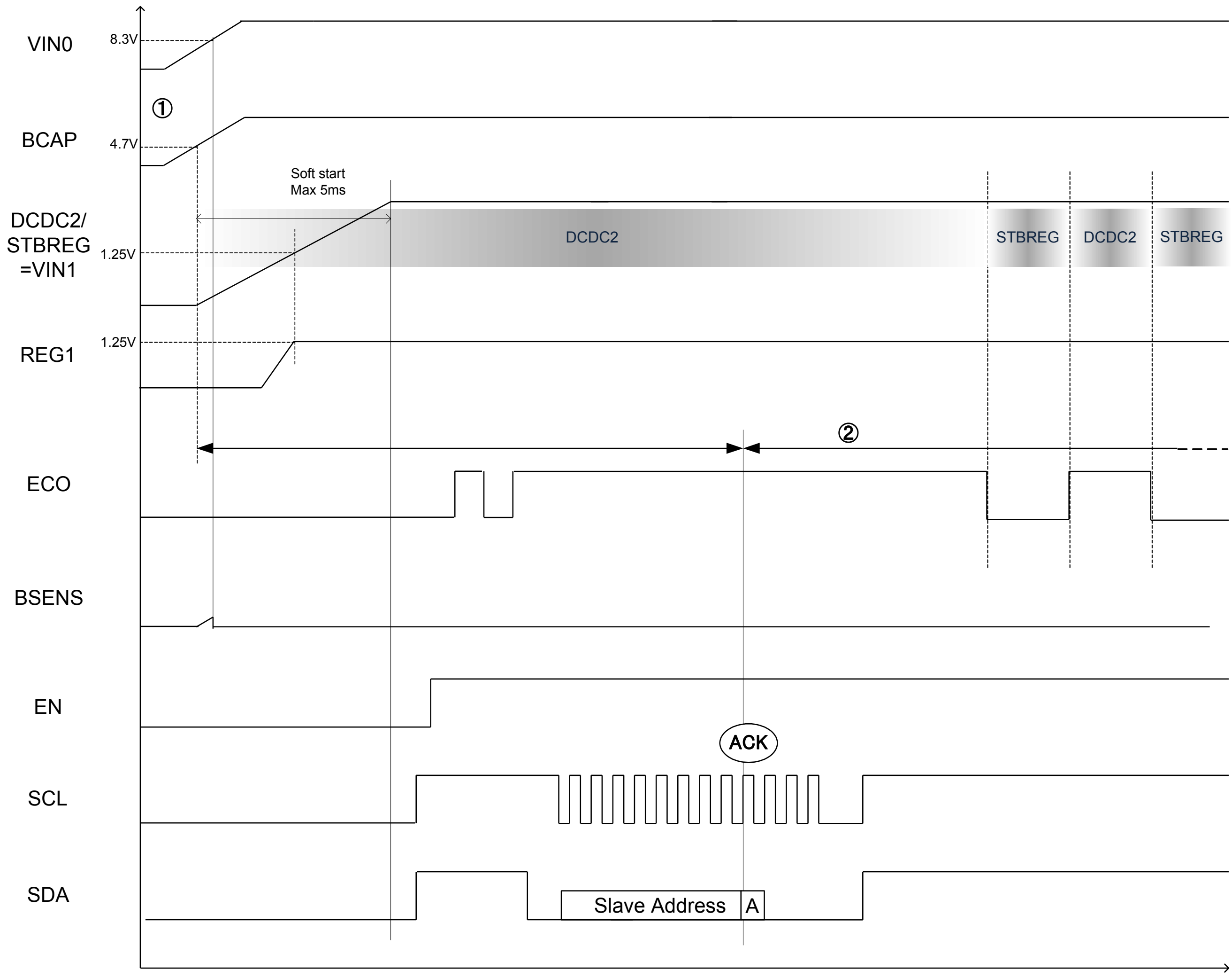


Figure 3. Timing Chart of VIN0 start up, Low Power Standby Mode

① When BD49101ARFS starts up, it starts in the normal operation mode (DCDC2 operation), independent of ECO setting. An internal regulator, the reference voltage circuit, and the OSC circuit start up when the voltage of the BCAP pin exceeds low voltage protection release voltage (4.7V).

② Following the first access to the I^2C interface, the ECO input is able to control the operating mode (normal or low power standby). ECO must be set to the desired operating mode prior to accessing the I^2C interface for the first time.

③ The conditions of independent of ECO setting is shown below.

- Input power supply for VIN0 at the first time
- BCAP voltage becomes under 4.5V
- DCDC2 detects over current and DCDC2 restarts

At each condition ECO setting become effective after you send I^2C command and receive ACK.

・Relations of BCAP Voltage and Operating Mode

When the voltage of the BCAP pin decreases under BCAP low voltage detection voltage (4.5V),
the registers are initialized and the ECO pin setting becomes invalid and forcibly changed to low power mode.
Afterwards, when BCAP voltage increases over BCAP low detection release voltage (4.7V)
without under POWER ON reset voltage (3.1V), the mode change to DCDC2 mode. (ECO pin setting is invalid.)
If BCAP voltage increases with under POWER ON reset voltage, the operation is same as VIN0 start up.

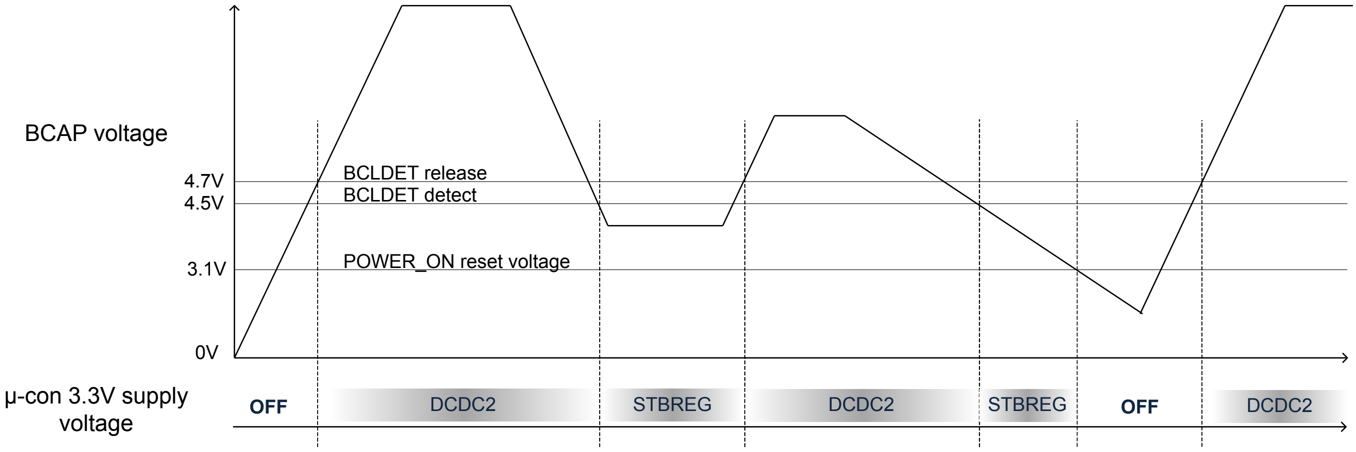


Figure 4. Relation of BCAP Voltage and Operating Mode

・Mode Changing (Normal Operation Mode ⇔ Low Power Mode)

When the ECO pin is changed from “L” to “H”, it changes from the low power mode to the normal operation mode. When it changes from the low power mode to the normal operation mode, the output voltage drops according to the load current. (Figure 5)
(ex.) : Supply Voltage 14.4V, Output Capacitor 100μF, Load Current 200mA: Output Drop Voltage= -80mV(Typ)
We recommend that you save consumption current of the microcomputer in 200mA within 1ms when the mode is changed to normal operation mode (Figure 6).

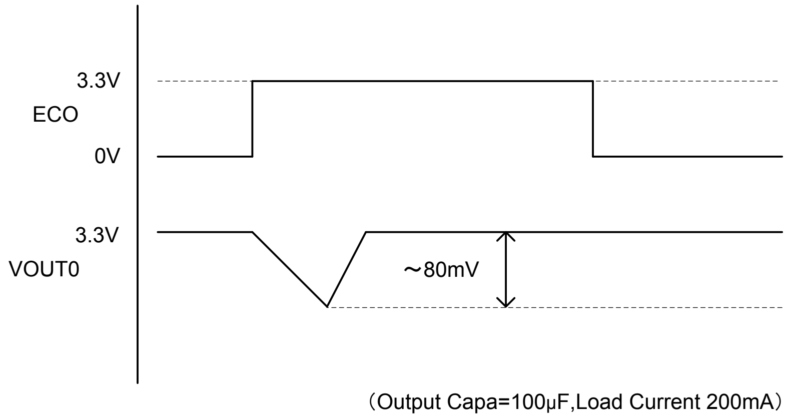


Figure 5. Timing Chart of Mode Changing (Normal Operation Mode ⇔ Low Power Mode)

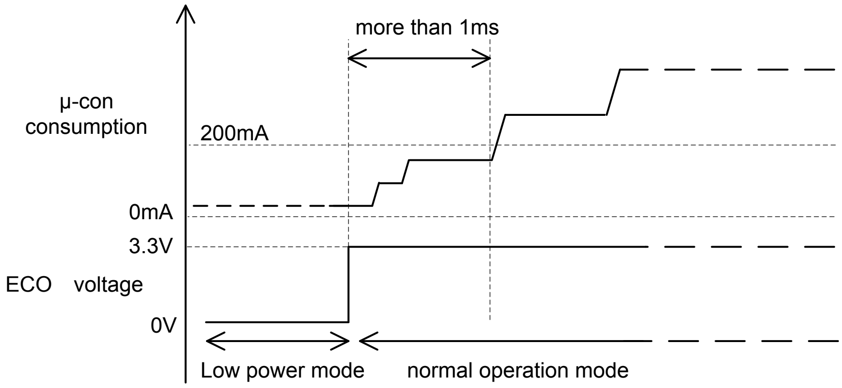


Figure 6. Image of Increasing Consumption Current when Switching from Low Power Mode to Normal Operation Mode

USB Supply Calibration (REG4).

The VOCAL input is used to adjust for cable impedance between the supply and USB connector. This adjustment will correct for voltage drop across the cable as a function of the current flow thus maintaining a constant voltage at the connector. Compensation of up to 0.5Ω of cable impedance can be achieved. The CLCAL input is used to set the over current threshold, up to a maximum of 1.5A.Please refer 2-(3)-② Setting of cable impedance calibration

Over Current Protection (OCP)

All regulators and high side switch have over current protection. When OCP is detected, the following conditions will apply:

- DCDC1: After disabled for a certain period, it will attempt to restart automatically.
- DCDC2 : After disabled for a certain period, it will attempt to restart automatically and the register will be initialized.
- REG4 – Current limit circuit will operate and REG4OCB is activated (Low).
- Other regulators and a high side switch – Current limit circuit will operate.

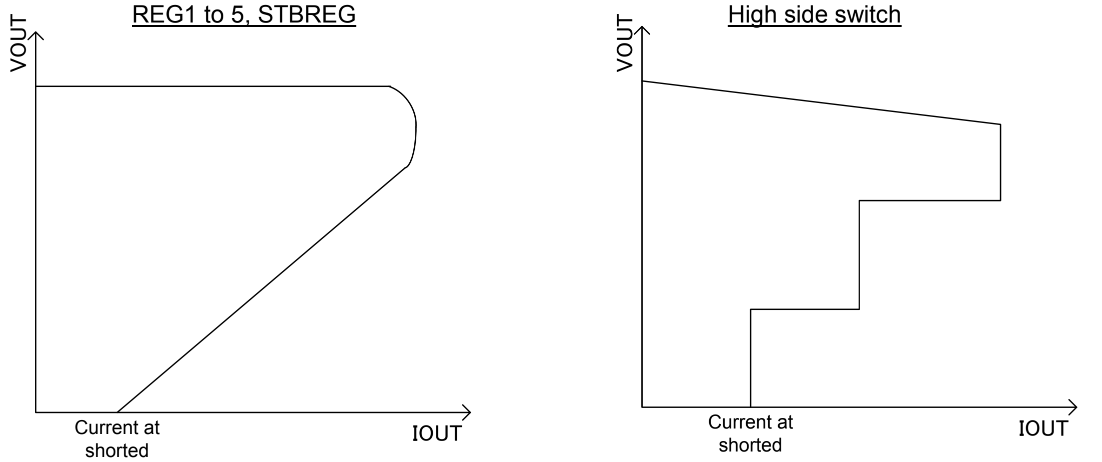


Figure 7. REG, High Side Switch Example of the Characteristics about Output Voltage vs Output Current

Battery Voltage Monitoring Function and BSENS Output

The BSENS output is active (High) when over voltage protection(OVP) is active. OVP becomes active when VIN0 exceeds 20.2V(Typ) OVP is cleared when VIN0 falls below 18.2V(Typ).
BSENS is also active (High) when VIN0 falls below 7.8V(Typ, initial register condition), afterwards BSENS is cleared when VIN0 exceeds 8.3V (Typ, initial register condition).
This low detection (LDET) voltage can change from 5.7V to 6.4V, and from 7.7V to 8.4V with writing register (Initial setting is 7.8V).

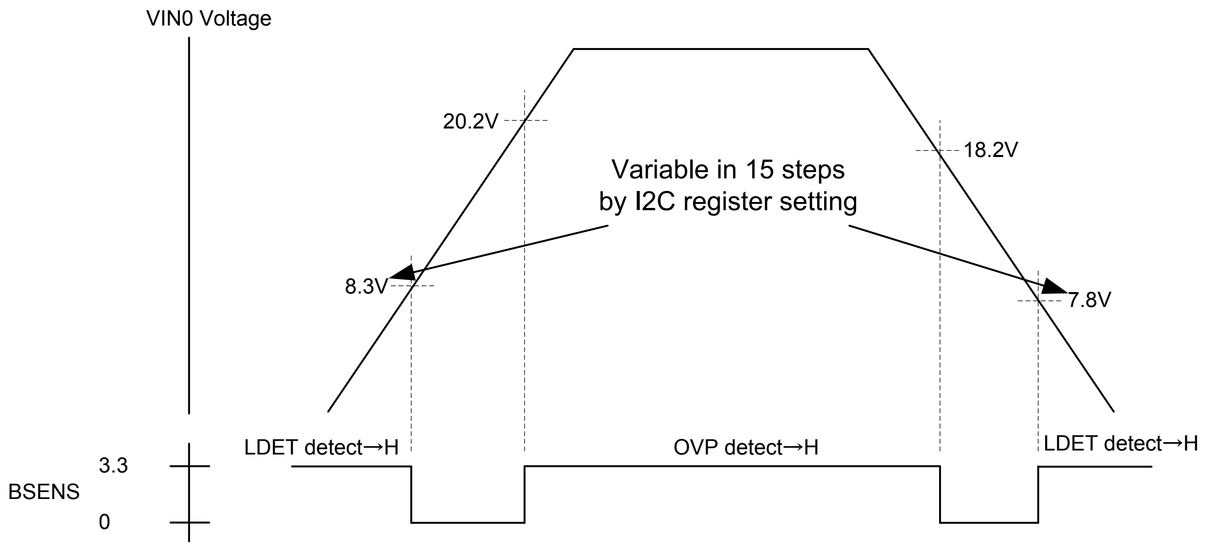


Figure 8. Timing Chart of OVP/LDET Detection

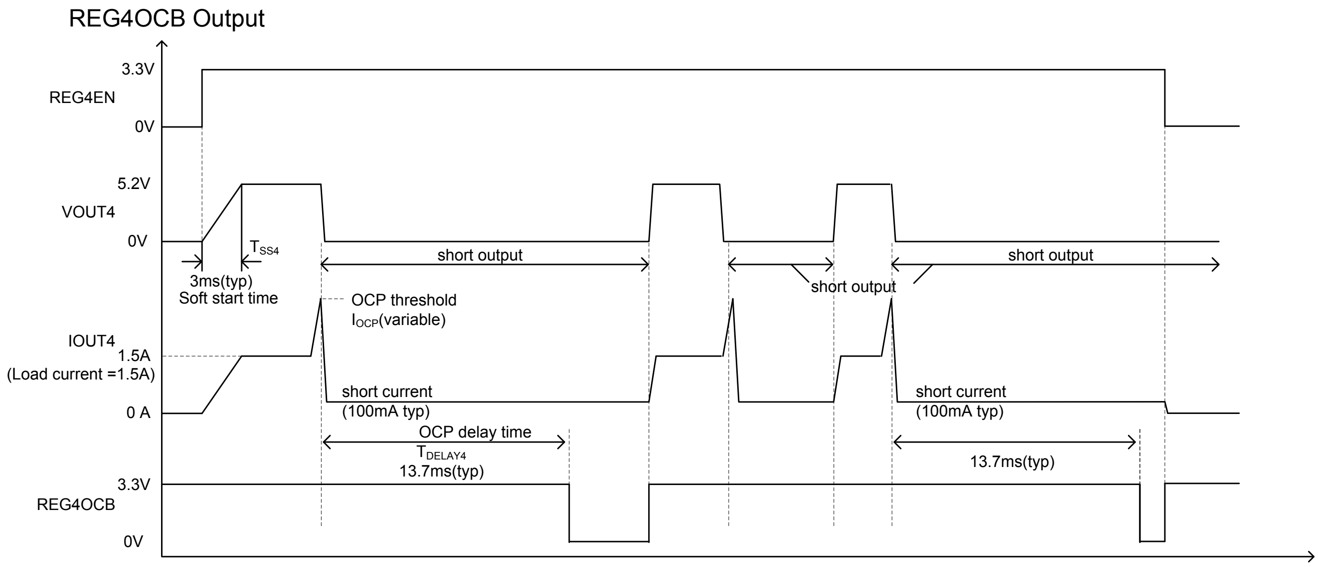


Figure 9. Timing Chart of REG4OCB Output

REG4 starts by a soft start in 3ms(Typ). And when detecting over current detection the REG4OCB output is active (Low) after 13.7ms continuous over current condition.

External Synchronization

The SYNC input is used to synchronize the switching frequency of DCDC1 and DCDC2. A signal in the range of 200kHz – 500kHz can be input. The input signal must be at a higher frequency than that set by the resistor on RT input and should be configured between 0.6 to 1.5 times the set frequencies.(when SYNC Duty=45 to 55%)
When it changes from internal oscillation mode to external synchronization mode, it changes after it is inputted continuously 3 pulses.
When it changes from external synchronization mode to internal oscillation mode, it changes within a period of internal oscillator frequency after SYNC input sets L. When SYNC input sets H, it doesn't change to internal oscillation mode. The high pulse within 50ns(like unexpected noise etc.) input could stop DCDC operation. In that case you can take measure by inserting damping resister etc. to reduce the pulse.
At first applying of power on VIN0(BCAP), SYNC pin must be under "input L level" max value until VODC2 rises up. If it is not so, the IC could not start normally.
It can adjust to the phase of switching pulse between DCDC1 and DCDC2 by the duty of SYNC input.
The switching positive edge timing of DCDC1,2 is below.

- DCDC1: synchronized the negative edge of SYNC input.
- DCDC2: synchronized the positive edge of SYNC input

The EN and the REG4EN pins

When the EN pin is set to H, I2C register setting is available, and when set to L, all register reset.
This function enable all REG and HSW channel expect DCDC2/STBREG and REG1 to OFF.
REG4EN is the enable pin of REG4 and can control REG4 through REG4_EN register or REG4EN.
When the EN pin is set to L, REG4 becomes OFF even if the REG4EN pin is set to H.

Input Pin	Output Conditions							Register
	STBREG	DCDC2	REG1	DCDC1	REG2,3,5	REG4	HSW	
EN	–	–	L=ON	L=OFF need resetting when turning ON				Reset (input"L")
REG4EN	–	–	–	–	–	L=OFF H=ON(Note 1)	–	–
ECO	L=STBREG H=DCDC2		–	–	–	–	–	–

(Note 1) When the EN pin input H.

Figure 10. Table of EN control

I^{2}C Interface

The I^{2}C interface allows access to the internal registers. The internal registers are used for the following functions:

- Enable the high side switch and power supplies except for DCDC2-STBREG.
- Setting LDET – VIN0 low voltage detection threshold.
- Detecting high side switch over current condition (address 0x04)

For Protect and Detect Functions and Enable Function

		Output Conditions							Error Flag		Register
		STBREG	DCDC2	REG1	DCDC1	REG2,3,5	REG4	HSW	BSENS	REG4OCB	
over current detection	STBREG	fold back limit	–	–	–	–	–	–	–	–	–
	DCDC2	–	restart (Note 1)	–	OFF(Note 2)				–	–	Reset
	REG1	–	–	fold back limit	–	–	–	–	–	–	–
	DCDC1	–	–	–	restart (Note 1)	–	–	–	–	–	–
	REG2,3,5	–	–	–	–	fold back limit	–	–	–	–	–
	REG4	–	–	–	–	–	fold back limit		–	○	–
	HSW	–	–	–	–	–	–	fold back limit	–	–	–
thermal power supply voltage detection	TSD	–	–	–	OFF(Note 3)				–	–	–
	LDET	–	–	–	–	–	–	–	○	–	–
	OVP	–	–	–	–	–	–	–			
	BCLDET	ON (Note 4)	OFF (Note 4)	–	OFF(Note 2)				–	–	Reset
	BCOVP	–	–	–	OFF(Note 3)				–	–	–

(Note 1) When detecting each output is limited in minimum duty and dropping output and INV voltage then restarts after 1024clk.
(Note 2) When detecting each output doesn’t restart.
(Note 3) When detecting each output restarts.
(Note 4) When detecting BCAP low voltage the operation mode switches to standby mode without depending on the ECO setting.

Figure 11. Table of EN Protect and Detect Functions

Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage (PIN4,19,20,21)	V_{CC}	-0.3 to +42	V
Input Voltage(PIN24,25,26,29,30,31)	Vin	-0.3 to +7	V
Pin Voltage 1(PIN1,7,15,17,22)	V_{PIN1}	-0.3 to +42	V
Pin Voltage 2(PIN2,3)	V_{PIN2}	VIN0 – 7 to VIN0	V
Pin Voltage 3(PIN8-14,23,27,28,33,35-44)	V_{PIN3}	-0.3 to +7	V
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings

Parameter	Symbol	Limits	Unit
Operating Power Supply Voltage1(VIN0,BCAP)	V_{INopr}	5.5 to 25	V
Output Voltage Range 1(DCDC1/2)	$V_{OUTopr1}$	0.8 to V_{INopr}	V
Output Voltage Range 2(REG1/3/4)	$V_{OUTopr2}$	0.8 to 2.4 (REG1) 0.8 to VIN3,4 - $VSAT_{RG3,4}$ (REG3.4)	V
Output Voltage Range 3(REG2/5)	$V_{OUTopr3}$	0.8 to 10.5 (REG2) 0.8 to 8.5 (REG5)	V
DCDC Switching Frequency	f_{SW}	200 to 500	kHz
Oscillator Frequency Setting Resistance	R_T	27 to 82	kΩ
External Sync Frequency	f_{CLK}	200 to 500	kHz
External Synchronization Pulse Duty	D_{CLK}	20 to 80	%
REG4 Over Current Detection Set Resistance	R_{CLCAL}	5 to 50	kΩ
REG4 Cable Impedance Compensation Set Resistance	R_{VOCAL}	0 to 230	Ω

Electrical Characteristics

(Unless otherwise specified, Ta= 25°C, VIN0=BCAP=14.4V, EN=3.3V, VOUT1=1.25V, VOUT2=5.78V, VOUT3=3.3V, VOUT4=5.2V, VOUT5=5.0V)

Parameter	Symbol	Spec Values			Unit	Conditions
		Min	Typ	Max		
【Consumption Current】						
Standby Current	I_{STB}	―	100	150	μA	ECO=0V, EN=0V
Circuit Current	I_Q	―	5.0	7.5	mA	ECO=3.3V, EN=3.3V, Io=0A ENABLE=0x7F
【Over Voltage Detection】						
Detection Threshold Voltage	V_{OVPON}	18.2	20.2	22.2	V	
Release Threshold Voltage	V_{OVPOFF}	16.2	18.2	20.2	V	
【Low Voltage Detection】						
Detection Threshold Voltage	V_{LDETON}	7.5	7.8	8.1	V	LDET_SETTING=0x09
Release Threshold Voltage	$V_{LDETOFF}$	8.0	8.3	8.6	V	
【OSC】						
Oscillator Frequency	F_{OSC}	285	300	315	kHz	RT=51kΩ
【DCDC1】						
Reference Voltage	V_{REF1_DC1}	0.784	0.800	0.816	V	
Over Current Detection Threshold Voltage	$V_{OCP\_TH\_DC1}$	-	0.1	-	V	SNSH-SNSL
Maximum FB1 Voltage	V_{FB1H}	-	3.0	-	V	INV1=0V
Minimum FB1 Voltage	V_{FB1L}	-	0.8	-	V	INV1=2V
FB1 Sink Current	$I_{FB1SINK}$	-800	-400	-200	μA	FB1=1V, INV1=1V
FB1 Source Current	$I_{FB1SOURCE}$	50	100	200	μA	FB1=1V, INV1=0.6V
Maximum GATE1 Voltage	V_{GT1H}	-	-	VIN +0.3V	V	INV1=2V
Minimum GATE1 Voltage	V_{GT1L}	8.1	-	-	V	INV1=0V
Soft Start	TSS1	-	-	5	ms	
【DCDC2】						
Reference Voltage	V_{REF1_DC2}	0.784	0.800	0.816	V	
Output Current Capacity	IO_{DC2}	1	-	-	A	
Maximum FB2 Voltage	V_{FB2H}	-	3.0	-	V	INV2=0V
Minimum FB2 Voltage	V_{FB2L}	-	0.8	-	V	INV2=2V
FB2 Sink Current	$I_{FB2SINK}$	-800	-400	-200	μA	FB2=1V, INV2=1V
FB2 Source Current	$I_{FB2SOURCE}$	50	100	200	μA	FB2=1V, INV2=0.6V
Soft Start	TSS2	-	-	5	ms	
Power MOS FET ON Resistance	R_{ON}	125	250	500	mΩ	IO=800mA

Parameter	Symbol	Spec Values			Unit	Conditions
		Min	Typ	Max		
【STBREG】						
Reference Voltage	V_{REF_STLD}	3.234	3.300	3.366	V	
Load Current Capacity	IO_{STLD}	200	-	-	mA	
Line Regulation	ΔVI_{STLD}	-	-	15	mV	VIN0=7 to 18V, Io=5mA
Load Regulation	ΔVL_{STLD}	-	-	30	mV	IO=5m to 200mA
Ripple Rejection	RR_{STLD}	-	70	-	dB	Frp=100Hz, VIN0rp=1Vpp
I/O Voltage Difference	$VSAT_{STLD}$	-	-	0.6	V	IO=100mA
【REG1】						
Reference Voltage	V_{REF_LD1}	0.588	0.600	0.612	V	
Load Current Capacity	IO_{LD1}	500	-	-	mA	VIN1=3.3V
Line Regulation	ΔVI_{LD1}	-	-	10	mV	VIN1=3 to 6V, Io=5mA
Load Regulation	ΔVL_{LD1}	-	-	20	mV	IO=5m to 500mA
Ripple Rejection	RR_{LD1}	-	70	-	dB	Frp=100Hz, VIN1rp=1Vpp
I/O Voltage Difference	$VSAT_{LD1}$	-	-	1.0	V	IO=250mA
【REG2】						
Reference Voltage	V_{REF_LD2}	0.777	0.793	0.809	V	
Load Current Capacity	IO_{LD2}	100	-	-	mA	
Line Regulation	ΔVI_{LD2}	-	-	25	mV	VIN2=9 to 18V, Io=5mA
Load Regulation	ΔVL_{LD2}	-	-	50	mV	IO=5mA to 100mA
Ripple Rejection	RR_{LD2}	-	70	-	dB	Frp=100Hz, VIN2rp=1Vpp
I/O Voltage Difference	$VSAT_{LD2}$	-	-	0.65	V	IO=50mA
【REG3】						
Reference Voltage	V_{REF_LD3}	0.784	0.800	0.816	V	
Load Current Capacity	IO_{LD3}	300	-	-	mA	VIN3=6V
Line Regulation	ΔVI_{LD3}	-	-	20	mV	VIN3=4.0 to 6.5V, Io=5mA
Load Regulation	ΔVL_{LD3}	-	-	40	mV	IO=5m to 300mA
Ripple Rejection	RR_{LD3}	-	70	-	dB	Frp=100Hz, VIN3rp=1Vpp
I/O Voltage Difference	$VSAT_{LD3}$	-	-	0.6	V	IO=150mA

Parameter	Symbol	Spec Values			Unit	Conditions
		Min	Typ	Max		
【REG4】						
Reference Voltage	V_{REF_RG4}	0.784	0.800	0.816	V	
Load Current Capacity	IO_{RG4}	1.5	―	―	A	VIN4=6V,VOCAL=0Ω
Line Regulation	$⊿VI_{RG4}$	―	―	50	mV	VIN4=5.6 to 6.5V, Io=5mA
Load Regulation	$⊿VL_{RG4}$	―	―	40	mV	Io=5m to 1.5A
Ripple Rejection	RR_{RG4}	―	55	―	dB	Frp=100Hz, VIN4rp=1Vpp
I/O Voltage Difference	$VSAT_{RG4}$	―	―	0.4	V	Io=1.5A
Over Current Detection Threshold 1	I_{OCP1}	1.18	1.47	1.76	A	VIN4=6V, CLCAL= 6.8kΩ, VOCAL=0Ω
Over Current Detection Threshold 2	I_{OCP2}	534	667	800	mA	VIN4=6V, CLCAL= 15kΩ, VOCAL=0Ω
Voltage Adjusted For Cable Impedance(0.26Ω)	V_{cal}	5.32	5.46	5.60	V	VIN4=6.5V,Io=1.0A, VOCAL=120Ω
Soft Start Time	T_{SS4}	―	3	―	ms	
OCP Delay Time	T_{DELAY4}	8.7	13.7	18.7	ms	f_{sw} = 300kHz
【REG5】						
Reference Voltage	V_{REF_RG5}	0.784	0.800	0.816	V	
Load Current Capacity	IO_{RG5}	50	―	―	mA	
Line Regulation	$⊿VI_{RG5}$	―	―	25	mV	VIN0=9 to 18V, Io=5mA
Load Regulation	$⊿VL_{RG5}$	―	―	50	mV	Io=5mA to 50mA
Ripple Rejection	RR_{RG5}	―	70	―	dB	Frp=100Hz, VIN5rp=1Vpp
I/O Voltage Difference	$VSAT_{RG5}$	―	―	0.65	V	Io=25mA
【High Side SW】						
Output Current Capacity	IO_{SW1}	500	-	-	mA	
ON Resistance	R_{ON_SW1}	―	-	3	Ω	IO=500mA
【Digital IO】 (EN,REG4EN,ECO,SYNC,BSENS,REG4OCB)						
Input H level	V_{IH}	2.6	-	-	V	For pin EN, REG4EN, ECO,SYNC
Input L level	V_{IL}	-	-	0.8	V	For pin EN, REG4EN, ECO,SYNC
Input Pulldown Resistance1	R_{IND1}	―	100k	―	Ω	For pin REG4EN, ECO,SYNC
Input Pulldown Resistance2	R_{IND2}	―	660k	―	Ω	For pin EN
Output H level	V_{OH}	2.6	-	-	V	For pin BSENS,REG4OCB IO=1mA
Output L level	V_{OL}	-	-	0.8	V	For pin BSENS,REG4OCB IO= -1mA

Typical Performance Curves(reference)

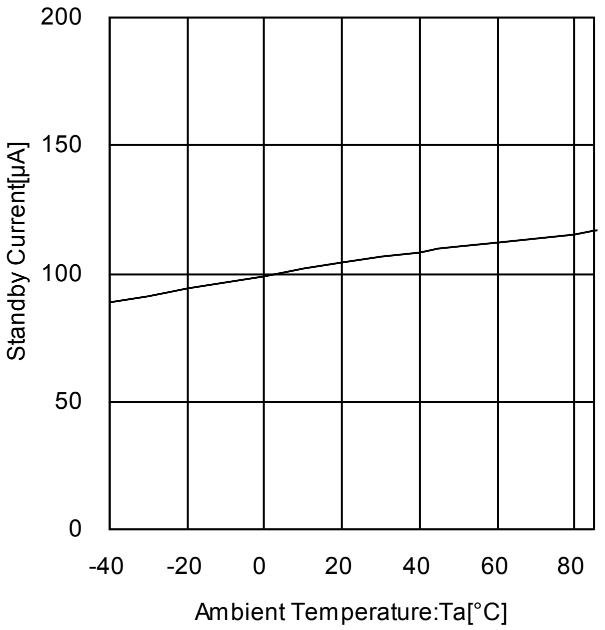


Figure 12. Standby Current vs Temperature

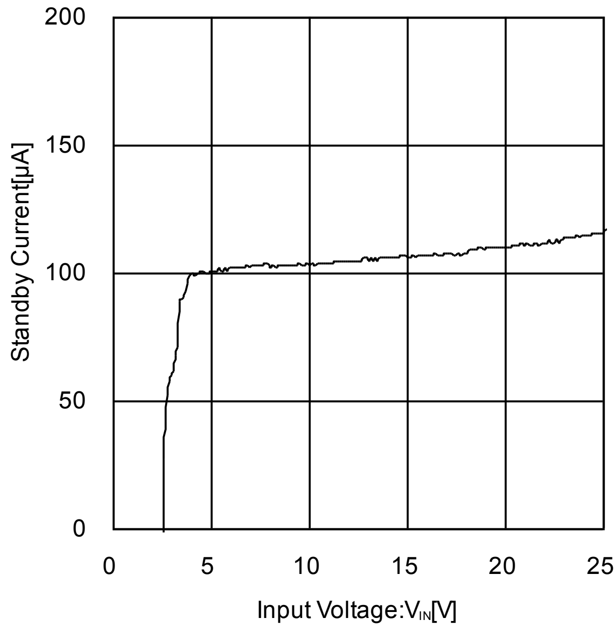


Figure 13. Standby Current vs Input Voltage

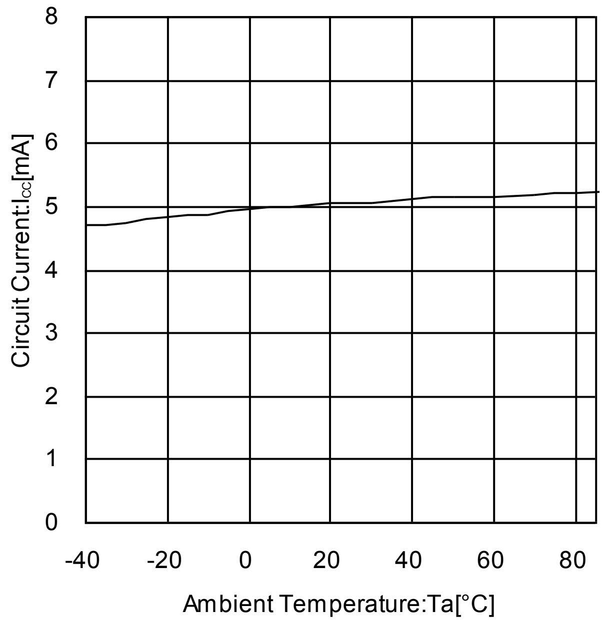


Figure 14. Circuit Current vs Temperature

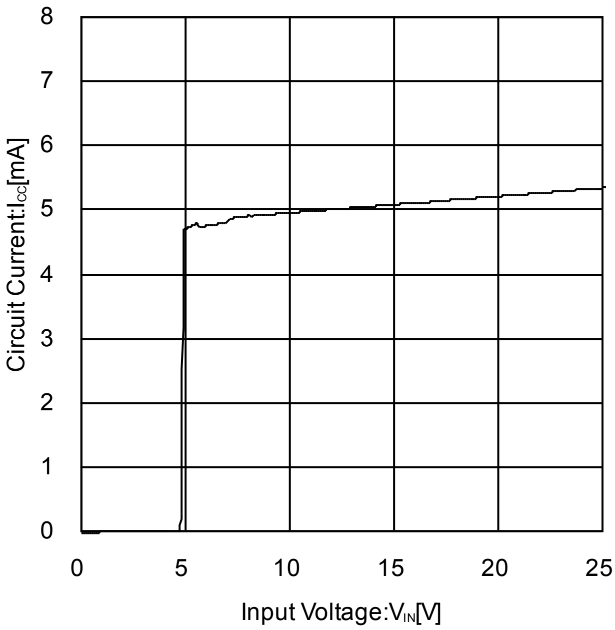


Figure 15. Circuit Current vs Input Voltage

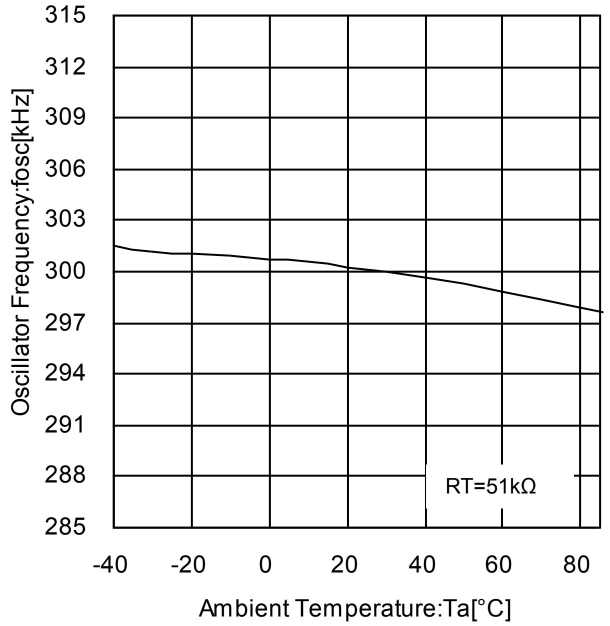


Figure 16. Oscillator Frequency vs Temperature

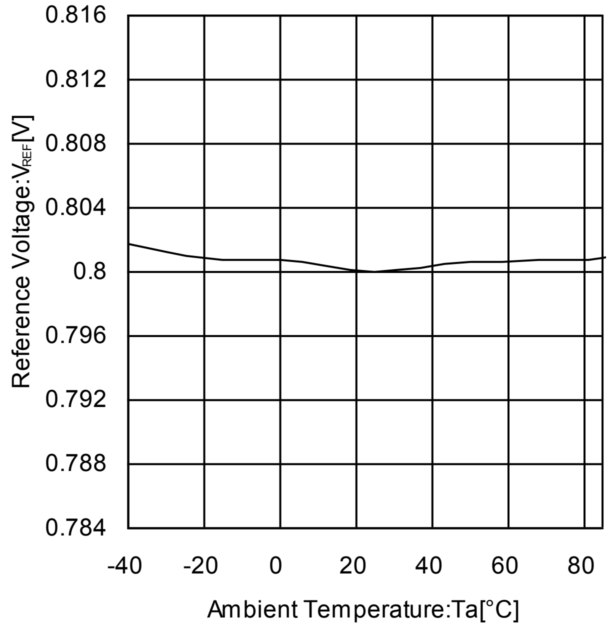


Figure 17. DCDC1 Reference Voltage vs Temperature

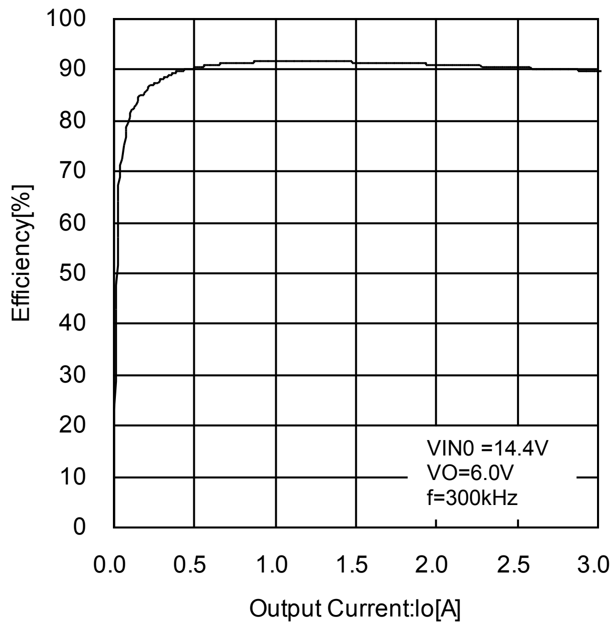


Figure 18. DCDC1 Efficiency vs Output Current

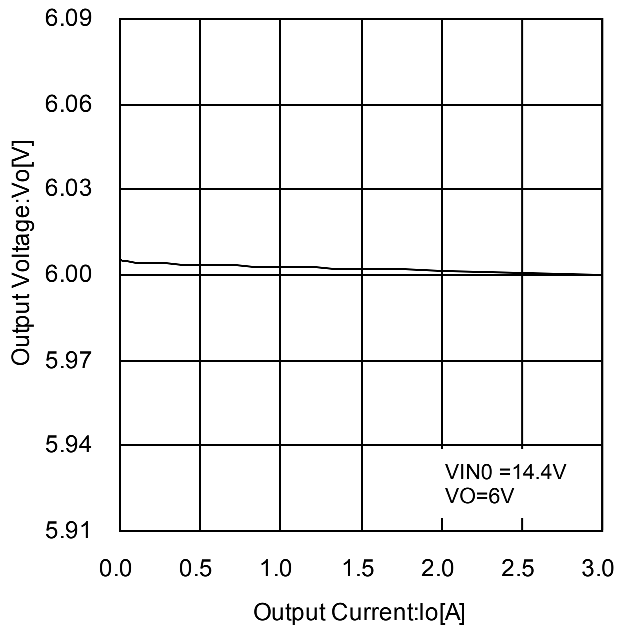


Figure 19. DCDC1 Output Voltage vs Output Current

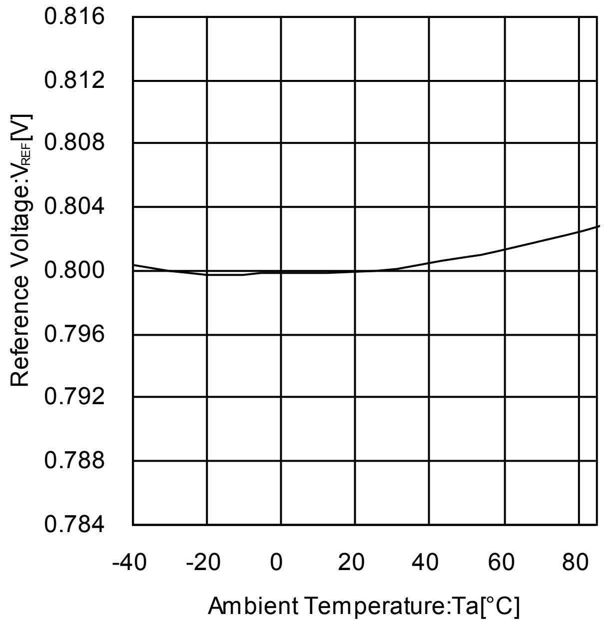


Figure 20. DCDC2 Reference Voltage vs Temperature

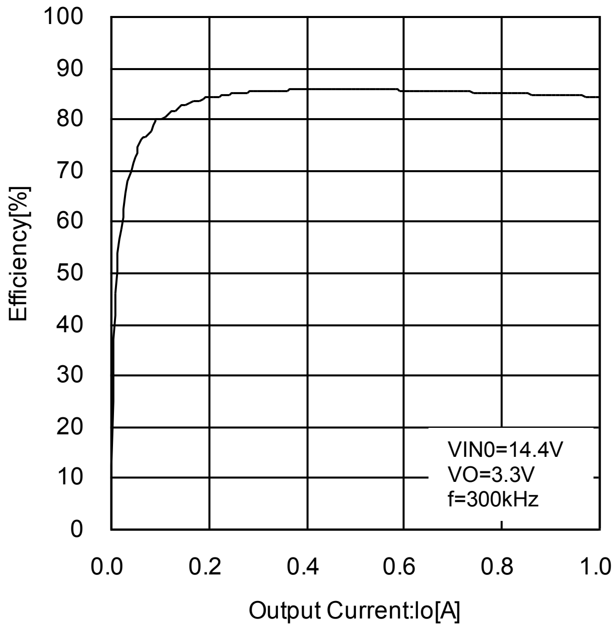


Figure 21. DCDC2 Conversion Efficiency vs Output Current

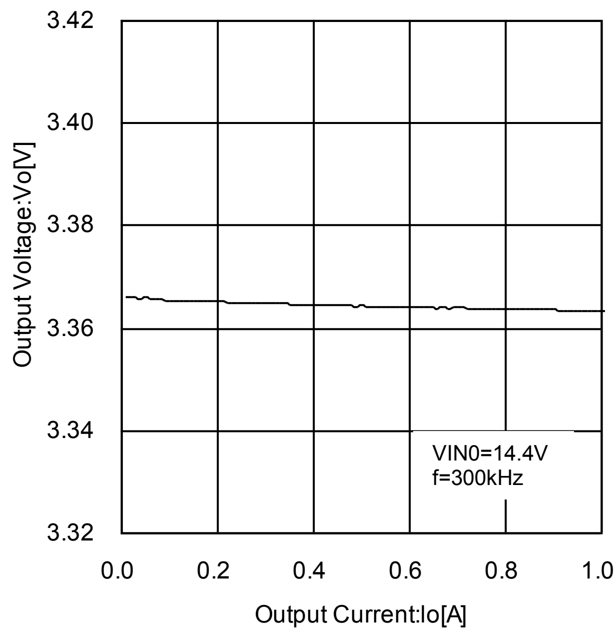


Figure 22. DCDC2 Output Voltage vs Output Current

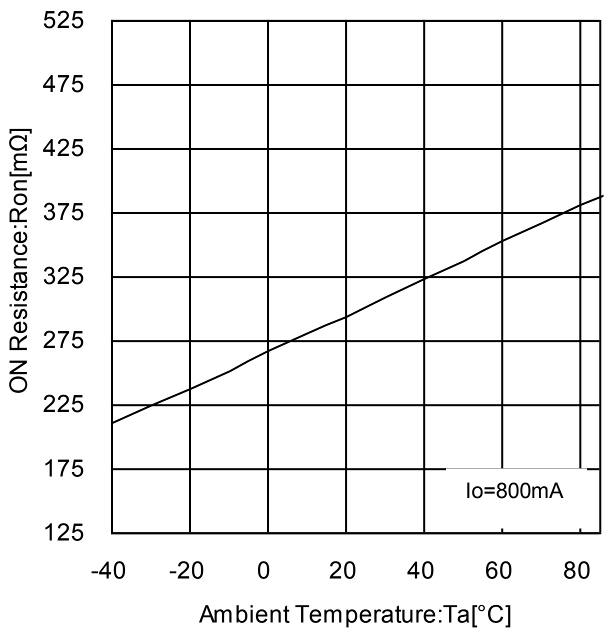


Figure 23. DCDC2 FET ON Resistance vs Temperature

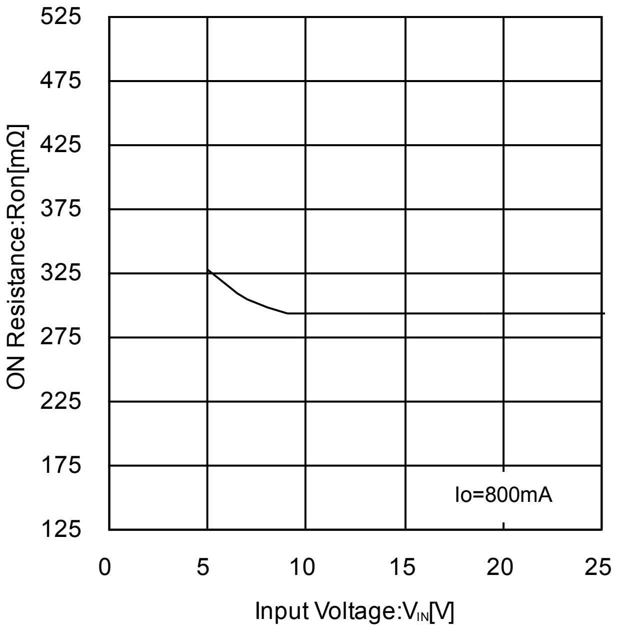


Figure 24. DCDC2 FET ON Resistance vs Input Voltage

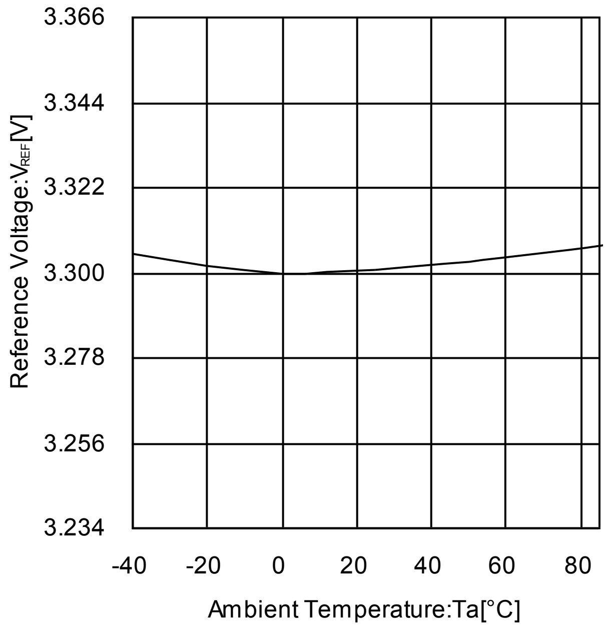


Figure 25. STBREG Reference Voltage vs Temperature

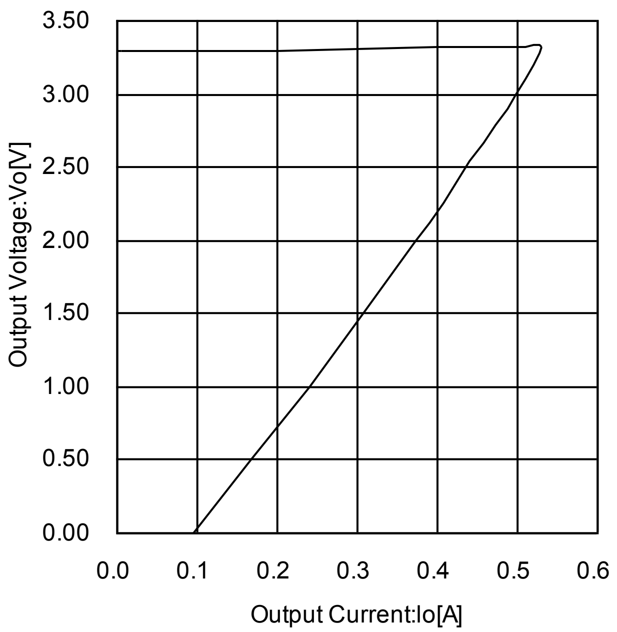


Figure 26. STBREG Output Voltage vs Output Current

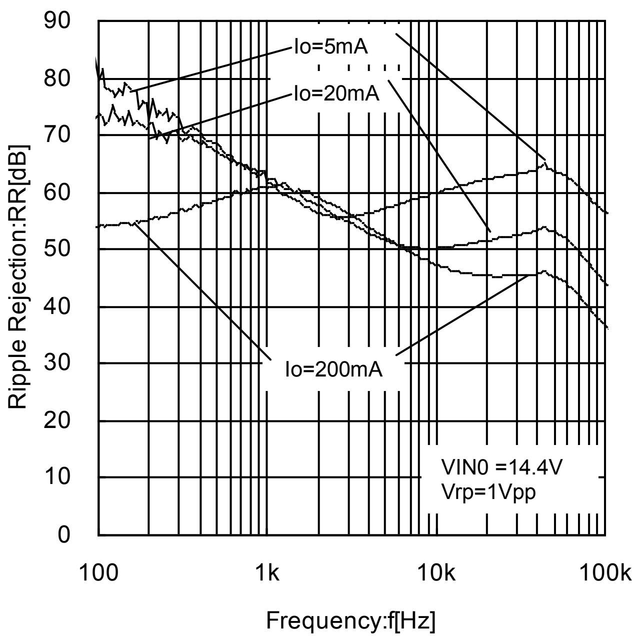


Figure 27. STBREG Ripple Rejection vs Frequency

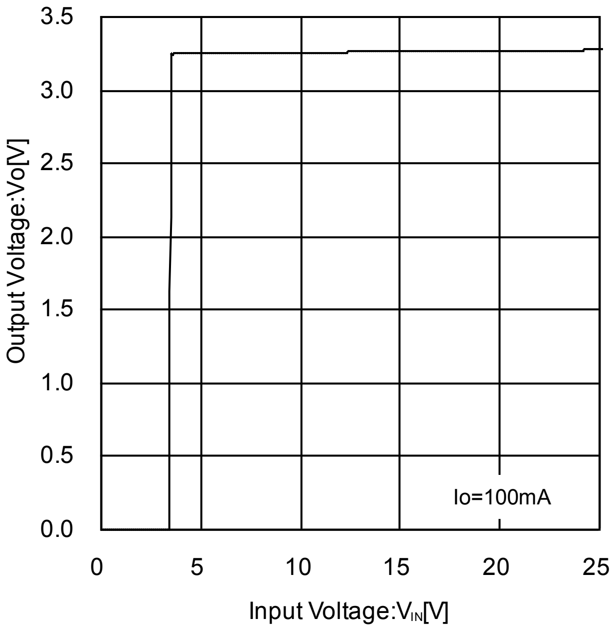


Figure 28. STBREG Output Voltage vs Input Voltage

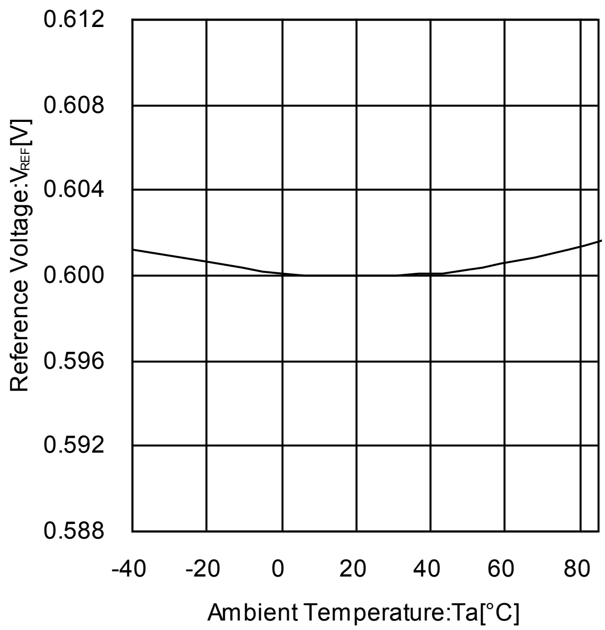


Figure 29. REG1 Reference Voltage vs Temperature

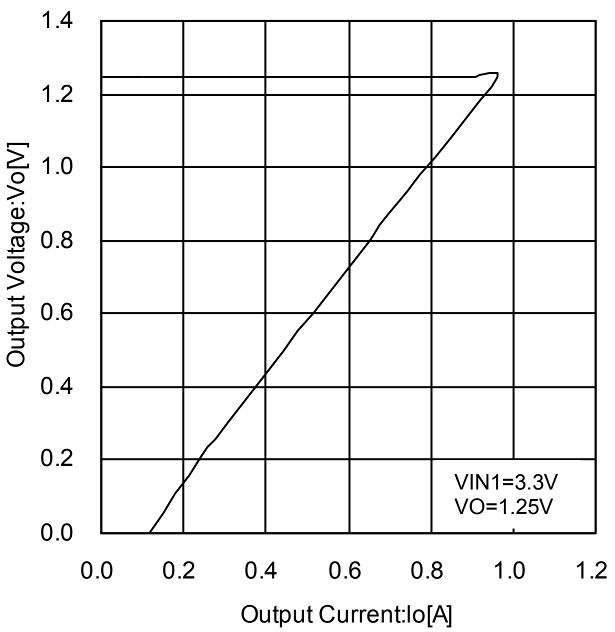


Figure 30. REG1 Output Voltage vs Output Current

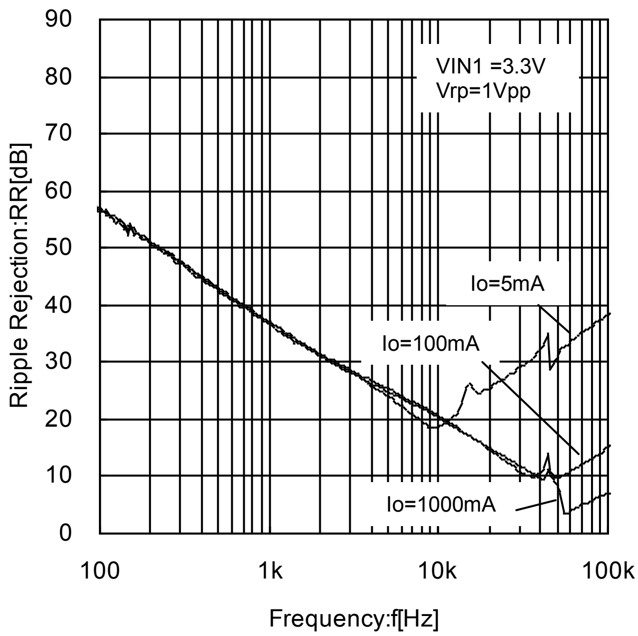


Figure 31. REG1 Ripple Rejection vs Frequency

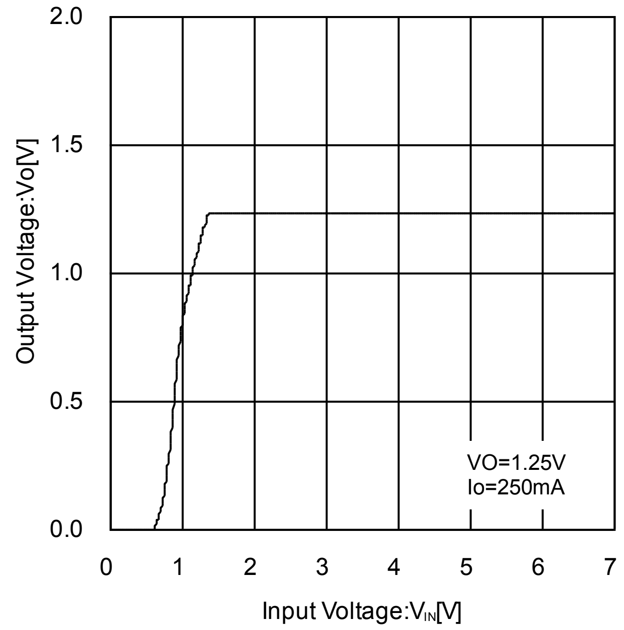


Figure 32. REG1 Output Voltage vs Input Voltage

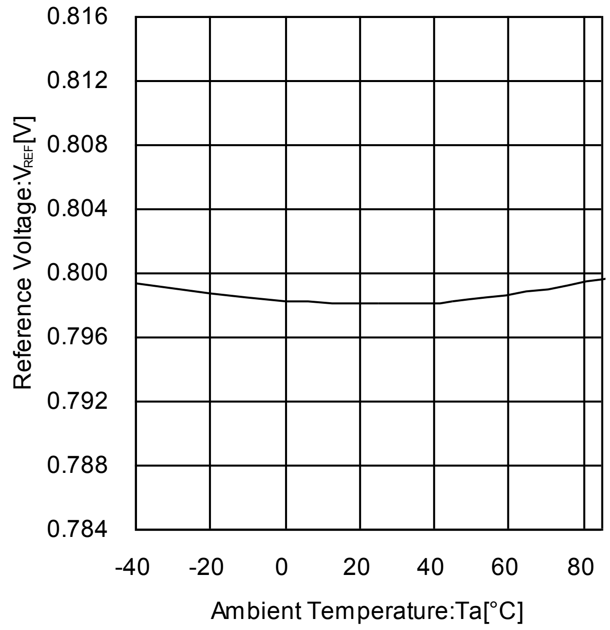


Figure 33. REG2 Reference Voltage vs Temperature

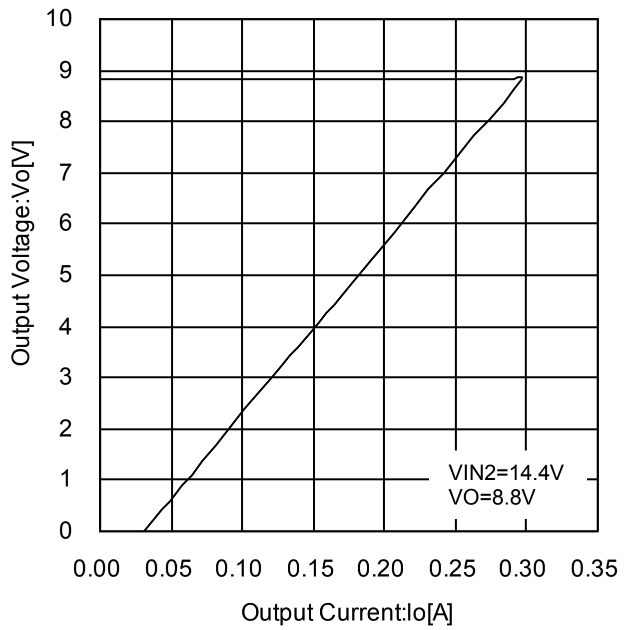


Figure 34. REG2 Output Voltage vs Output Current

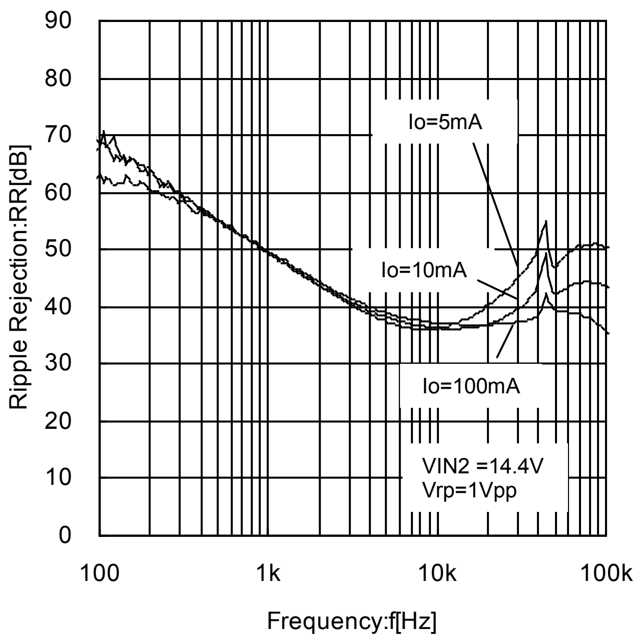


Figure 35. REG2 Ripple Rejection vs Frequency

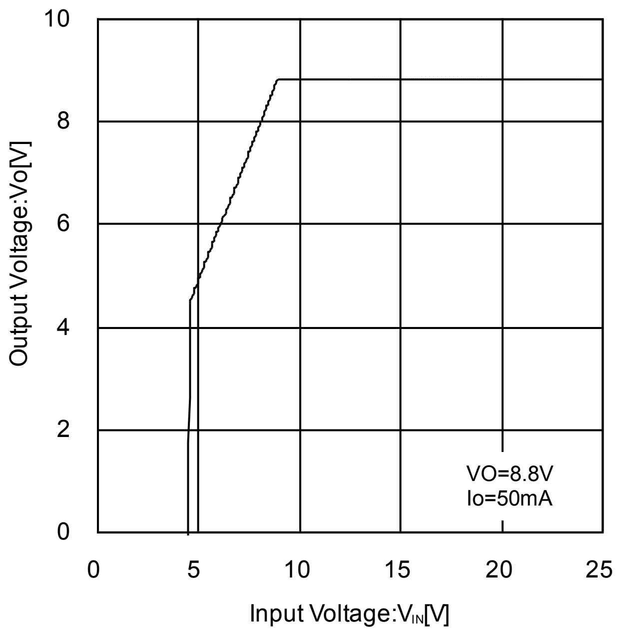


Figure 36. REG2 Output Voltage vs Input Voltage

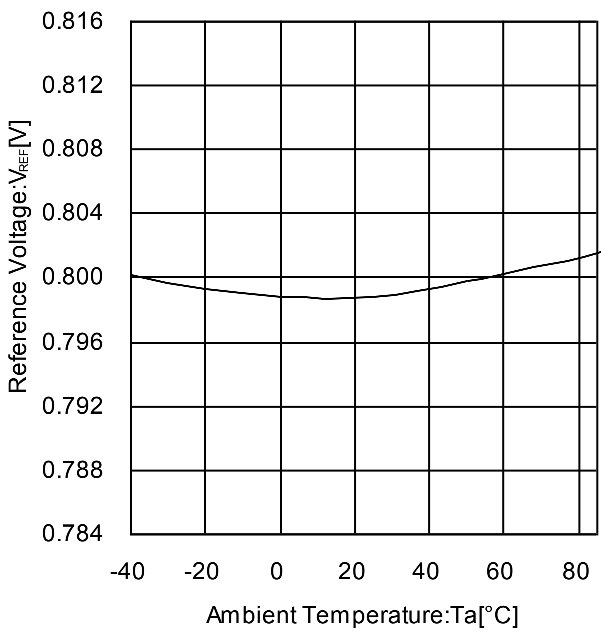


Figure 37. REG3 Reference Voltage vs Temperature

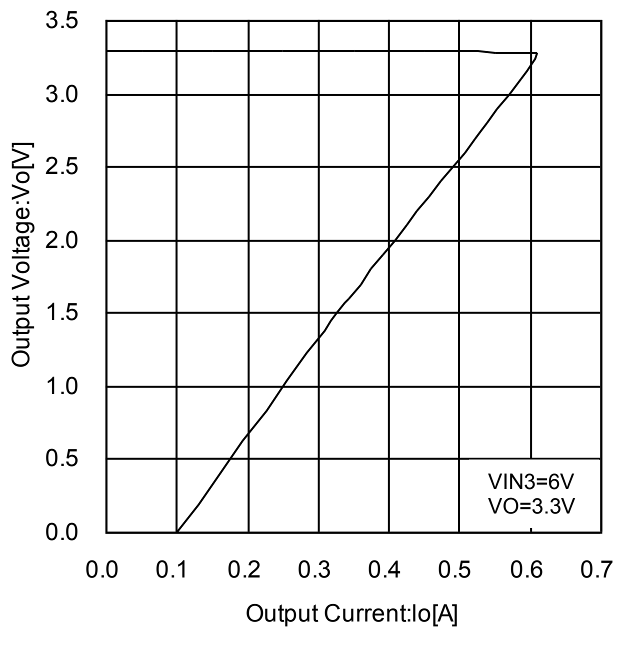


Figure 38. REG3 Output Voltage vs Output Current

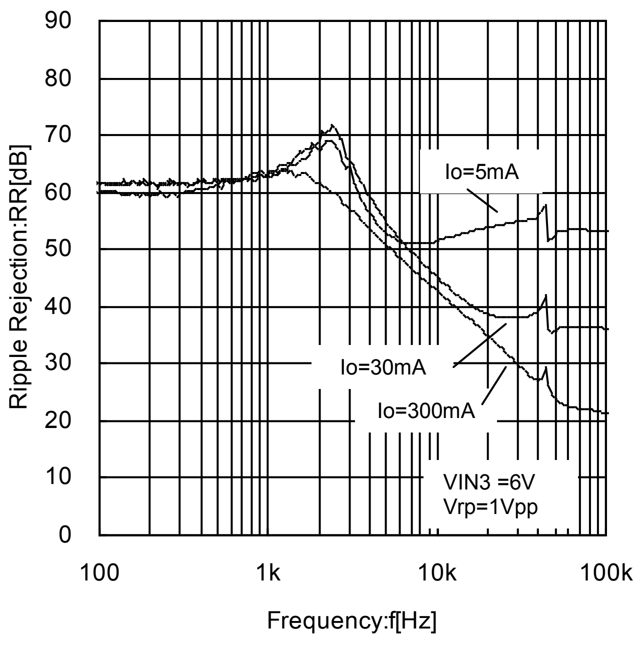


Figure 39. REG3 Ripple Rejection vs Frequency

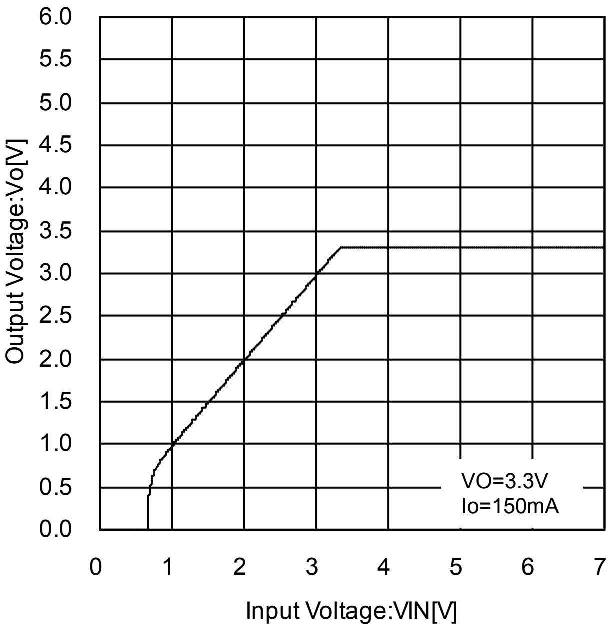


Figure 40. REG3 Output Voltage vs Input Voltage

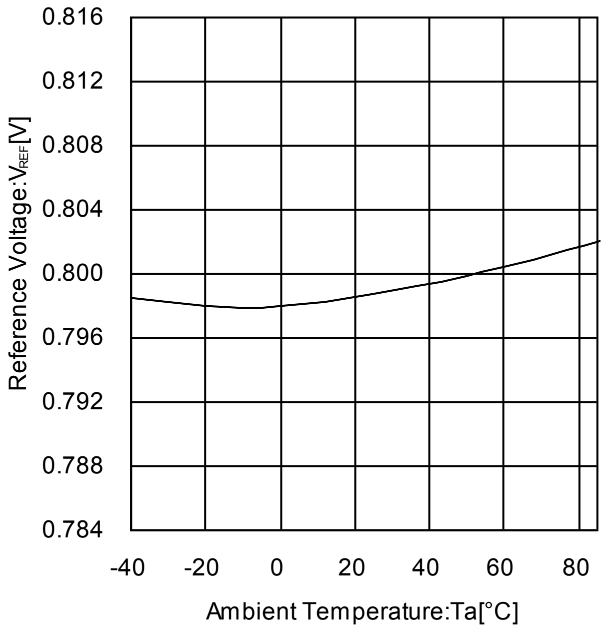


Figure 41. REG4 Reference Voltage vs Temperature

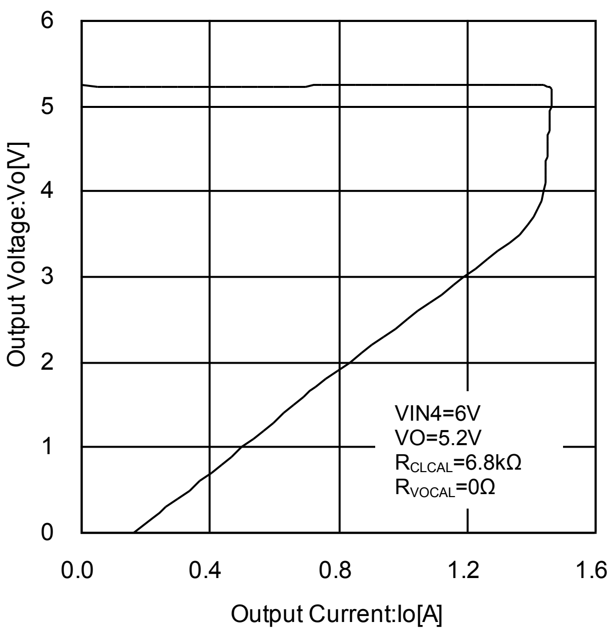


Figure 42. REG4 Output Voltage vs Output Current

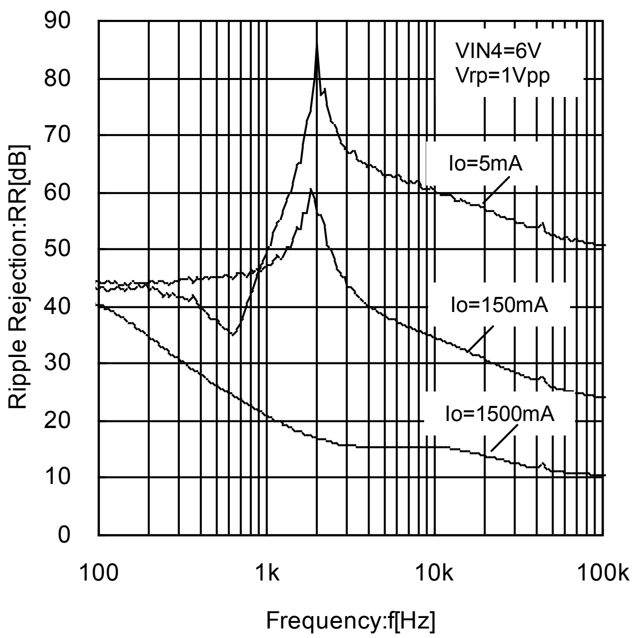


Figure 43. REG4 Ripple Rejection vs Frequency

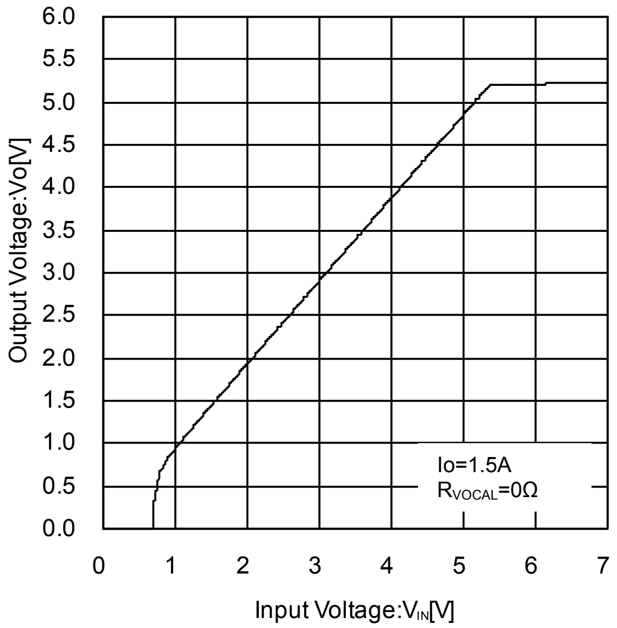


Figure 44. REG4 Output Voltage vs Input Voltage

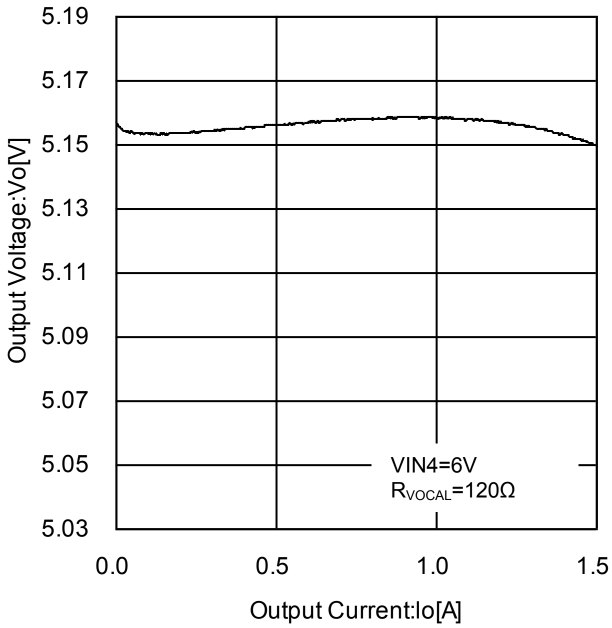


Figure 45. Voltage Adjusted for Cable Impedance vs Output Current

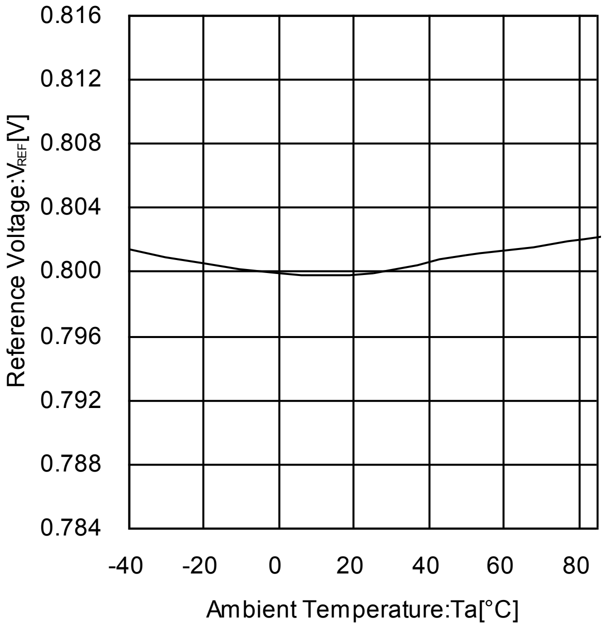


Figure 46. REG5 Reference Voltage vs Temperature

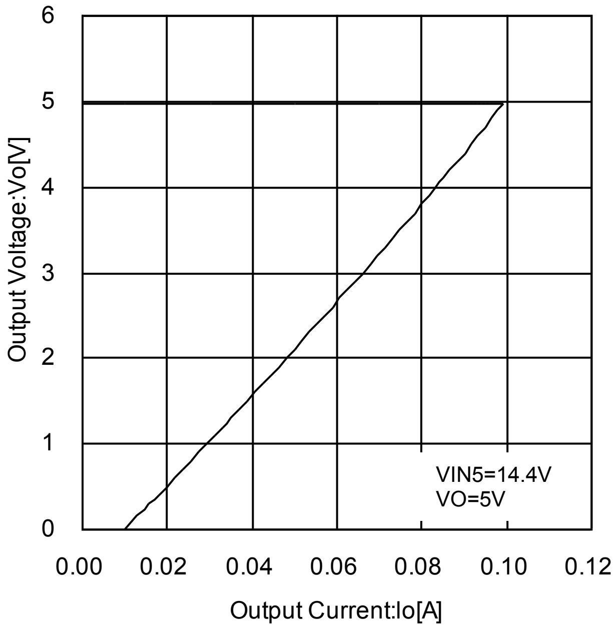


Figure 47. REG5 Output Voltage vs Output Current

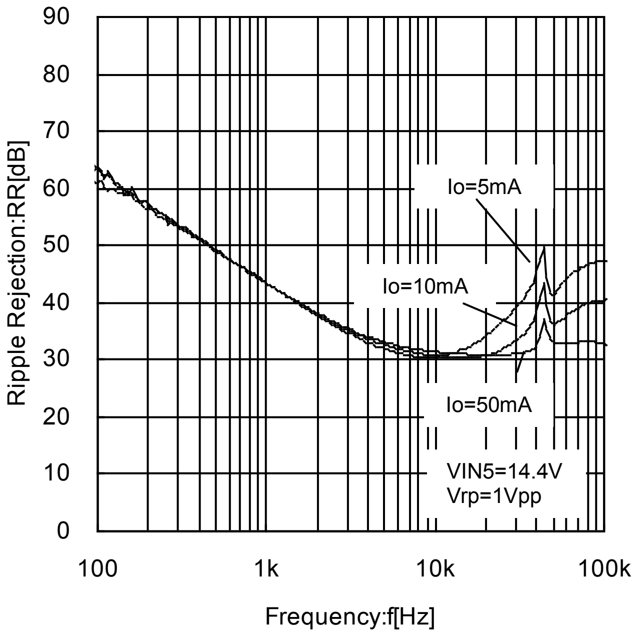


Figure 48. REG5 Ripple Rejection vs Frequency

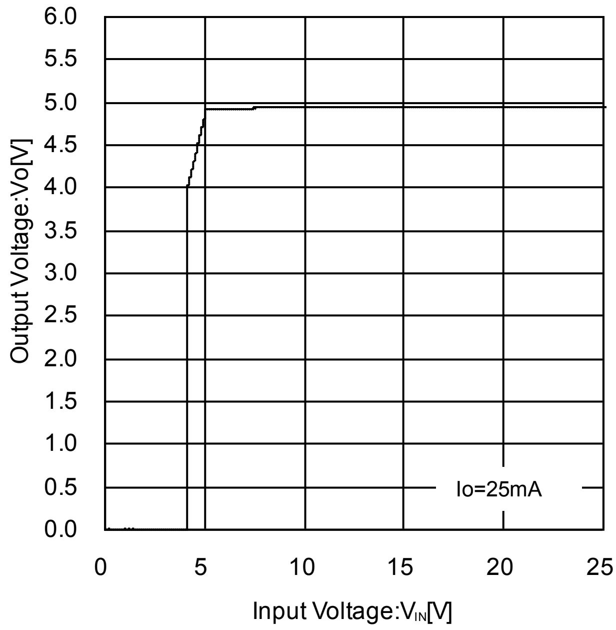


Figure 49. REG5 Output Voltage vs Input Voltage

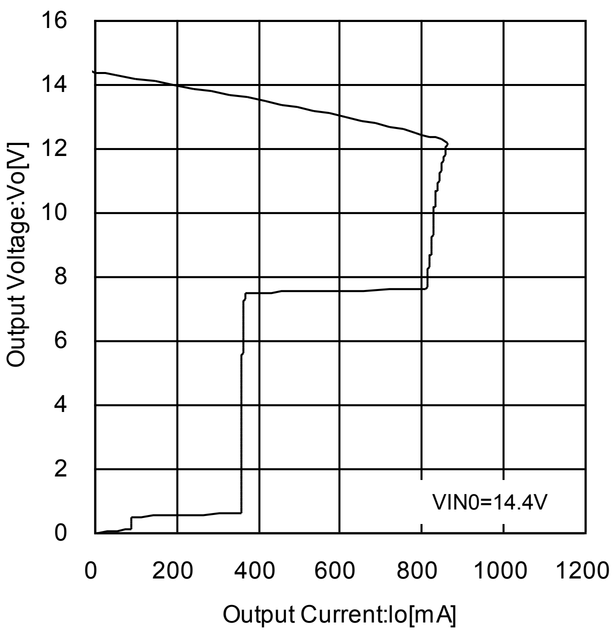


Figure 50. HSW Output Voltage vs Output Current

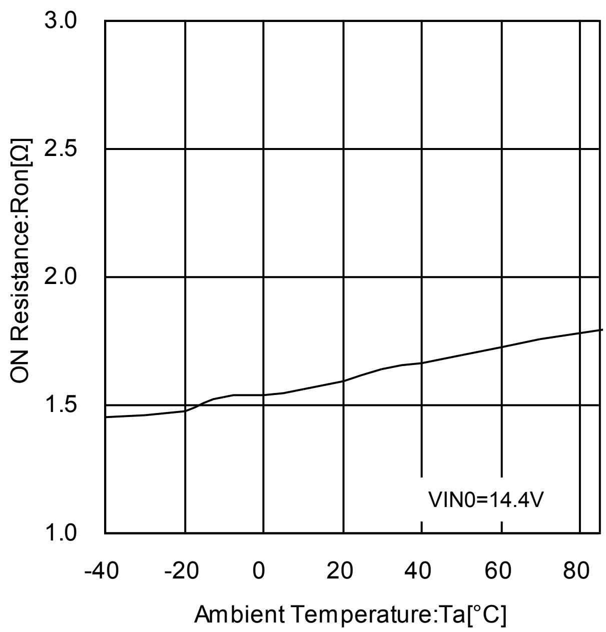


Figure 51. HSW ON Resistance vs Temperature

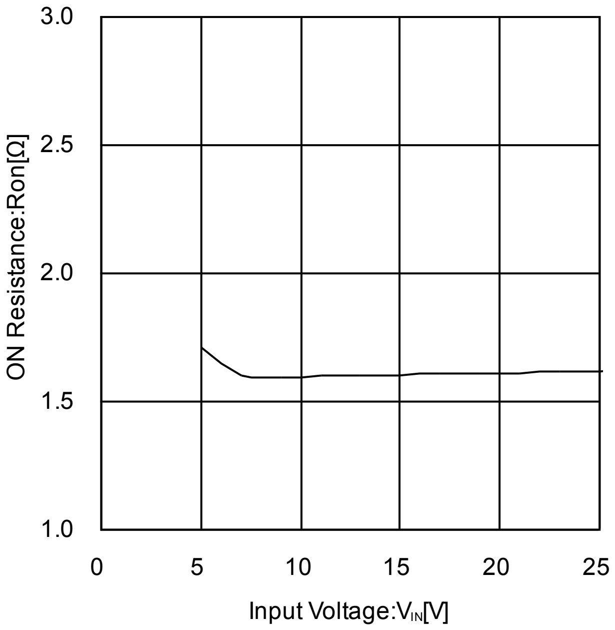


Figure 52. HSW ON Resistance vs Input Voltage

I^2C-bus Block

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

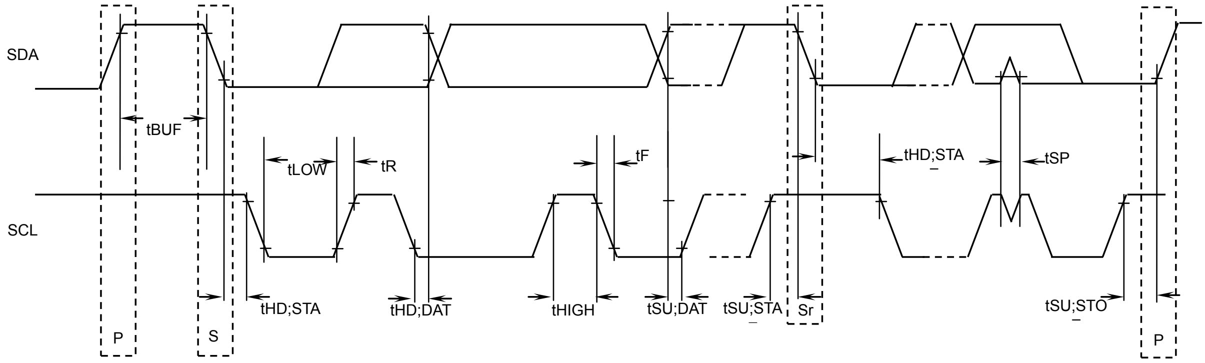


Figure 53. Definition of timing on the I^2C-bus

Table 1. Characteristics of the SDA and SCL Bus Lines for I^2C-bus Devices
(Unless specified particularly, Ta=25°C, VIN0=14.4V)

Parameter		Symbol	Fast-mode I^2C-bus		Unit
			Min	Max	
1	SCL Clock Frequency	fSCL	0	400	kHz
2	Bus Free Time between a STOP and START Condition	tBUF	1.3	—	μs
3	Hold Time (repeated) Start Condition (After this period, the first clock pulse is generated.)	tHD;STA	0.6	—	μs
4	LOW Period of the SCL Clock	tLOW	1.3	—	μs
5	HIGH Period of the SCL Clock	tHIGH	0.6	—	μs
6	Set-up Time for a Repeated START Condition	tSU;STA	0.6	—	μs
7	Data Hold Time	tHD;DAT	0.06 (Note 1)	—	μs
8	Data Setup Time	tSU;DAT	120	—	ns
9	Setup Time for STOP Condition	tSU;STO	0.6	—	μs

All values referred to VIH min and VIL max levels (see Table 2).

(Note 1) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH min. of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
About 7(tHD;DAT), 8(tSU;DAT), make it the setup which a margin is fully in .

Table 2. Characteristics of the SDA and SCL I/O stages for I^2C-bus Devices

Parameter		Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW Level Input Voltage:	VIL	-0.3	+1	V
11	HIGH Level Input Voltage:	VIH	2.3	5	V
12	Pulse Width of Spikes which must be suppressed by the input filter.	tSP	0	50	ns
13	LOW Level Output Voltage: at 3mA sink current	VOL1	0	0.4	V
14	Input Current each I/O pin with an input voltage between 0.4V and 4.5V.	Ii	-10	+10	μA

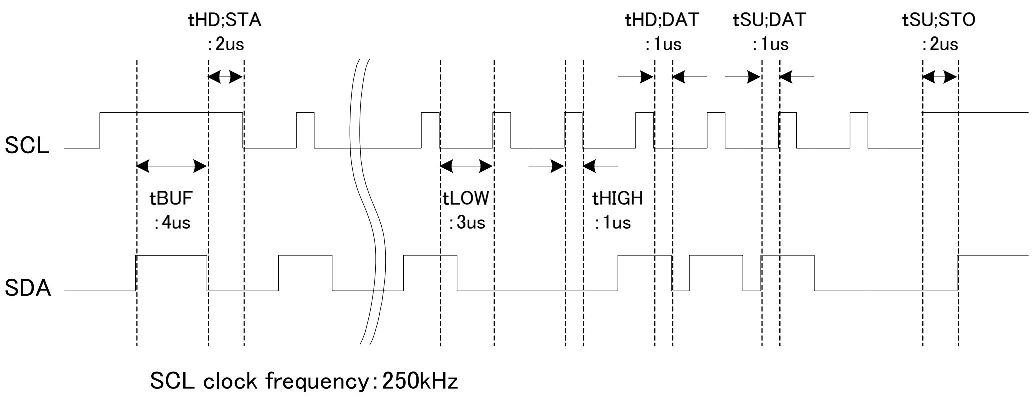


Figure 54. A Command Timing Example in the I^2C Data Transmission

(2)I²C-bus Format

MSB		LSB	MSB		LSB	MSB		LSB		

S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start Conditions (Recognition of Start Bit)
Slave Address = Recognition of Slave Address. 7 bits in upper order are voluntary. The least significant bit is "L" due to writing.
A = Acknowledge Bit (SDA "L")
$\overline{A}$ = Not Acknowledge Bit (SDA "H")
Select Address = Select ENABLE / LDET SETTING / HSW OCP.
Data = Data on ENABLE / LDET SETTING / HSW OCP
P = Stop Condition (Recognition of Stop Bit)

(3)I²C-bus Interface・Protocol

1)Write Mode Fundamental

S	Slave Address	A	Select Address	A	Data	A	P

MSB LSB MSB LSB MSB LSB

2)Auto Increment(The selection address does increment(+1) the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	・・・・	DataN	A	P

MSB LSB MSB LSB MSB LSB MSB LSB MSB LSB

(Example) ①Data 1 is set as data of the address specified in the selection address.
②Data 2 is set as data of the address specified in the selection address +1.
③Data N is set as data of the address specified in the selection address +N-1

3)Composition that cannot be transmitted(In this case, the selection address only 1 is set.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P

MSB LSB MSB LSB MSB LSB MSB LSB MSB LSB

(Attention) When you transmit data as selection address 2 next to data, it doesn't recognize as selection address 2, and it recognizes it as data.

4)Read Mode Protocol(Address 0x04 Read)

S	Slave Address	A	REQ Address	A	Select Address	A	P

MSB 0xD8 LSB MSB 0xD0 LSB MSB 0x04 LSB

S	Slave Address	A	※READ DATA	$\overline{A}$	P

MSB 0xD9 LSB MSB LSB

Because read data outputs with synchronizing with falling edge of SCL, it latches with synchronizing with rising edge of SCL.

(4)Slave Address

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	1	0	0	1/0

Register Map

Items	Select Address	init	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
ENABLE	01	0x02	—	HSW_EN	REG5_EN	REG4_EN	REG3_EN	REG2_EN	REG1_EN	DCDC1_EN
LDET SETTING	02	0x09	—	—	—	—	LDET[3:0]			
HSW OCP	04	0x00	—	—	—	—	—	—	—	HSW OCP

・Select Address 01 : ENABLE

Items	Select Address	init	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
ENABLE	01	0x02	—	HSW_EN	REG5_EN	REG4_EN	REG3_EN	REG2_EN	REG1_EN	DCDC1_EN

D[0]: DCDC1_EN ・・・DCDC1 enable control.
"0": OFF (Initial Value)
"1": ON

D[1]: REG1_EN ・・・REG1 enable control.
"0": OFF
"1": ON (Initial Value)

D[2]: REG2_EN ・・・REG2 enable control.
"0": OFF (Initial Value)
"1": ON

D[3]: REG3_EN ・・・REG3 enable control.
"0": OFF (Initial Value)
"1": ON

D[4]: REG4_EN ・・・REG4 enable control.
"0": OFF (Initial Value)
"1": ON

D[5]: REG5_EN ・・・REG5 enable control.
"0": OFF (Initial Value)
"1": ON

D[6]: HSW_EN ・・・HSW enable control.
"0": OFF (Initial Value)
"1": ON

・Select Address 02 : LDET SETTING

Items	Select Address	init	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
LDET SETTING	02	0x09	—	—	—	—	LDET[3:0]			

D[3:0]: LDET ・・・ The low voltage detect threshold of the pin VIN0 is set. When the pin VIN0 becomes below the set threshold, the pin BSENS becomes L.

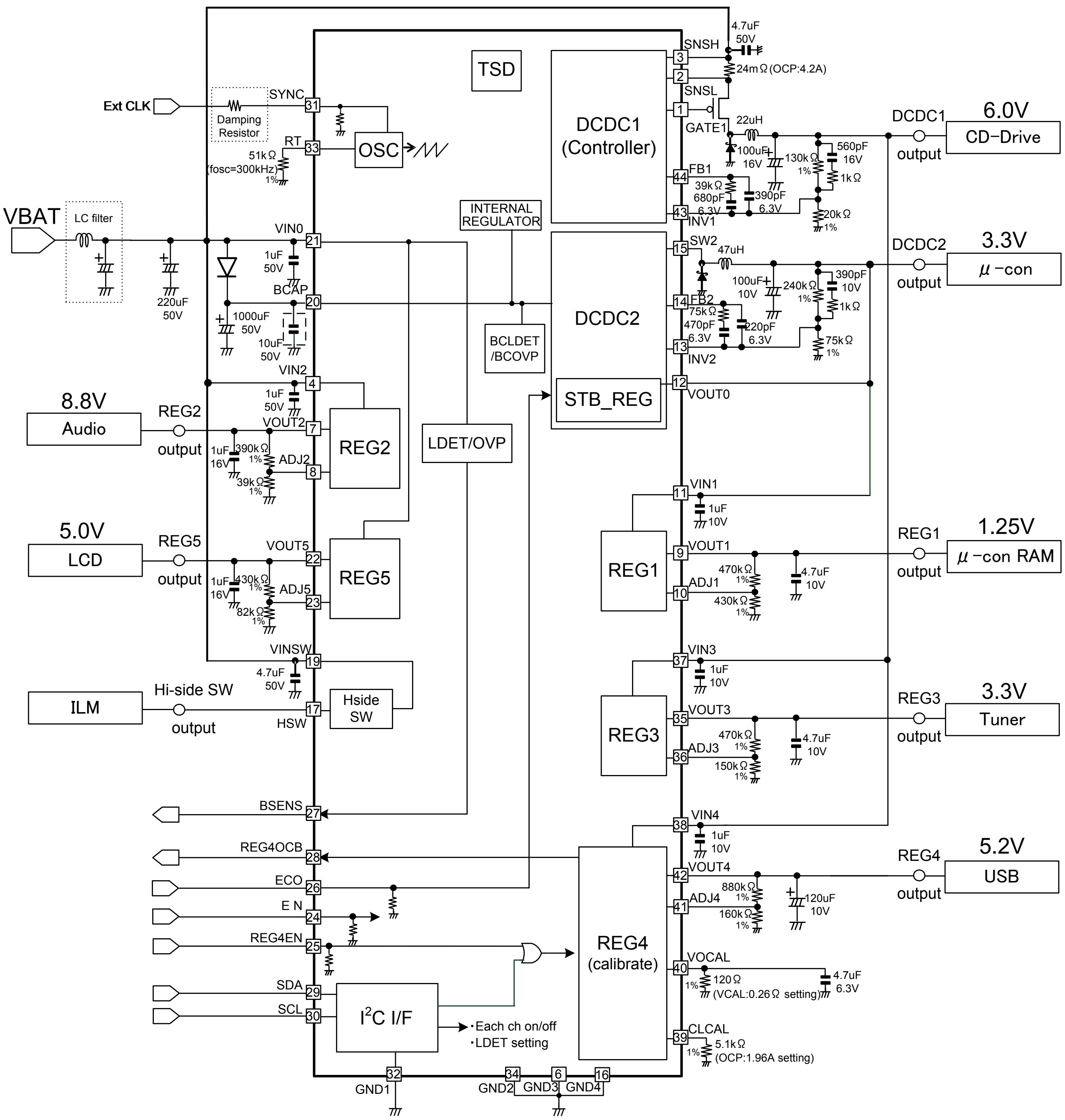
"0000":	5.7V	"1000":	7.7V
"0001":	5.8V	"1001":	7.8V (Initial Value)
"0010":	5.9V	"1010":	7.9V
"0011":	6.0V	"1011":	8.0V
"0100":	6.1V	"1100":	8.1V
"0101":	6.2V	"1101":	8.2V
"0110":	6.3V	"1110":	8.3V
"0111":	6.4V	"1111":	8.4V

・Select Address 04 : HSW OCP (Read only)

Items	Select Address	Init	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
HSW OCP	04	0x00	—	—	—	—	—	—	—	HSW OCP

D[0]: HSW OCP ・・・ Detecting HSW over current condition
"0": No detected (Initial Value)
"1": Detected

Application Example



[ ] Please put this BCAP capacitor near BCAP pin as much as possible.

※ We recommend you use less than 1% accuracy resistor with voltage, frequency, OCP datect and cable compensation setting.

※ This is an example. Please decide all parts after enough evaluations and verifications.

Figure 55. Application Example

Selection of Components Externally Connected

1. Setting External Components for DCDC

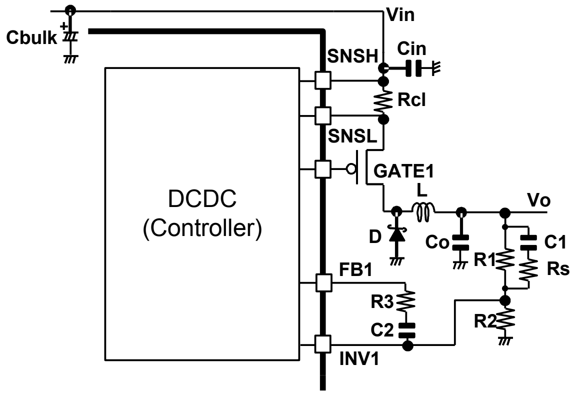


Figure 56. External Components for DCDC

(1) Setting Output Voltage

To set output voltage, connect R1 between VOUT and INV, R2 between INV and GND.
Furthermore, set the R1 and R2 to 10k–1MΩ.

$VOUT = V_{INV}$ x (R1 + R2)/R2 [V]

V_{INV} : INV Voltage 0.8V(Typ),

(2) Selection of Coil L

The value of the coil can be obtained by the formula shown below:

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times f \times \Delta I_L}$$

ΔI_L: Output Ripple Current

ΔI_L should typically be approximately 20 to 30% of Iomax (the maximum load current of DCDC)

If this coil is not set to the optimum value, normal (continuous) oscillation may not be achieved. Furthermore, set the value of the coil with an adequate margin so that the peak current passing through the coil will not exceed the rated current of the coil.

(3) Selection of Output Capacitors

The output capacitor can be determined according to the output ripple voltage ΔVpp required. Obtain the required ESR value by the formula shown below and then select the capacitance.

$$\Delta I_L = \frac{(V_{IN} - V_O) \times V_O}{L \times f \times V_{IN}}$$

$$\Delta Vpp = \Delta I_L \times ESR + \frac{\Delta IL \times V_O}{2 \times Co \times f \times V_{IN}}$$

Set the rating of the capacitor with an adequate margin to the output voltage. Also, set the maximum allowable ripple current with an adequate margin to ΔIL. Furthermore, the output rise time should be shorter than the soft start time. Select the output capacitor having a value smaller than that obtained by the formula shown below.

$$C_{MAX} = \frac{1.7ms \times \{ I_{LIMIT} - I_O(Max) \}}{V_O}$$

I_{LIMIT}: DCDC Over Current Limit Value 0.1/Rcl[A] (DCDC1)
3.6 [A] (DCDC2)

Rcl: Resistance between SNSH and SNSL

If these capacitances are not optimum, faulty startup may result.
(※1.7m is soft start time(min))

(4) Selection of Diodes

Set diode rating with an adequate margin to the maximum load current. Also, make setting of the rated inverse voltage with an adequate margin to the maximum input voltage.
A diode with a low forward voltage and short reverse recovery time will provide high efficiency.

(5) Selection of Input Capacitors
Be sure to insert a ceramic capacitor of 2 to 10µF for C_{in}
Furthermore, connect the capacitor C_{bulk} to keep input voltage.
The capacitor C_{bulk} should have a low ESR and a significantly large ripple current. The ripple current IRMS can be obtained by the following formula:

$$IRMS = Io \times \sqrt{Vo \times (Vin - Vo) / Vin^2}$$

Select capacitors that can accept this ripple current.
If the capacitance of C_{IN} and C28 is not optimum, the IC may malfunction.

(6) Setting of Phase Compensation
The following section summarizes the targeted characteristics of this application for the stability condition of DCDC.

- At a 1(0dB)gain, the phase delay is 150°or less(i.e. the phase margin is 30° or more).
- The GBW for this occasion is 1/10 or less of the switching frequency.

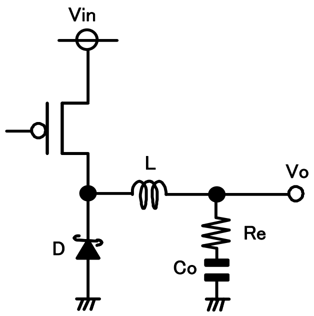


Figure 57. LC Filter of DCDC

$$f_r = \frac{1}{2\pi \times \sqrt{L \times Co}} \quad \text{[Hz] (LC Resonance Point)}$$

$$f_{ESR} = \frac{1}{2\pi \times Re \times Co} \quad \text{[Hz] (Phase Lead)}$$

Replace a secondary phase delay(-180°) with a secondary phase lead by inserting two-phase leads, to ensure the stability through the phase compensation.

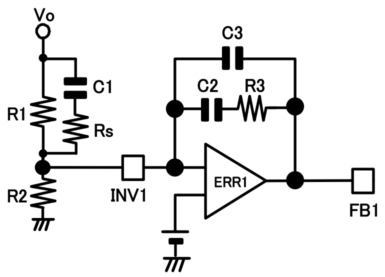


Figure 58. Phase Compensation

$$f_{z1} = \frac{1}{2\pi \times R1 \times C1} \quad \text{[Hz] (Phase Lead)}$$

$$f_{z2} = \frac{1}{2\pi \times R3 \times C2} \quad \text{[Hz] (Phase Lead)}$$

Setting fz1,fz2 to be half to 2 times a frequency as large as fr provides an appropriate phase margin.
For output capacitors that have high ESR, because f_{ESR}(phase lead) occurs near LC resonance point, it is unnecessary to insert fz1(phase lead).
For output capacitors that have low ESR, insert fz1(phase lead) and fp1 obtained by the following formula and adjust frequency response.

$$f_{p1} = \frac{C2 + C3}{2\pi \times R3 \times C2 \times C3} \quad \text{[Hz] (Phase Delay)}$$

The setting value above is simple estimate. Consequently, the setting may be adjusted on the actual system. Furthermore, since these characteristics vary with the layout of PCB loading conditions, precise calculations should be made on the actual system.
To check on the actual frequency characteristics, use a FRA or a gain-phase analyzer. Moreover, there is a method of guessing the room degree by the loading response, too, when these measuring instruments do not exist. The response is low when the change of the output when it is made to change under no load to the maximum load is monitored, and there are a lot of variation quantities. It can be said that the phase margin degree is little when there are a lot of ringing frequencies after it changes. As the standard, it is two times or more of ringing. However, a quantitative phase margin degree cannot be confirmed.

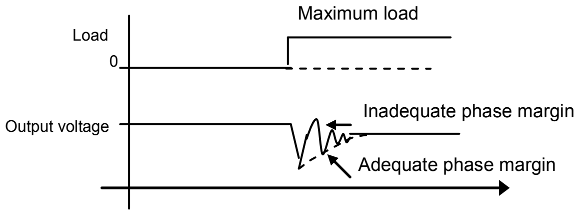


Figure 59. Load Response

(7) Setting of the Threshold for DCDC1 Over Current Protection
When the peak of the inductor current gets over the over current protection values, over current protection circuit operates. The over current protection values can be obtained by the following formula:

$$Iocp = \frac{100mV}{Rcl}$$

(8) Selection of the Pch FET for DCDC1

- VDS＜-Vin
- VGS＜-5V(Typ)
- Allowable Current ＞ Output Current + Ripple Current

※Recommended more than the threshold for over current protection
※The FET with low on resistance will provide high efficiency.

2. Setting External Components for REG

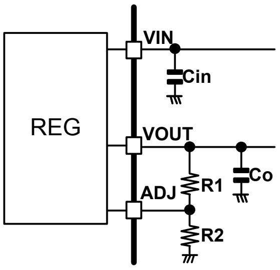


Figure 60. External Components for REG

ch	Output Voltage[V]	Input Voltage Range[V]			OCP Current Threshold[A]			Output Capacitance[μF]		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
REG1	1.25	2.25(Note 1)	3.3	6.5	0.5	1.0	1.5	4.7	-	-
REG2	8.8	9.45(Note 1)	14.4	25	0.15	0.30	0.45	1	-	-
REG3	3.3	3.9(Note 1)	6	6.5	0.3	0.6	0.9	4.7	-	-
REG4	5.2	5.6(Note 1)	6	6.5	Typ-20%	Variable	Typ+20%	47	-	-
REG5	5	5.65(Note 1)	14.4	25	0.05	0.10	0.15	1	-	-

(Note 1) the value when Output Voltage is indicated above

Figure 61. Each REG's Specification of BD49101ARFS-M

(1) Setting Output Voltage
To set output voltage, connect R2 between ADJ and GND, R1 between VOUT and ADJ.
Furthermore, set the R1 to 100kΩ(400kΩ for REG3) or more.

$$VOUT = V_{ADJ} \times (R1+R2)/R2 \text{ [V]}$$

V_{ADJ}:ADJ Voltage(=Reference Voltage) REG3,REG4,REG5: 0.8V(Typ),
REG1: 0.6V(Typ),
REG2: 0.793V(Typ)

(2) Selection of Output Capacitors
To prevent from oscillation, insert output capacitor. Check to Figure 61 about minimum capacitance of each REG. (Temperature characteristic is excluded) It may be use ceramic capacitors.
Because steep change and input voltage change have effect on output voltage change, please confirm output capacitance in actual application.

(3) Over Current Protection(OCP) Threshold
The OCP threshold depends on output voltage setting value. Especially if you set lower voltage than indicated shown as Figure 61, OCP threshold value decrease.

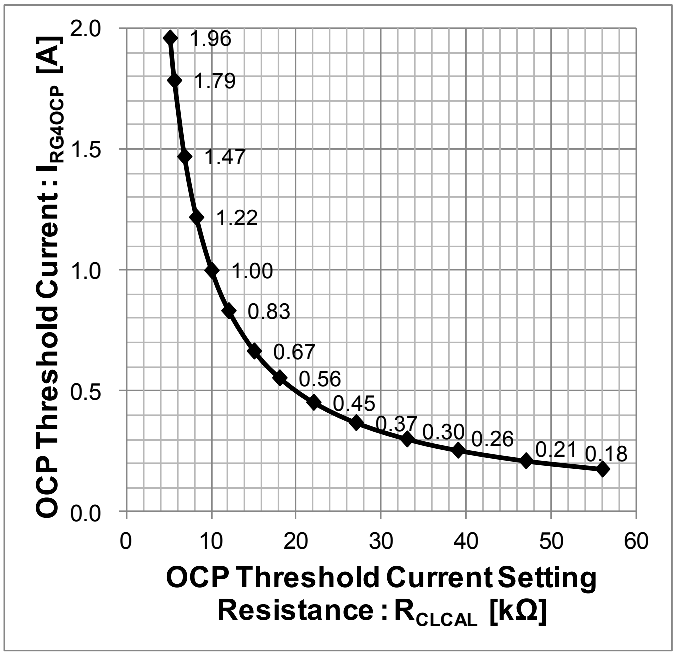
(4) Setting of REG4 Over Current Protection Threshold and Cable Impedance Calibration

① Setting of Over Current Protection Threshold

The over current protection threshold (I_{RG4OCP}) can be set by the resistance connected with CLCAL (R_{CLCAL}).
The threshold can be obtained by the following formula (Typical Characteristic)

$R_{CLCAL}[\Omega] = 5.1k \times 1.96A / I_{RG4OCP}[A]$

The relation between resistance and the threshold is decided as shown in the figure below.



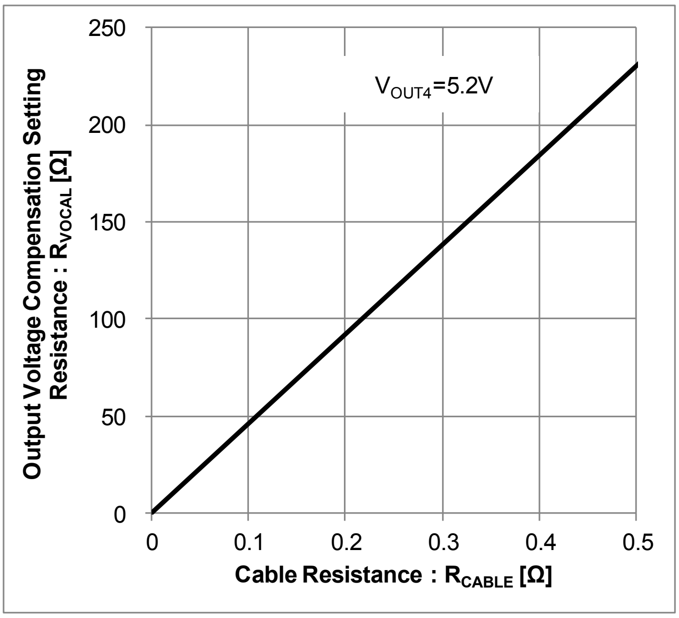
R_{CLCAL}[kΩ]	I_{RG4OCP}[A]
5.1	1.96
5.6	1.79
6.8	1.47
8.2	1.22
10.0	1.00
12.0	0.83
15.0	0.67
18.0	0.56
22.0	0.45
27.0	0.37
33.0	0.30
39.0	0.26
47.0	0.21
56.0	0.18

Figure 62. Setting of Over Current Protection Threshold

② Setting of Cable Impedance Calibration

The cable impedance (R_{CABLE}) calibration value can be set by the resistance connected with the VOCAL pin (R_{VOCAL}).
This value can be obtained by the following formula (Typical Characteristic):

$R_{VOCAL}[\Omega] = R_{CABLE}[\Omega] \times 2400 / VOUT4$
V_{OUT4}: REG4 Output Setting Value(Typ)



R_{CABLE}[Ω]	R_{VOCAL}[Ω] VOUT4=5.2V
0.000	0
0.022	10
0.039	18
0.085	39
0.163	75
0.217	100
0.238	110
0.260	120
0.282	130
0.325	150
0.347	160
0.390	180
0.433	200
0.477	220
0.520	240

Figure 63. Setting of Cable Impedance Calibration

When you set cable impedance, please assume VOUT4 absolute maximum rating(7.0V) and I/O voltage difference(0.4V max) so that the cable impedance calibration cause rising output voltage.

③Setting of the VOCAL Capacitor

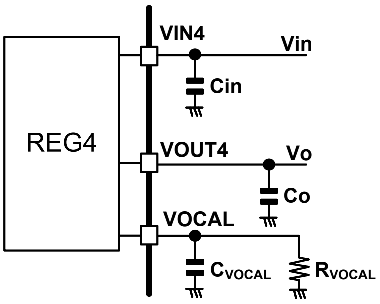


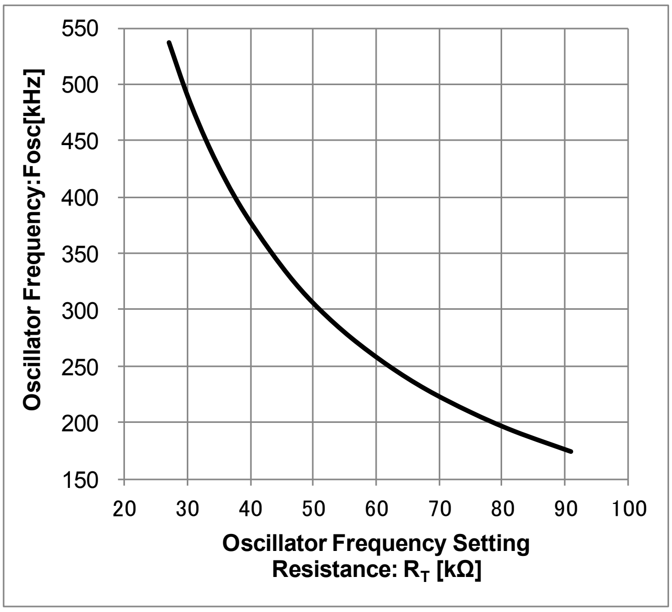
Figure 64. Capacitance of the VOCAL pin (C_{VOCAL})

For the oscillation of REG4 cable impedance calibration circuit, insert more than 4.7μF capacitor to VOCAL as shown above.

(5) The VOUT0 Pin Setting
Be sure to connect DCDC2 output with the VOUT0 pin. (refer to Figure 55.)
The VOUT0 pin is a power supply for I/O pin (24-31pin). Therefore, if VOUT0 and VODC2 output would not be connected, you could not set external synchronization, register and DCDC2/STBREG mode or could not get BSENS or REG4OCB output signal.

3. Setting the Oscillator Frequency (F_{OSC})

An internal oscillator frequency can be set by the resistance connected with the RT pin.
The relation between resistance and the oscillator frequency is decided as shown in the figure below. (Typical Characteristic)



R_T[kΩ]	F_{OSC}[kHz]
27	537
30	489
33	449
36	415
39	386
43	353
47	324
51	300
56	275
62	250
68	229
75	209
82	192
91	174

Figure 65. Oscillator Frequency vs R_T

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
HTSSOP-A44R				
Junction to Ambient	θ_{JA}	75.7	49.6	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	6	6	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

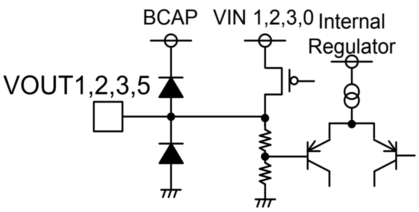
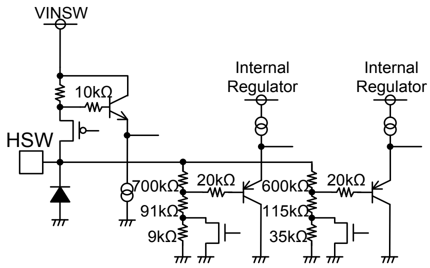
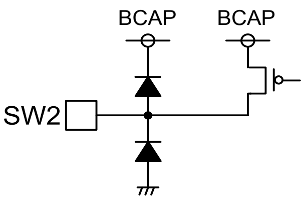
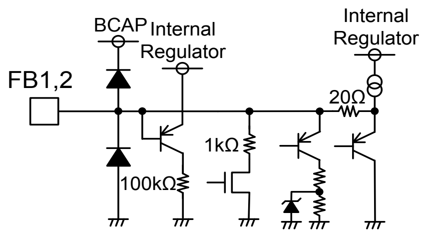
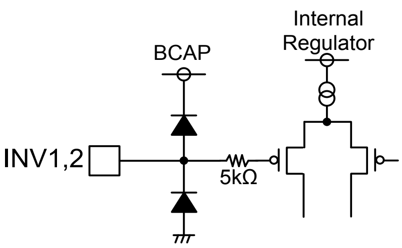
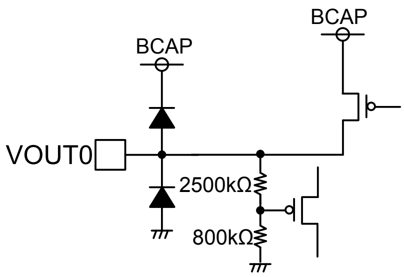
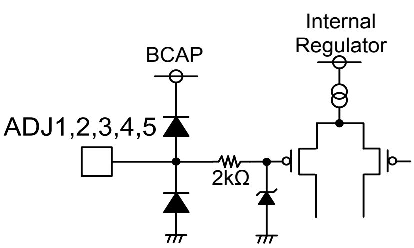
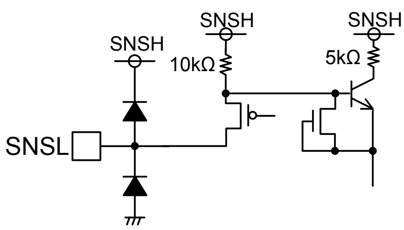
*(Note 4)*Using a PCB board based on JESD51-7.

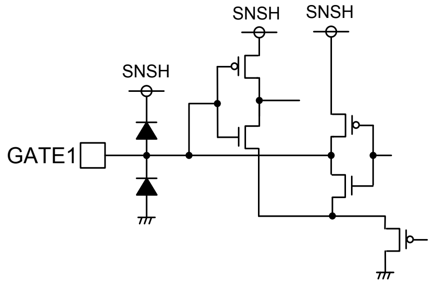
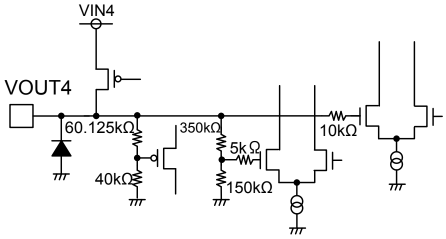
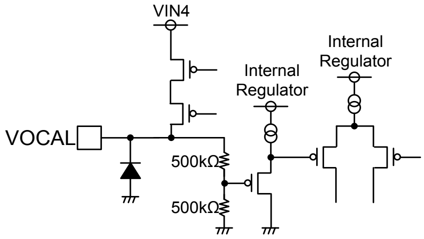
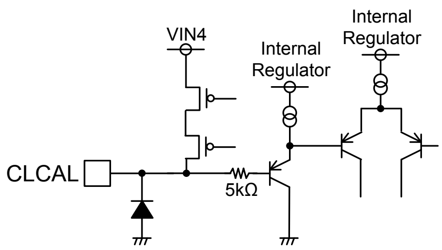
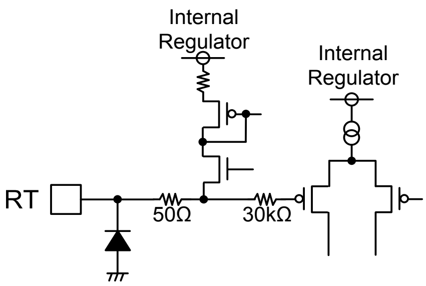
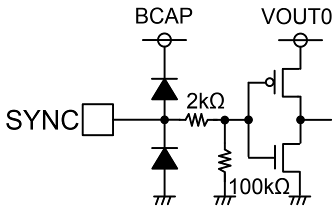
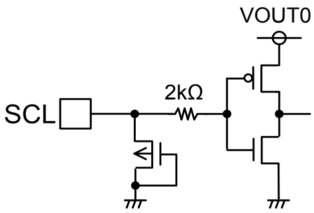
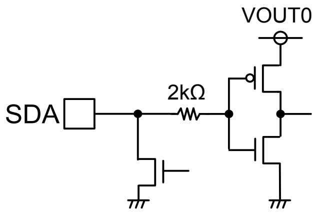
Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

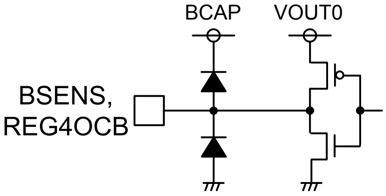
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Figure 66. Thermal Reduction Characteristics

I/O Equivalence Circuit(s)

Pin No.	Pin Name	Equivalent Circuit	Pin No.	Pin Name	Equivalent Circuit
9 7 35 22	VOUT1 VOUT2 VOUT3 VOUT5		17	HSW	
15	SW2		44 14	FB1 FB2	
43 13	INV1 INV2		12	VOUT0	
10 8 36 41 23	ADJ1 ADJ2 ADJ3 ADJ4 ADJ5		2	SNSL	

Pin No.	Pin Name	Equivalent Circuit	Pin No.	Pin Name	Equivalent Circuit
1	GATE1		42	VOUT4	
40	VOCAL		39	CLCAL	
33	RT		31	SYNC	
30	SCL		29	SDA	

Pin No.	Pin Name	Equivalent Circuit
27 28	BSENS REG4 OCB	

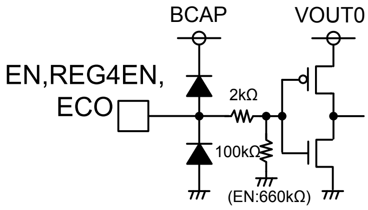
Pin No.	Pin Name	Equivalent Circuit
24 25 26	EN REG4 EN ECO	

Figure 67. I/O Equivalence Circuit(s)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

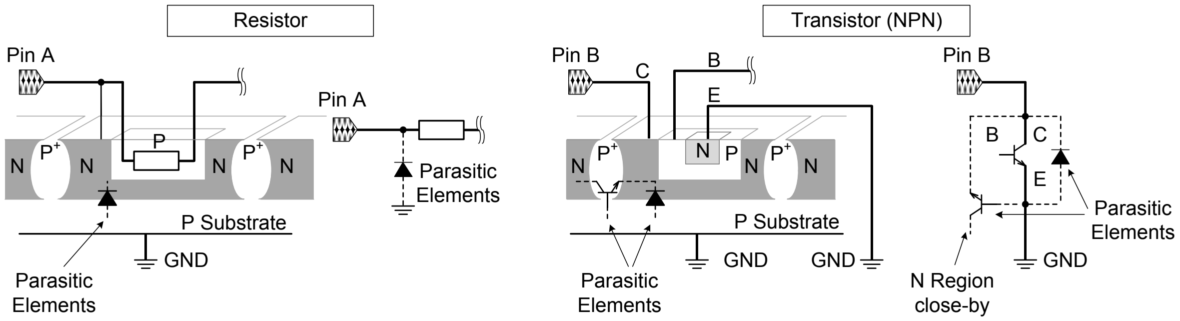


Figure 68. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins except DCDC2/STBREG and REG1. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. DCDC2 Short Current Protection (SCP)

While OCP operates, if the output voltage falls below 70%, SCP will start up. If SCP operates, the output will be OFF period of 1024 pulse. It extends the output OFF time to reduce the average output current. In addition, when power start-up this feature is masked until it reaches the output voltage is set to prevent the startup imperfection.

18. BCAP Over Voltage Protection (BCOVP)

The output except DCDC2/STBREG and REG1 will be turned OFF when BCAP voltage exceeds 30V(Typ).
When the voltage falls under 28V(Typ), those outputs restarts. Please care the range of use voltage.

19. BCAP Voltage Slew Rate Limitation

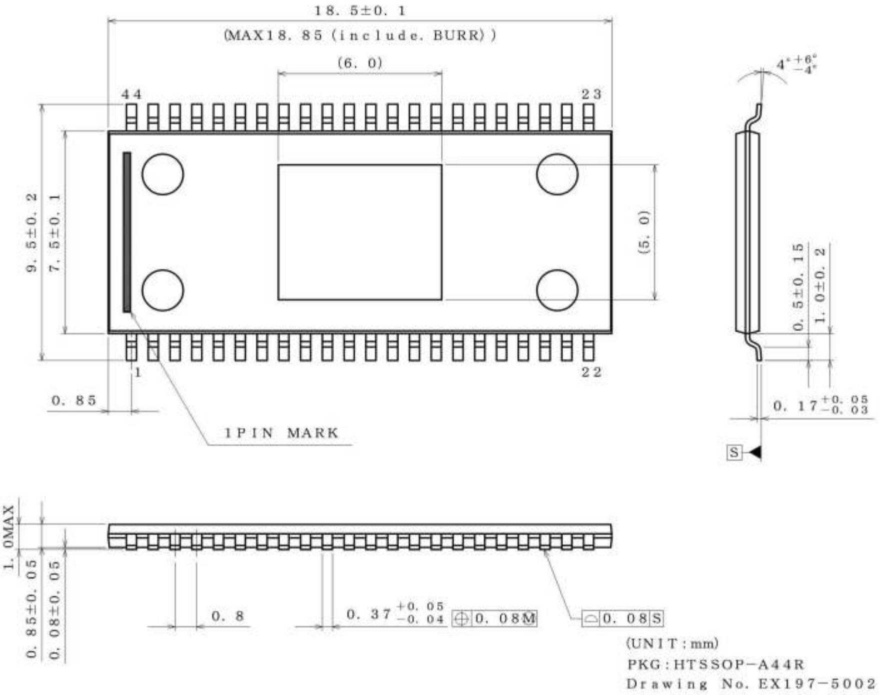
When the large voltage slew rate would input on the BCAP pin over 1 V/µs, the IC could be reset. Please care with a bypass capacitor or input LC filter etc. to reduce the slew rate.

Ordering Information

B D 4 9 1 0 1 A R F S - M E 2

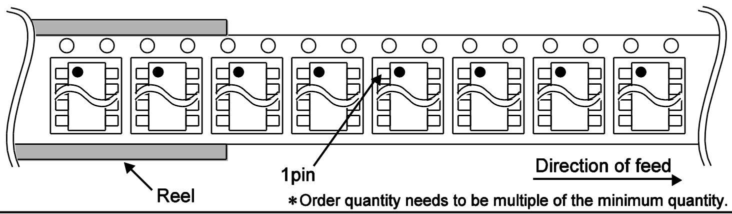
- Part Number
- Package
RFS: HTSSOP-A44R
- M: for Automotive
- Packaging and forming specification
E2: Embossed tape and reel

Physical Dimension, Tape and Reel Information



<Tape and Reel information>

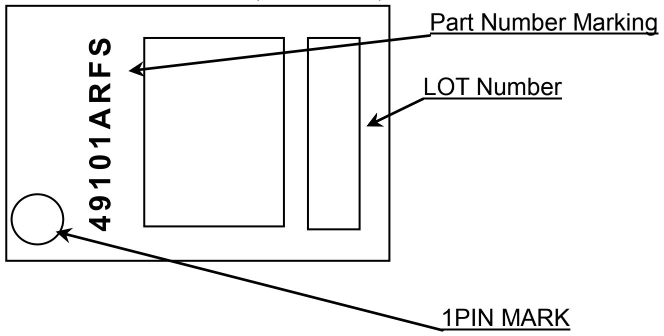
Tape	Embossed carrier tape (with dry pack)
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Marking Diagrams

HTSSOP-A44R (TOP VIEW)



Revision History

Date	Revision	Changes
20.Sep.2016	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

<table>
<tr><th>JAPAN</th><th>USA</th><th>EU</th><th>CHINA</th></tr>
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<tr><td>CLASSⅣ</td><td>CLASSⅢ</td></tr>
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2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.
2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).
3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

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3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.
4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

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