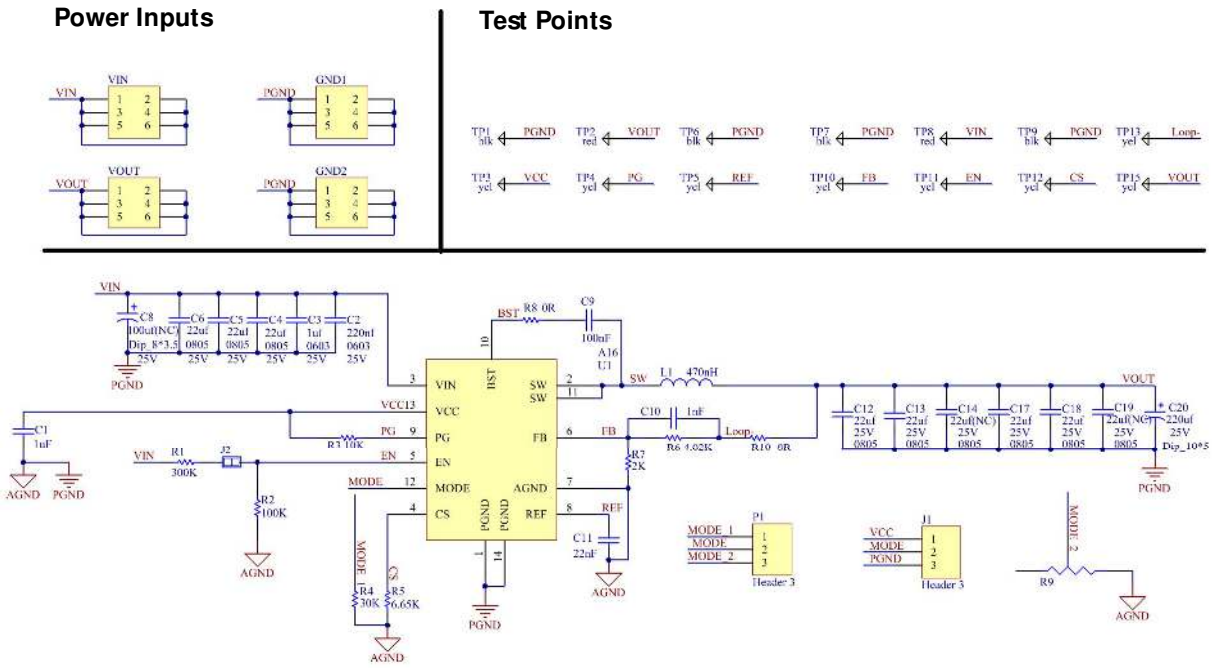
IS6605A Evaluation Board User Guide

EVM Schematic



Note:

1) **This schematic design is based on VIN=12V, VOUT=1.8V.**

2) **PGOOD is an indicator of system fault (including UV, OV, OC and OT). If it is not needed, remove R1 to float PGOOD.**

3) **EN is used to enable the IC. It is connected via a resistor divider from Vin (to generate 3.3V). If EN is supplied by external signal, remove J3 jumper and connect it directly to the external enable signal.**

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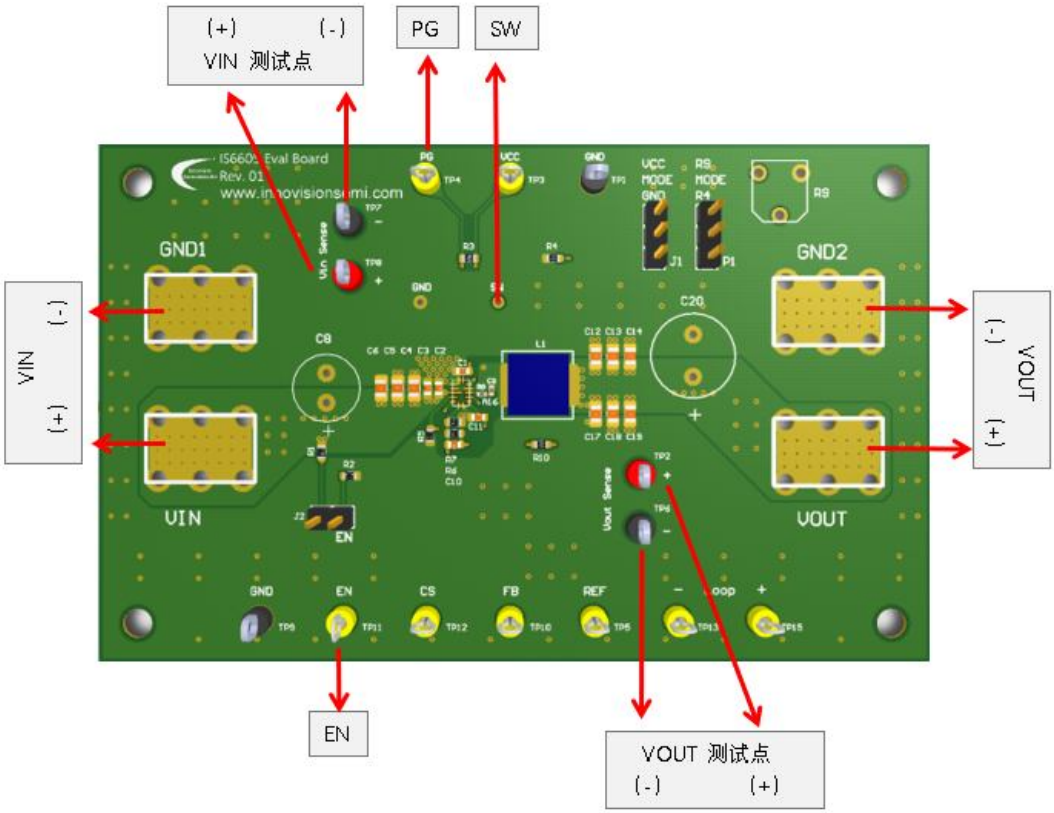
Designator	Value	Description	Footprint	Quantity
U1	16V/6A	IS6605A	2mmx3mm14-Pin QFN Package	1
GND1, GND2, VIN, VOUT	50A	power interface	Header 3X2	4
C1, C3	1uf	Cap 0603 X7R 1UF K 25V	0603_CAP	2
C2	220nf	Cap 0603 X7R220NF K 25V	0603_CAP	1
C4, C5, C6, C12, C13, C17, C18	22uf	Cap 0805 X2R 22UF M 25V	0805_CAP	7
C9	100nf	Cap 0402 X7R 100NF K 50V	0402_cap	1
C10	1nf	Cap 0603 X7R 1NF K 50V	0603_CAP	1
C11	22nf	Cap 0603 X7R 22NF K 50V	0603_CAP	1
C20	220uf	Cap Dip_10*13*5 25V	Dip_10*13*5	1
R1	300K	Res 0603 300K F	0603_RES	1
R2	100k	Res 0603 100K F	0603_RES	1
R3	10k	Res 0603 1K F	0603_RES	1
R4	30k	Res 0603 30K F	0603_RES	1
R5	6.65k	Res 0603 6.65K F	0603_RES	1
R6	4.02k	Res 0603 4.02K F	0603_RES	1
R7	2k	Res 0603 2K F	0603_RES	1
R8	0R	Res 0402 0R F	0402_RES	1
R10	0R	Res 0603 0R F	0603_RES	1
R9	500K	Tapped Resistor 500K	Tapped Resistor	1
L1	470nH	Hotland MDW0650-R47-N2	0650	1
J2	Header 2	Header, 2-Pin	PIN-2-2.54-1.0	2
P1, J1	Header 3	Header, 3-Pin	PIN-3-2.54-1.0	1
TP1, TP6, TP7, TP9	blk	Test Point	TEST_POINT_BLK	4

TP2, TP8	Red	Test Point	TEST_POINT_RED	2
TP3, TP4, TP5, TP10, TP11, TP12	Yel	Test Point	TEST_POINT_YEL	6

Configuration and Operation

The IS6605A Eval Board has designed all necessary connections and test points to test and evaluate its performance. Before operation, make sure that all external power supplies and loads are disabled or turned off.



Power On

It is assumed that all power supplies and active loads are preset to proper output and load conditions, and all connections are made.

1) Ensure that all power supply voltages are turned off.

2) VIN input 12V.

3) Connect the J2 jumper cap or apply 2V to 5V to the "EN". external point shown to make the circuit work normally.

4) Use electronic load (0-6A).

5) Power off in reverse order.

When measuring efficiency, it is recommended to use a precision shunt and a multimeter with more than 5 digits to measure current and voltage. If the above conditions are met, your efficiency results should be accurate.

Change Settings

Users can change four settings on IS6605A Eval Board:

Step 1. Output voltage

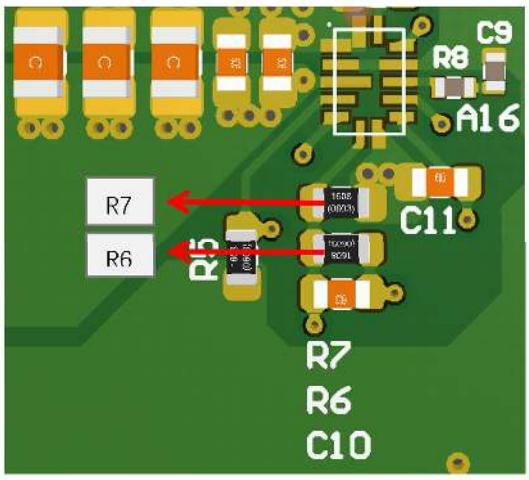
Step 2. Current limitation

Step 3. Soft start time

Step 4. Switching frequency

Step 1. To change the output voltage, use the following equation to calculate. R6 is the top resistor (from VOUT to FB) and R7 is the bottom resistor (from FB to GND). Reference to the table below for actual resistor value. Recommended resistance ranges from 1K to 10K..

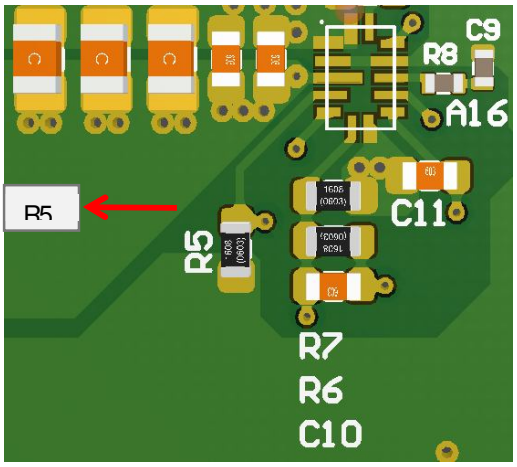
$$V_{OUT} = \frac{R_b + R_7}{R_7} \times 0.6V$$



VOUT/V	R6/K	R7/K
0.6	0	悬空
1.2	2	2
1.8	2	1
2.5	2	0.632
3.3	2	0.442
5	2	0.272

Step 2. To change current limit, use the following equation to determine the desired R5 value.

$$I_{LIM}(A) = \frac{V_{OCP}}{R_5 \times G_{CS}} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}} \times \frac{1}{2 \times L \times f_s}$$



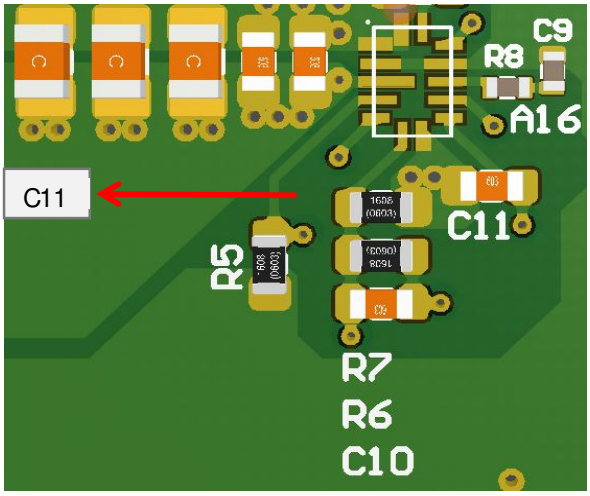
The inductor current information is reflected to the CS pin by Gcs.

V_{OCP}= 1.2V

G_{CS}= 40μA/ A

Step 3. In order to change Soft Start time, use the following equation to calculate.

$$T_{SS}(ms) = \frac{C_{11}(nF) \times 0.6(V)}{12(\mu A)}$$

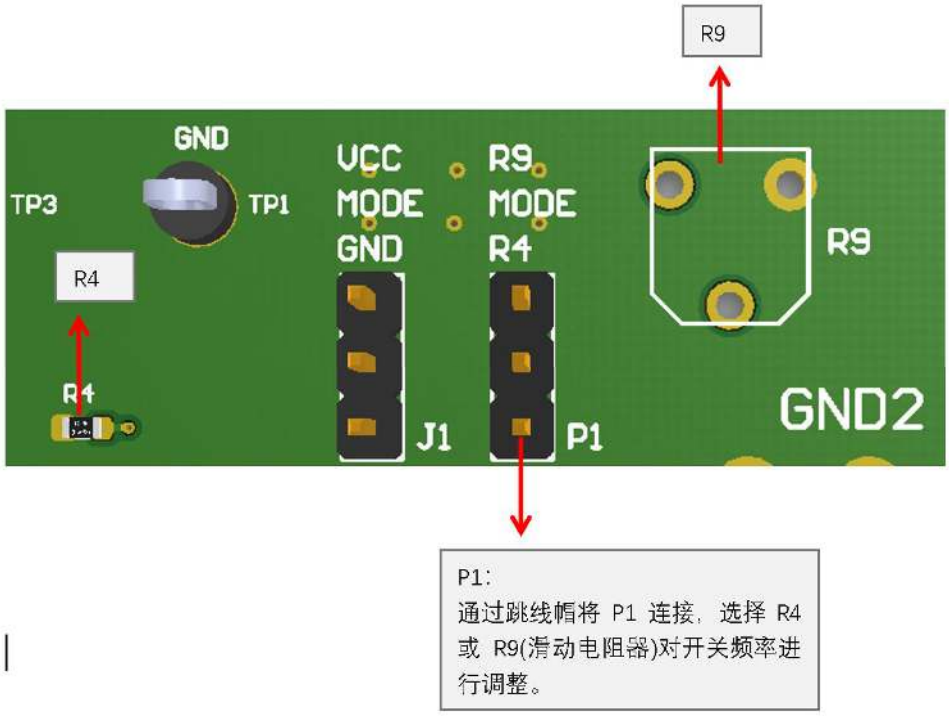


SS time is set at default of 1.4 msec. Adding a small MLCC capacitor between REF and RTN can extend the soft start time.

Step 4. In order to change the switching frequency of the EVM, use R4/R9. In the meantime, the IC must be turned off or power removed first.

MODE Selection

MDOE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600KHz
243kΩ(±20%) to GND	Pulse skip	800KHz
121kΩ(±20%) to GND	Pulse skip	1000KHz
GND	Forced CCM	600KHz
30.1kΩ(±20%) to GND	Forced CCM	800KHz
60.4kΩ(±20%) to GND	Forced CCM	1000KHz



P1:
通过跳线帽将 P1 连接，选择 R4 或 R9(滑动电阻器)对开关频率进行调整。

PCB Layout Guidelines:

An effective PCB layout is critical to the stable operation of the circuit. For best performance, please refer to the diagram in the PCB layout column and follow the PCB layout recommendations below.

1) The input ceramic capacitor should be as close as possible to the VIN and PGND pins, and the main ceramic capacitor should be placed on the same wiring layer as IS6605A. VIN and PGND of copper plane should be a maximum of make parasitic resistance is minimized .

2) Vin (pin 10) must be connected to a capacitance value close to the minimum 0.1μF capacitor. At least two 20/10 mil vias connected to the ground terminal of the capacitor is connected to the PCB ground.

3) Place as many PGND holes as possible closest to the PGND pin to minimize parasitic impedance and thermal resistance.

4) The VCC capacitor should be as close as possible to IS6605A. Connect AGND and PGND at the ground point of the VCC capacitor.

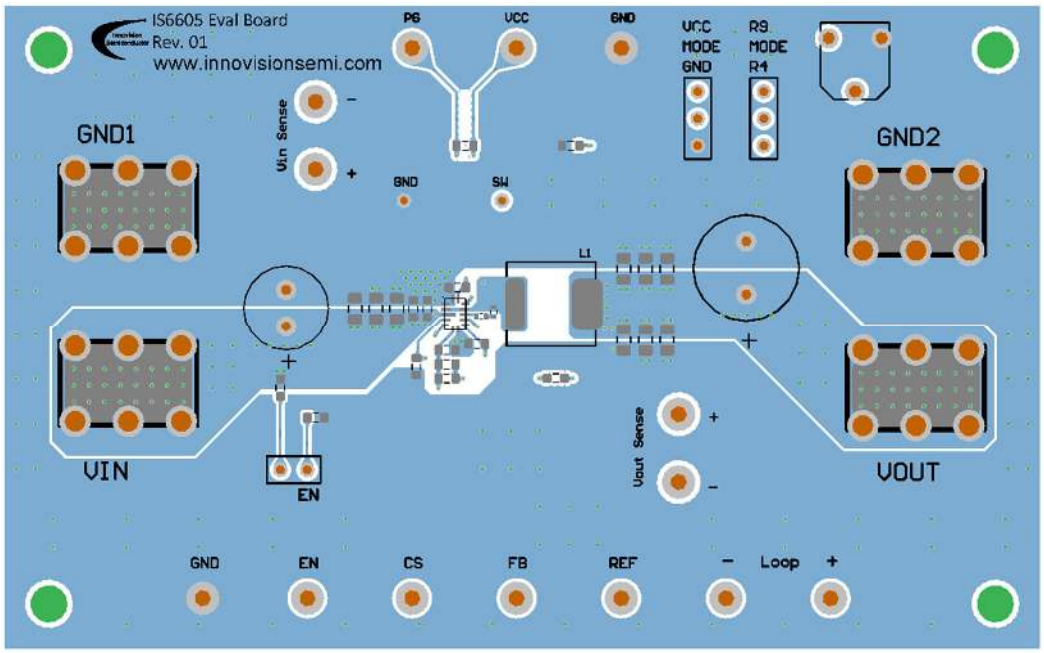
5) Place the BST capacitor as close as possible to BST and SW. The wiring width should be greater than 20mm. We recommend the use of 0.1 μF - 1 μF of the capacitor. The resistor is placed between the IC and BST capacitor. It is recommended to use a 3.3 Ω resistor.

6) Place the REF capacitor close to REF and connect to RTN. 22 nF is recommended to use a capacitor.

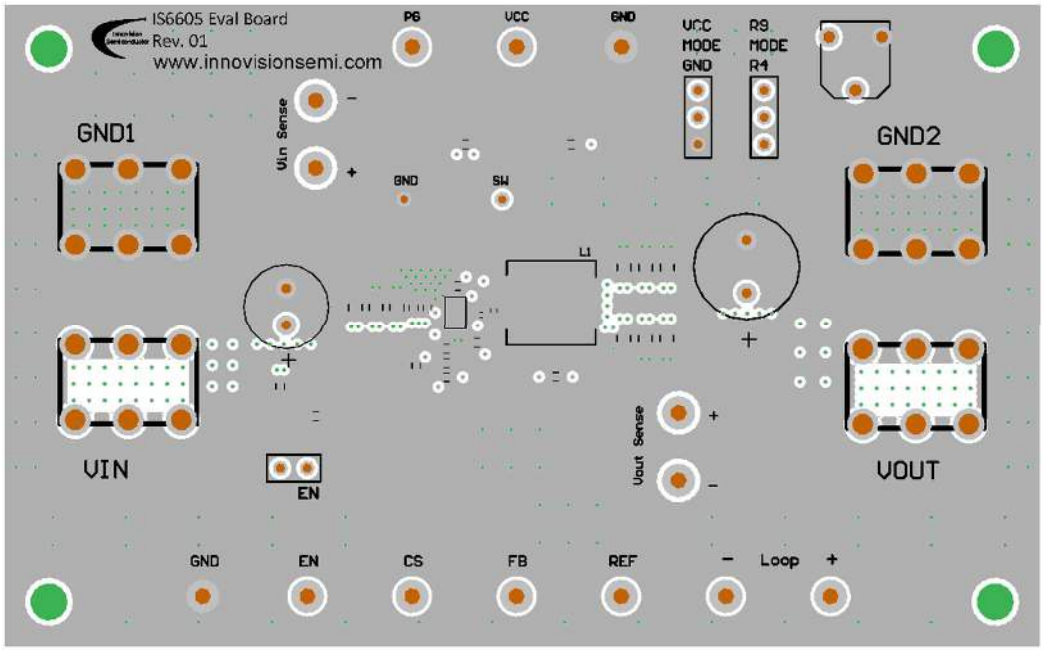
7) If the via must be placed on the PGOOD pin , place it at least 10 mm away from the positive side of the 1st input decoupling capacitor near IS6605A .

PCB Layout Example

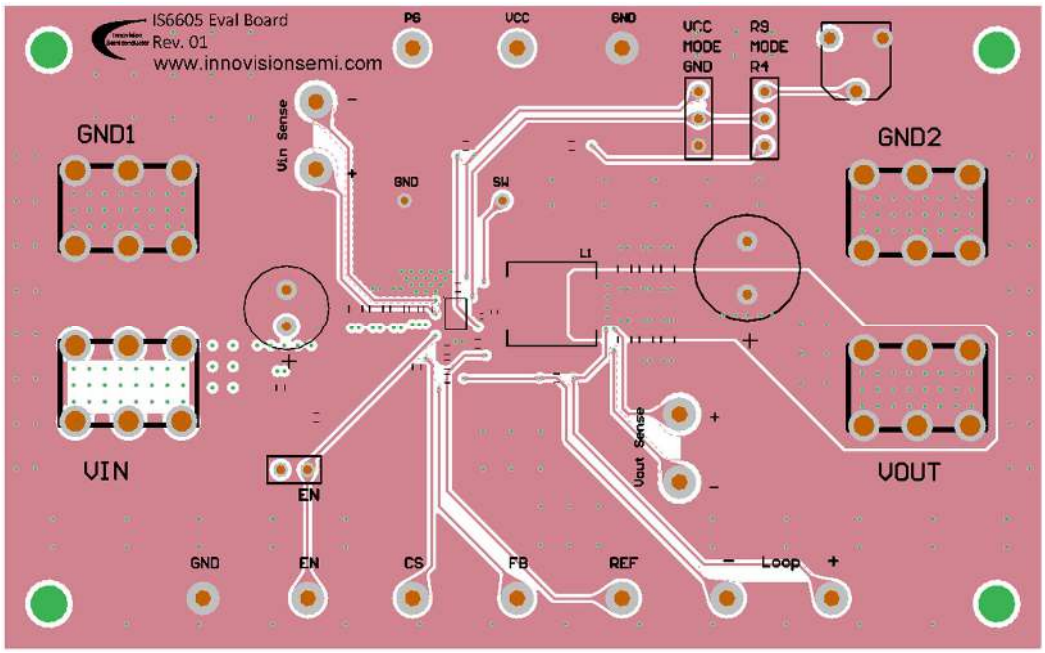
1) TOP Layer



2) Layer 2



3) Layer 3



4) Bottom Layer