FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

SEMICONDUCTOR™

NC7SP74
TinyLogic® ULP D-Type Flip-Flop with Preset and Clear

General Description

The NC7SP74 is a single D-type CMOS Flip-Flop with pre-set and clear from Fairchild's Ultra Low Power (ULP) Series of TinyLogic®. Ideal for applications where battery life is critical, this product is designed for ultra low power consumption within the V_{CC} operating range of 0.9V to 3.6V.

The internal circuit is composed of a minimum of inverter stages including the output buffer, to enable ultra low static and dynamic power.

The NC7SP74, for lower drive requirements, is uniquely designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve best in class speed operation while maintaining extremely low CMOS power dissipation.

The signal level applied to the D input is transferred to the Q output during the positive going transition of the CLK pulse.

Features

■ Space saving US8 surface mount package
■ MicroPak™ Pb-Free leadless package
■ 0.9V to 3.6V V_{CC} supply operation
■ 3.6V overvoltage tolerant I/Os at V_{CC} from 0.9V to 3.6V
■ t_{PD}

   3.0 ns typ for 3.0V to 3.6V V_{CC}
   4.0 ns typ for 2.3V to 2.7V V_{CC}
   5.0 ns typ for 1.65V to 1.95V V_{CC}
   6.0 ns typ for 1.40V to 1.60V V_{CC}
   9.0 ns typ for 1.10V to 1.30V V_{CC}
   24.0 ns typ for 0.90V V_{CC}

■ Power-Off high impedance inputs and outputs
■ Static Drive (I_{OH}/I_{OL})

   ±2.6 mA   @ 3.00V V_{CC}
   ±2.1 mA   @ 2.30V V_{CC}
   ±1.5 mA   @ 1.65V V_{CC}
   ±1.0 mA   @ 1.40V V_{CC}
   ±0.5 mA   @ 1.10V V_{CC}
   ±20 μA   @ 0.9V V_{CC}

■ Uses patented Quiet Series™ noise/EMI reduction circuitry
■ Ultra low dynamic power

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SP74K8X	MAB08A	P74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7SP74L8X	MAC08A	X9	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Battery Life vs. V_{CC} Supply Voltage
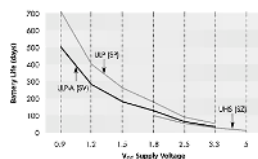
TinyLogic ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.

Battery Life = $(V_{battery} * I_{battery} * .9)/(P_{device})/24hrs/day$

Where, $P_{device} = (I_{CC} * V_{CC}) + (C_{PD} + C_L) * V_{CC}^2 * f$

Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L = 15 pF load

TinyLogic® is a registered trademark of Fairchild Semiconductor Corporation.

MicroPak™ and Quiet Series™ are trademarks of Fairchild Semiconductor Corporation.

Pin Descriptions

Pin Names	Description
D	Data Input
CK	Clock Pulse Input
$\overline{CLR}$	Direct Clear Input
Q, $\overline{Q}$	Flip-Flop Output
$\overline{PR}$	Direct Preset Input

Logic Symbol

IEEE/IEC
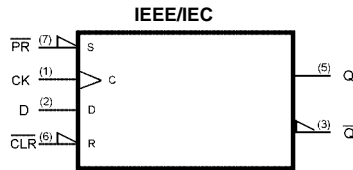
Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	No Change

H = HIGH Logic Level
L = LOW Logic Level
Q_n = No change in data
X = Immaterial
Z = High Impedance
↑ = Rising Edge
↓ = Falling edge

Connection Diagrams

Pin Assignments for US8

(Top View)
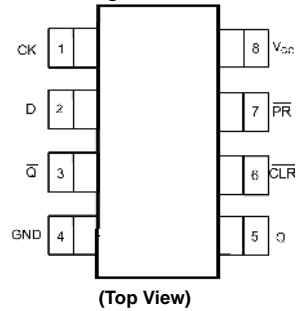
Pin One Orientation Diagram
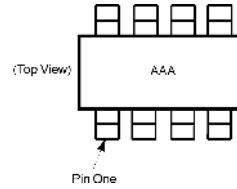
AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak
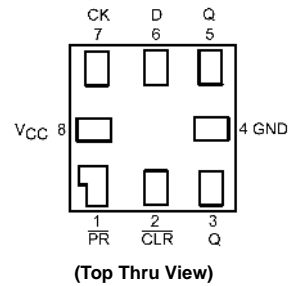
(Top Thru View)

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_{IN})	−0.5V to +4.6V
DC Output Voltage (V_{OUT})	−0.5V to +7.0V
HIGH or LOW State (Note 2)	−0.5V to V_{CC} +0.5V
V_{CC} = 0V	−0.5V to 4.6V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	±50 mA
DC Output Diode Current (I_{OK})	
V_{OUT} < 0V	−50 mA
V_{OUT} > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or Ground)	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	0.9V to 3.6V
Input Voltage (V_{IN})	0V to 3.6V
Output Voltage (V_{OUT})	
HIGH or LOW State	0V to V_{CC}
V_{CC} = 0V	0V to 3.6V
Output Current in (I_{OH}/I_{OL})	
V_{CC} = 3.0V to 3.6V	±2.6 mA
V_{CC} = 2.3V to 2.7V	±2.1 mA
V_{CC} = 1.65V to 1.95V	±1.5 mA
V_{CC} = 1.40V to 1.60V	±1.0 mA
V_{CC} = 1.10V to 1.30V	±0.5 mA
V_{CC} = 0.9V	±20 μA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

**Note 1:** Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Min	T_A = +25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions
V_{IH}	HIGH Level Input Voltage	0.90	0.65 x V_{CC}		0.65 x V_{CC}		V	
		1.10 ≤ V_{CC} ≤ 1.30	0.65 x V_{CC}		0.65 x V_{CC}			
		1.40 ≤ V_{CC} ≤ 1.60	0.65 x V_{CC}		0.65 x V_{CC}			
		1.65 ≤ V_{CC} ≤ 1.95	0.65 x V_{CC}		0.65 x V_{CC}			
		2.30 ≤ V_{CC} ≤ 2.70	1.6		1.6			
		3.00 ≤ V_{CC} ≤ 3.60	2.1		2.1			
V_{IL}	LOW Level Input Voltage	0.90		0.35 x V_{CC}		0.35 x V_{CC}	V	
		1.10 ≤ V_{CC} ≤ 1.30		0.35 x V_{CC}		0.35 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60		0.35 x V_{CC}		0.35 x V_{CC}		
		1.65 ≤ V_{CC} ≤ 1.95		0.35 x V_{CC}		0.35 x V_{CC}		
		2.30 ≤ V_{CC} ≤ 2.70		0.7		0.7		
		3.00 ≤ V_{CC} ≤ 3.60		0.9		0.9		
V_{OH}	HIGH Level Output Voltage	0.90	V_{CC} - 0.1		V_{CC} - 0.1		V	I_{OH} = −20 μA
		1.10 ≤ V_{CC} ≤ 1.30	V_{CC} - 0.1		V_{CC} - 0.1			
		1.40 ≤ V_{CC} ≤ 1.60	V_{CC} - 0.1		V_{CC} - 0.1			
		1.65 ≤ V_{CC} ≤ 1.95	V_{CC} - 0.1		V_{CC} - 0.1			
		2.30 ≤ V_{CC} ≤ 2.70	V_{CC} - 0.1		V_{CC} - 0.1			
		3.00 ≤ V_{CC} ≤ 3.60	V_{CC} - 0.1		V_{CC} - 0.1			
		1.10 ≤ V_{CC} ≤ 1.30	0.75 x V_{CC}		0.70 x V_{CC}			I_{OH} = −0.5 mA
		1.40 ≤ V_{CC} ≤ 1.60	1.07		0.99			I_{OH} = −1.0 mA
		1.65 ≤ V_{CC} ≤ 1.95	1.24		1.22			I_{OH} = −1.5 mA
		2.30 ≤ V_{CC} ≤ 2.70	1.95		1.87			I_{OH} = −2.1 mA
		3.00 ≤ V_{CC} ≤ 3.60	2.61		2.55			I_{OH} = −2.6 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter	V$_{CC}$ (V)	T$_A$ = +25°C Min	T$_A$ = +25°C Max	T$_A$ = −40°C to +85°C Min	T$_A$ = −40°C to +85°C Max	Units	Conditions
V$_{OL}$	LOW Level	0.90		0.1		0.1		
	Output Voltage	1.10 ≤ V$_{CC}$ ≤ 1.30		0.1		0.1		
		1.40 ≤ V$_{CC}$ ≤ 1.60		0.1		0.1		I$_{OL}$ = 20 μA
		1.65 ≤ V$_{CC}$ ≤ 1.95		0.1		0.1		
		2.30 ≤ V$_{CC}$ ≤ 2.70		0.1		0.1		
		3.00 ≤ V$_{CC}$ ≤ 3.60		0.1		0.1	V	
		1.10 ≤ V$_{CC}$ ≤ 1.30		0.30 x V$_{CC}$		0.30 x V$_{CC}$		I$_{OL}$ = 0.5 mA
		1.40 ≤ V$_{CC}$ ≤ 1.60		0.31		0.37		I$_{OL}$ = 1.0 mA
		1.65 ≤ V$_{CC}$ ≤ 1.95		0.31		0.35		I$_{OL}$ = 1.5 mA
		2.30 ≤ V$_{CC}$ ≤ 2.70		0.31		0.33		I$_{OL}$ = 2.1 mA
		3.00 ≤ V$_{CC}$ ≤ 3.60		0.31		0.33		I$_{OL}$ = 2.6 mA
I$_{IN}$	Input Leakage Current	0.90 to 3.60		±0.1		±0.5	μA	0 ≤ V$_I$ ≤ 3.6V
I$_{OFF}$	Power Off Leakage Current	0		0.5		0.5	μA	0 ≤ (V$_I$, V$_O$) ≤ 3.6V
I$_{CC}$	Quiescent Supply Current	0.90 to 3.60		0.9		0.9	μA	V$_I$ = V$_{CC}$ or GND

AC Electrical Characteristics (10pF, 1MΩ)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	$T_A = +25°C$ Typ	$T_A = +25°C$ Max	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units	Conditions	Figure Number
f_{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	$C_L = 10$ pF $R_D = 1$ MΩ	Figures 1, 5
		1.10 ≤ V_{CC} ≤ 1.30	50			50				
		1.40 ≤ V_{CC} ≤ 1.60	75			75				
		1.65 ≤ V_{CC} ≤ 1.95	100			100				
		2.30 ≤ V_{CC} ≤ 2.70	125			125				
		3.00 ≤ V_{CC} ≤ 3.60	150			150				
t_{PLH} t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	0.90		24.0				ns	$C_L = 10$ pF $R_D = 1$ MΩ	Figures 1, 3
		1.10 ≤ V_{CC} ≤ 1.30	4.0	15.0	22.0	3.5	31.0			
		1.40 ≤ V_{CC} ≤ 1.60	2.0	9.0	13.0	1.5	14.0			
		1.65 ≤ V_{CC} ≤ 1.95	1.5	7.0	11.0	1.0	13.0			
		2.30 ≤ V_{CC} ≤ 2.70	1.0	5.0	8.0	0.8	9.0			
		3.00 ≤ V_{CC} ≤ 3.60	1.0	4.0	7.0	0.5	8.0			
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$	0.90		6.5				ns	$C_L = 10$ pF $R_D = 1$ MΩ	Figures 1, 3
		1.10 ≤ V_{CC} ≤ 1.30	4.0	12.0	23.0	4.0	34.0			
		1.40 ≤ V_{CC} ≤ 1.60	2.0	9.0	12.0	2.0	14.0			
		1.65 ≤ V_{CC} ≤ 1.95	1.5	7.0	11.0	1.5	13.0			
		2.30 ≤ V_{CC} ≤ 2.70	1.0	5.0	9.0	1.0	9.0			
		3.00 ≤ V_{CC} ≤ 3.60	1.0	4.0	7.0	1.0	8.0			
t_S	Setup Time, CK to D	0.90		10.0				ns	$C_L = 10$ pF $R_D = 1$ MΩ	Figures 1, 4
		1.10 ≤ V_{CC} ≤ 1.30	7.0			7.0				
		1.40 ≤ V_{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V_{CC} ≤ 1.95	2.0			2.0				
		2.30 ≤ V_{CC} ≤ 2.70	1.5			1.5				
		3.00 ≤ V_{CC} ≤ 3.60	1.0			1.0				
t_H	Hold Time, CK to D	0.90		1.0				ns	$C_L = 10$ pF $R_D = 1$ MΩ	Figures 1, 4
		1.10 ≤ V_{CC} ≤ 1.30	0.5			0.5				
		1.40 ≤ V_{CC} ≤ 1.60	0.5			0.5				
		1.65 ≤ V_{CC} ≤ 1.95	0.5			0.5				
		2.30 ≤ V_{CC} ≤ 2.70	0.5			0.5				
		3.00 ≤ V_{CC} ≤ 3.60	0.5			0.5				
t_W	Pulse Width, CK, $\overline{PR}$, $\overline{CLR}$	0.90		5.0				ns	$C_L = 10$ pF $R_D = 1$ MΩ	Figures 1, 5
		1.10 ≤ V_{CC} ≤ 1.30	5.0			5.0				
		1.40 ≤ V_{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V_{CC} ≤ 1.95	2.5			2.5				
		2.30 ≤ V_{CC} ≤ 2.70	2.5			2.5				
		3.00 ≤ V_{CC} ≤ 3.60	2.0			2.0				
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	0.90		12.0				ns	$C_L = 10$ pF $R_D = 1$ MΩ	Figures 1, 4
		1.10 ≤ V_{CC} ≤ 1.30	8.5			8.5				
		1.40 ≤ V_{CC} ≤ 1.60	3.5			3.5				
		1.65 ≤ V_{CC} ≤ 1.95	3.0			3.0				
		2.30 ≤ V_{CC} ≤ 2.70	2.5			2.5				
		3.00 ≤ V_{CC} ≤ 3.60	2.0			2.0				

AC Electrical Characteristics (15pF, 1MΩ)

Symbol	Parameter	V_CC (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	C_L = 15 pF R_D = 1 MΩ	Figures 1, 5
		1.10 ≤ V_CC ≤ 1.30	50			150				
		1.40 ≤ V_CC ≤ 1.60	75			200				
		1.65 ≤ V_CC ≤ 1.95	100			250				
		2.30 ≤ V_CC ≤ 2.70	125			175				
		3.00 ≤ V_CC ≤ 3.60	150			200				
t_{PLH} t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	0.90		27.0				ns	C_L = 15 pF R_D = 1 MΩ	Figures 1, 3
		1.10 ≤ V_CC ≤ 1.30	5.0	16.0	23.0	4.5	34.0			
		1.40 ≤ V_CC ≤ 1.60	3.0	10.0	14.0	2.5	16.0			
		1.65 ≤ V_CC ≤ 1.95	2.0	7.0	11.0	2.0	13.0			
		2.30 ≤ V_CC ≤ 2.70	1.5	5.0	8.0	1.0	9.0			
		3.00 ≤ V_CC ≤ 3.60	1.0	4.0	7.0	0.5	8.0			
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$	0.90		27.0				ns	C_L = 15 pF R_D = 1 MΩ	Figures 1, 3
		1.10 ≤ V_CC ≤ 1.30	5.0	15.0	24.0	5.0	37.0			
		1.40 ≤ V_CC ≤ 1.60	3.0	10.0	13.0	3.0	16.0			
		1.65 ≤ V_CC ≤ 1.95	2.0	7.0	11.0	2.0	13.0			
		2.30 ≤ V_CC ≤ 2.70	1.5	5.0	9.0	1.5	9.0			
		3.00 ≤ V_CC ≤ 3.60	1.0	4.0	7.0	1.0	8.0			
t_S	Setup Time, CK to D	0.90		10.0				ns	C_L = 15 pF R_D = 1 MΩ	Figures 1, 4
		1.10 ≤ V_CC ≤ 1.30	7.0			7.0				
		1.40 ≤ V_CC ≤ 1.60	3.0			3.0				
		1.65 ≤ V_CC ≤ 1.95	2.0			2.0				
		2.30 ≤ V_CC ≤ 2.70	1.5			1.5				
		3.00 ≤ V_CC ≤ 3.60	1.0			1.0				
t_H	Hold Time, CK to D	0.90		1.0				ns	C_L = 15 pF R_D = 1 MΩ	Figures 1, 4
		1.10 ≤ V_CC ≤ 1.30	0.5			0.5				
		1.40 ≤ V_CC ≤ 1.60	0.5			0.5				
		1.65 ≤ V_CC ≤ 1.95	0.5			0.5				
		2.30 ≤ V_CC ≤ 2.70	0.5			0.5				
		3.00 ≤ V_CC ≤ 3.60	0.5			0.5				
t_W	Pulse Width, CK, $\overline{PR}$, $\overline{CLR}$	0.90		5.0				ns	C_L = 15 pF R_D = 1 MΩ	Figures 1, 5
		1.10 ≤ V_CC ≤ 1.30	5.0			5.0				
		1.40 ≤ V_CC ≤ 1.60	3.0			3.0				
		1.65 ≤ V_CC ≤ 1.95	2.5			2.5				
		2.30 ≤ V_CC ≤ 2.70	2.5			2.5				
		3.00 ≤ V_CC ≤ 3.60	2.0			2.0				
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	0.90		12.0				ns	C_L = 15 pF R_D = 1 MΩ	Figures 1, 4
		1.10 ≤ V_CC ≤ 1.30	8.5			8.5				
		1.40 ≤ V_CC ≤ 1.60	3.5			3.5				
		1.65 ≤ V_CC ≤ 1.95	3.0			3.0				
		2.30 ≤ V_CC ≤ 2.70	2.5			2.5				
		3.00 ≤ V_CC ≤ 3.60	2.0			2.0				

AC Electrical Characteristics (30pF, 1MΩ)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	$T_A = +25°C$ Typ	$T_A = +25°C$ Max	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units	Conditions	Figure Number
f_{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	$C_L = 30$ pF $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \leq V_{CC} \leq 1.30$	50			150				
		$1.40 \leq V_{CC} \leq 1.60$	75			200				
		$1.65 \leq V_{CC} \leq 1.95$	100			250				
		$2.30 \leq V_{CC} \leq 2.70$	125			175				
		$3.00 \leq V_{CC} \leq 3.60$	150			200				
t_{PLH} t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	0.90		34.0				ns	$C_L = 30$ pF $R_D = 1$ MΩ	Figures 1, 3
		$1.10 \leq V_{CC} \leq 1.30$	6.0	18.0	27.0	5.0	43.0			
		$1.40 \leq V_{CC} \leq 1.60$	4.0	11.0	17.0	3.0	18.0			
		$1.65 \leq V_{CC} \leq 1.95$	2.0	8.0	13.0	2.0	15.0			
		$2.30 \leq V_{CC} \leq 2.70$	1.0	6.0	10.0	1.0	11.0			
		$3.00 \leq V_{CC} \leq 3.60$	0.8	5.0	8.0	0.5	10.0			
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$	0.90		34.0				ns	$C_L = 30$ pF $R_D = 1$ MΩ	Figures 1, 3
		$1.10 \leq V_{CC} \leq 1.30$	6.0	17.0	28.0	5.5	46.0			
		$1.40 \leq V_{CC} \leq 1.60$	4.0	11.0	16.0	3.5	18.0			
		$1.65 \leq V_{CC} \leq 1.95$	2.0	8.0	13.0	2.5	15.0			
		$2.30 \leq V_{CC} \leq 2.70$	1.0	6.0	9.0	1.5	11.0			
		$3.00 \leq V_{CC} \leq 3.60$	0.8	5.0	8.0	1.0	10.0			
t_S	Setup Time, CK to D	0.90		10.0				ns	$C_L = 30$ pF $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \leq V_{CC} \leq 1.30$	7.0			7.0				
		$1.40 \leq V_{CC} \leq 1.60$	3.0			3.0				
		$1.65 \leq V_{CC} \leq 1.95$	2.0			2.0				
		$2.30 \leq V_{CC} \leq 2.70$	1.5			1.5				
		$3.00 \leq V_{CC} \leq 3.60$	1.0			1.0				
t_H	Hold Time, CK to D	0.90		1.0				ns	$C_L = 30$ pF $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \leq V_{CC} \leq 1.30$	0.5			0.5				
		$1.40 \leq V_{CC} \leq 1.60$	0.5			0.5				
		$1.65 \leq V_{CC} \leq 1.95$	0.5			0.5				
		$2.30 \leq V_{CC} \leq 2.70$	0.5			0.5				
		$3.00 \leq V_{CC} \leq 3.60$	0.5			0.5				
t_W	Pulse Width, CK, $\overline{PR}$, $\overline{CLR}$	0.90		5.0				ns	$C_L = 30$ pF $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \leq V_{CC} \leq 1.30$	5.0			4.0				
		$1.40 \leq V_{CC} \leq 1.60$	3.0			3.0				
		$1.65 \leq V_{CC} \leq 1.95$	2.5			2.0				
		$2.30 \leq V_{CC} \leq 2.70$	2.5			3.0				
		$3.00 \leq V_{CC} \leq 3.60$	2.0			2.0				
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	0.90		12.0				ns	$C_L = 30$ pF $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \leq V_{CC} \leq 1.30$	8.5			8.5				
		$1.40 \leq V_{CC} \leq 1.60$	3.5			3.5				
		$1.65 \leq V_{CC} \leq 1.95$	3.0			3.0				
		$2.30 \leq V_{CC} \leq 2.70$	2.5			2.5				
		$3.00 \leq V_{CC} \leq 3.60$	2.0			2.0				

Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
C_{IN}	Input Capacitance	2.0		pF	$V_{CC} = 0$V	
C_{OUT}	Output Capacitance	4.0		pF	$V_{CC} = 0$V	
C_{PD}	Power Dissipation Capacitance	8.0		pF	$V_I = 0$V or V_{CC} $f = 10$ MHz	Figure 2

AC Loading and Waveforms
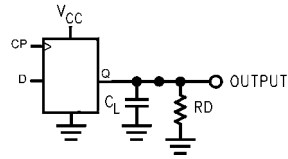
C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit
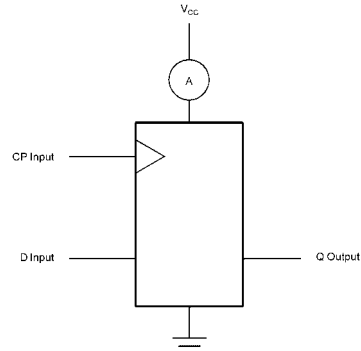
CP Input = AC Waveform; $t_r = t_f$ = 2.5 ns;
CP Input PRR = 10 MHz; Duty Cycle = 50%
D Input PRR = 5MHz; Duty Cycle = 50%
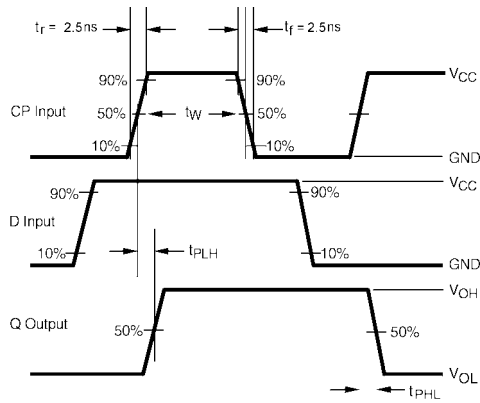
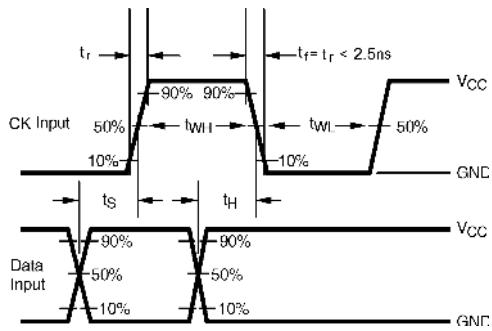**FIGURE 2. I_{CCD} Test Circuit**

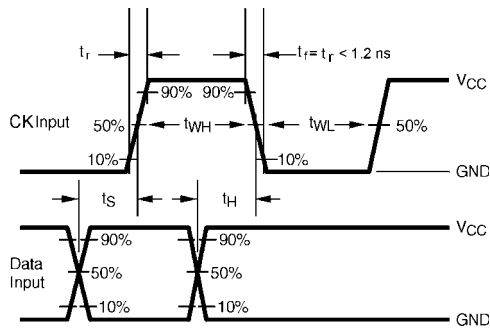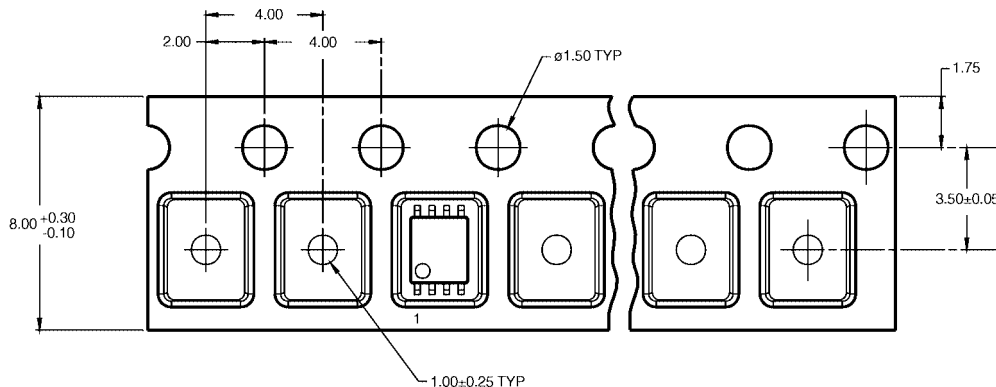**FIGURE 3. AC Waveforms**

FIGURE 4. AC Waveforms

FIGURE 5. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)
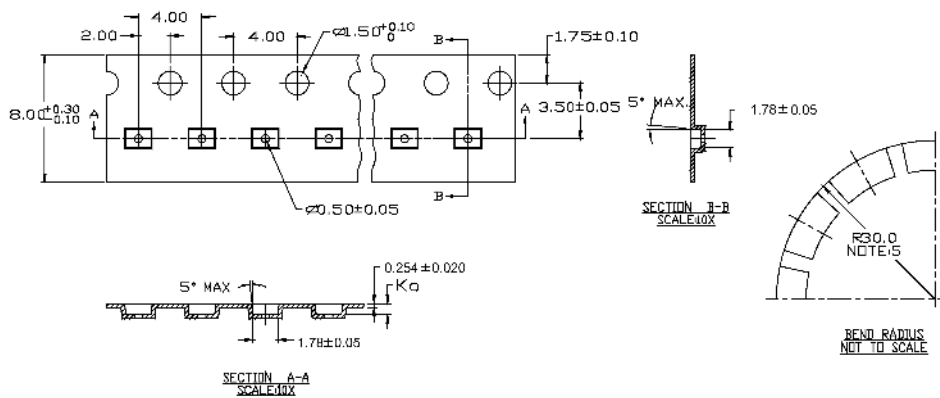
Tape and Reel Specification (Continued)
REEL DIMENSIONS inches (millimeters)

TAPE SLOT

DETAIL X

B

C

D

DETAIL X
SCALE: 3X

W₁

N

W₃

W₂
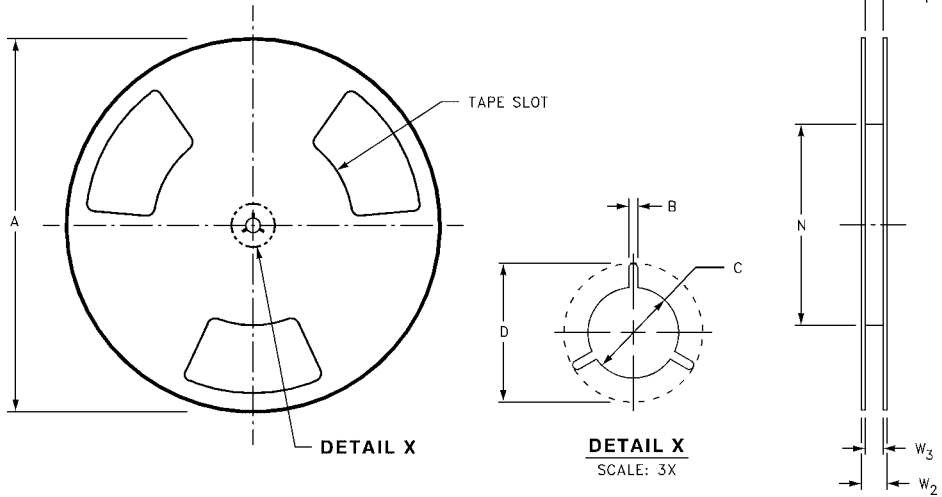
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/−0.000 (8.40 + 1.50/−0.00)	0.567 (14.40)	W1 + 0.078/−0.039 (W1 + 2.00/−1.00)

Physical Dimensions inches (millimeters) unless otherwise noted

-A-

2.0±.01

0.15

8   5

-B-

3.1±.1

2.3±0.1

1.55

1

4

⌒ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1.80

0.70

2.70

3.40

1.00

0.30 TYP

0.5 TYP
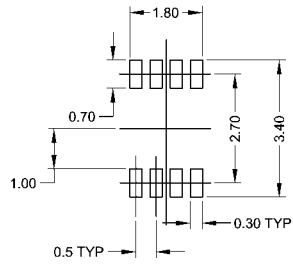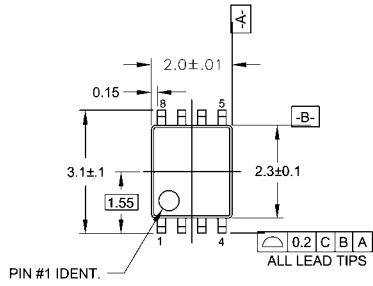
LAND PATTERN RECOMMENDATION

ALL LEAD TIPS

0.90 MAX

⌒ 0.1 C

0.70±0.10

-C-

0.10
0.00

0.17-0.27

0.50TYP

⊕ 0.13Ⓜ A BⓈ CⓈ

DETAIL A

0.10-0.18

0.4 TYP

GAGE PLANE

0.12

0°-8°

0.20-0.35

SEATING PLANE
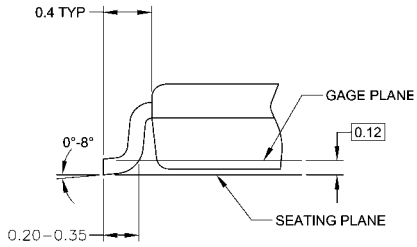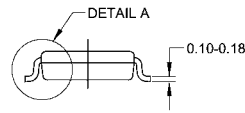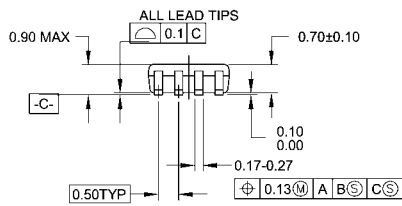
DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
   AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

2X ⌒ 0.10 C

B ◄ 1.6 ► A

1.6

INDEX AREA

2X ⌒ 0.10 C

TOP VIEW

(0.8)
(0.625)
(0.375)
(0.125)

(0.805)
(0.41)
(0.125)

(0.4)8X

(0.25)8X

Recommended Landpattern

0.55 MAX

// 0.05 C

0.05
0.00

C ⌒ 0.05 C

1.0

8X(0.09)

0.5

4 (0.1)

8X 0.35
0.25

0.15
0.25

8X

⊕ | 0.10 Ⓜ | C | A | B
0.05 Ⓜ | C

3X(0.2)

BOTTOM VIEW
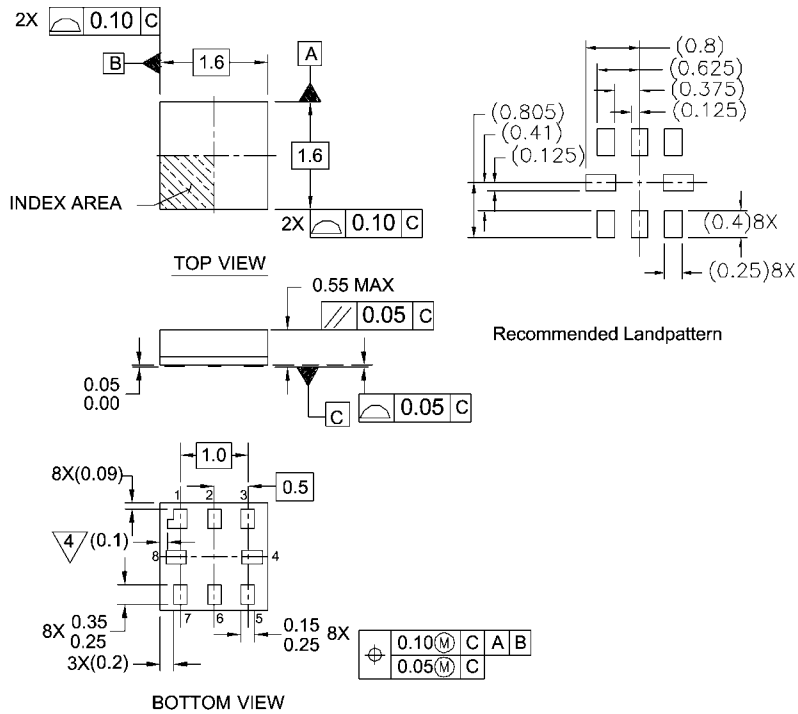
Notes:
1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

**Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC

www.onsemi.com