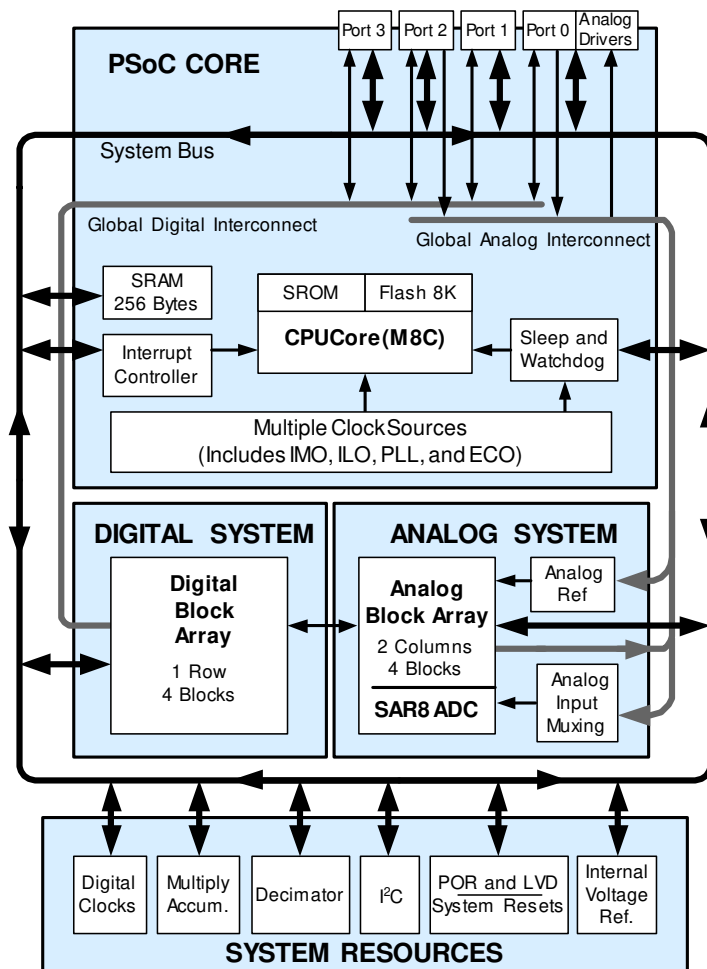## Features

- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - 8x8 Multiply, 32-Bit Accumulate
  - Low Power at High Speed
  - 3.0 to 5.25V Operating Voltage
  - Industrial Temperature Range: -40°C to +85°C
- Advanced Peripherals (PSoC® Blocks)
  - 4 Rail-to-Rail Analog PSoC Blocks Provide:
    - Up to 14-Bit ADCs
    - Up to 8-Bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - 4 Digital PSoC Blocks Provide:
    - 8 to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Full-Duplex UART
    - Multiple SPI Masters or Slaves
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
  - High speed 8-bit SAR ADC optimized for motor control
- Precision, Programmable Clocking
  - Internal ±5% 24/48 MHz Oscillator
  - High Accuracy 24 MHz with Optional 32 kHz Crystal and PLL
  - Optional External Oscillator, up to 24 MHz
  - Internal Oscillator for Watchdog and Sleep

- Flexible On-Chip Memory
  - 8K Bytes Flash Program Storage 50,000 Erase/Write Cycles
  - 256 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - 25 mA Sink on all GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Up to 10 Analog Inputs on GPIO
  - Two 30 mA Analog Outputs on GPIO
  - Configurable Interrupt on all GPIO
- Additional System Resources
  - I²C Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free development Software (PSoC Designer™)
  - Full-Featured In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory

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[+] Feedback

Block Diagram

Contents

PSoC Functional Overview

The PSoC family consists of many programmable system-on-chip with on-chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated in the Block Diagram, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global buses allows all the device resources to be combined into a complete custom system. The PSoC CY8C24x33 family can have up to three I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and four analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with 11 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 8 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to ±5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram
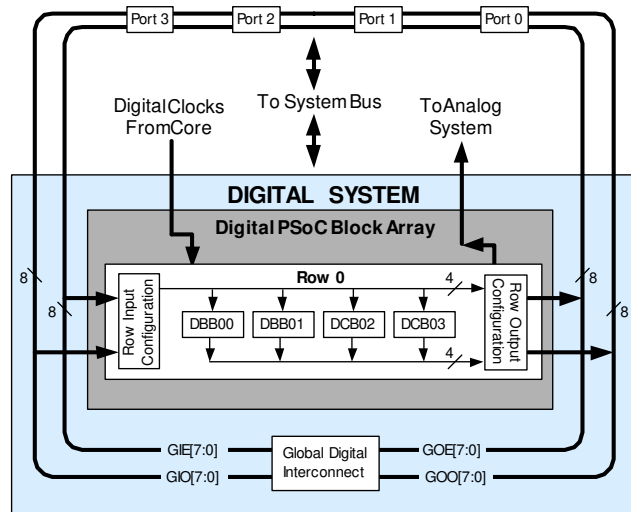
Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)

- PWMs with Dead Band (8 to 32 bit)

- Counters (8 to 32 bit)

- Timers (8 to 32 bit)

- UART 8 bit with selectable parity (up to 1)

- SPI master and slave (up to 1)

- I2C slave and master (1 available as a System Resource)

- Cyclical Redundancy Checker/Generator (8 to 32 bit)

- IrDA (up to 1)

- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks are connected to any GPIO through a series of global buses that route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 6.

The Analog System

The Analog system is composed of an 8-bit SAR ADC and four configurable blocks. The programmable 8-bit SAR ADC is an optimized ADC that runs up to 300 Ksps, with monotonic guarantee. It also has the features to support a motor control application.

Each analog block is comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Filters (2 and 4 pole band pass, low-pass, and notch)

- Amplifiers (up to 2, with selectable gain to 48x)

- Instrumentation amplifiers (1 with selectable gain to 93x)

- Comparators (up to 2, with 16 selectable thresholds)

- DACs (up to 2, with 6- to 9-bit resolution)

- Multiplying DACs (up to 2, with 6- to 9-bit resolution)

- High current output drivers (two with 30 mA drive as a Core Resource)

- 1.3V reference (as a System Resource)

- DTMF dialer

- Modulators

- Correlators

- Peak detectors

- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The Analog Column 0 contains the SAR8 ADC block rather than the standard SC blocks.

Figure 2. Analog System Block Diagram
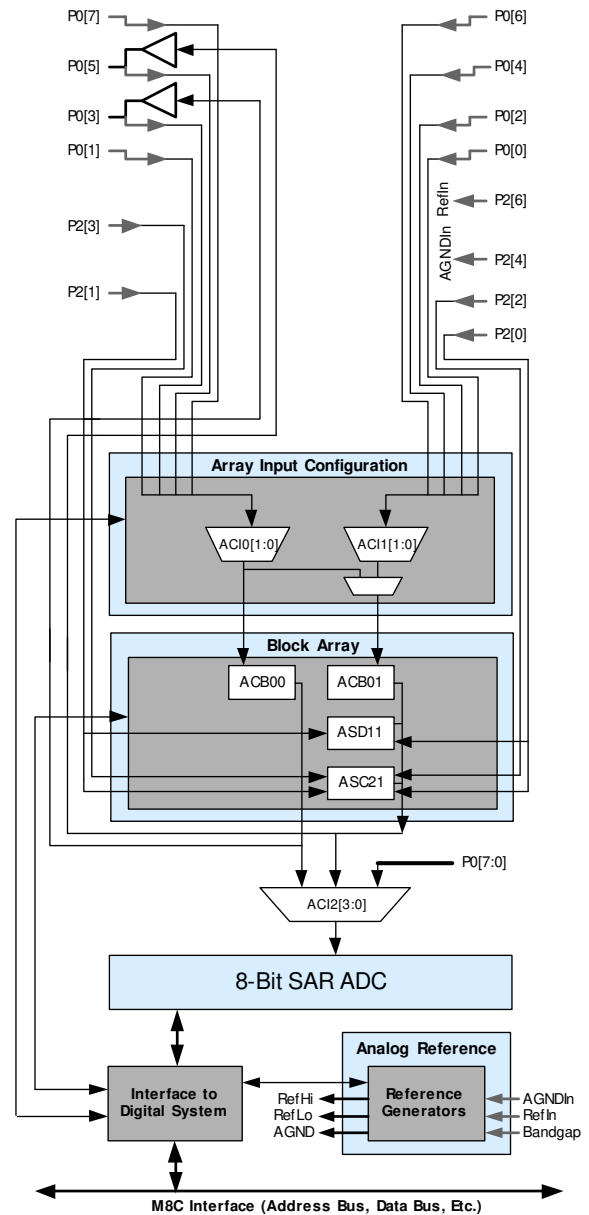
Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.

- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.

- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.

- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.

- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SAR8 ADC
CY8C29x66	up to 64	4	16	12	4	4	12	No
CY8C27x43	up to 44	2	8	12	4	4	12	No
CY8C24x94	56	1	4	48	2	2	6	No
CY8C24633	**up to 25**	**1**	**4**	**12**	**2**	**2**	**4**	**Yes**
CY8C24x23A	up to 24	1	4	12	2	2	6	No
CY8C21x34	up to 28	1	4	28	0	2	4[1]	No
CY8C21x23	16	1	4	8	0	2	4[1]	No
CY8C20x34	up to 28	0	0	28	0	0	3[2]	No

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the *PSoC Programmable System-on-Chip Technical Reference Manual* for CY8C24xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The

training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication inter-faces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC On-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called "drivers" and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called "user modules". User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms Used

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose I/O
I/O	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
RAM	random access memory
ROM	read only memory
SC	switched capacitor

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 7 on page 15 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

Pinouts

The PSoC CY8C24633 is available in 28-pin SSOP and 56-pin SSOP OCD packages. Refer to the following information for details. Every port pin (labeled with a "P"), except Vss, Vdd, and XRES in the following tables and illustrations, is capable of Digital I/O.

28-Pin Part Pinout

The 28-pin part is for the CY8C24633 PSoC device.

Table 3. 28-Pin Part Pinout (SSOP)

Pin No.	Digital	Analog	Pin Name	Description
1	I/O	I	P0[7]	Analog Col Mux IP and ADC IP
2	I/O	I/O	P0[5]	Analog Col Mux IP and Column O/P and ADC IP
3	I/O	I/O	P0[3]	Analog Col Mux IP and Column O/P and ADC IP
4	I/O	I	P0[1]	Analog Col Mux IP and ADC IP
5	I/O		P2[7]	GPIO
6	I/O		P2[5]	GPIO
7	I/O	I	P2[3]	Direct switched capacitor input
8	I/O	I	P2[1]	Direct switched capacitor input
9	I/O	AVref	P3[0][3]	GPIO/ADC Vref (optional)
10	I/O		P1[7]	I2C SCL
11	I/O		P1[5]	I2C SDA
12	I/O		P1[3]	GPIO
13	I/O		P1[1][4]	GPIO, Xtal input, I2C SCL, ISSP SCL
14	Power		Vss	Ground pin
15	I/O		P1[0][4]	GPIO, Xtal output, I2C SDA, ISSP SDA
16	I/O		P1[2]	GPIO
17	I/O		P1[4]	GPIO, external clock IP
18	I/O		P1[6]	GPIO
19			XRES	External reset
20	I/O	I	P2[0]	Direct switched capacitor input
21	I/O	I	P2[2]	Direct switched capacitor input
22	I/O		P2[4]	GPIO
23	I/O		P2[6]	GPIO
24	I/O	I	P0[0]	Analog Col Mux IP and ADC IP
25	I/O	I	P0[2]	Analog Col Mux IP and ADC IP
26	I/O	I	P0[4]	Analog Col Mux IP and ADC IP
27	I/O	I	P0[6]	Analog Col Mux IP and ADC IP
28	Power		Vdd	Supply voltage

LEGEND A = Analog, I = Input, and O = Output

Figure 3. CY8C24633 PSoC Device

Notes
3. Even though P3[0] is an odd port, it resides on the left side of the pinout.
4. ISSP pin, which is not High Z at POR.

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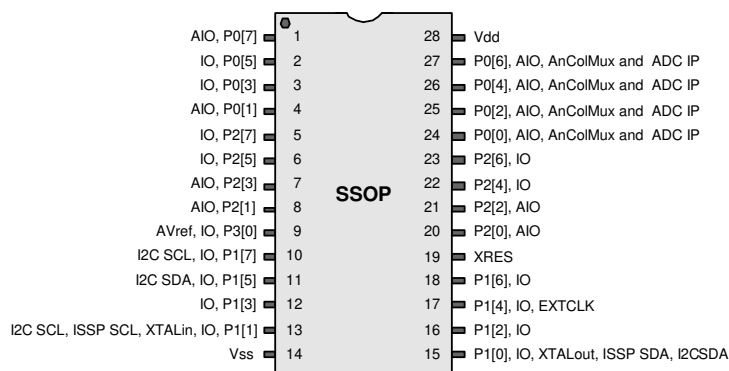
56-Pin Part Pinout

The 56-pin OCD (On-Chip Debug) part is for the CY8C24633 (CY8C24033) PSoC device.

**Note** OCD parts are only used for in-circuit debugging. OCD parts are NOT available for production.

Table 4. 56-Pin OCD Part Pinout (SSOP)

Pin No.	Name	Description
1	NC	No internal connection
2	P0[7]	Analog column mux input: AI
3	P0[5]	Analog column mux input and column output: AIO
4	P0[3]	Analog column mux input and column output: AIO
5	P0[1]	Analog column mux input: AI
6	P2[7]	
7	P2[5]	
8	P2[3]	Direct switched capacitor block input: AI
9	P2[1]	Direct switched capacitor block input: AI
10	NC	No internal connection
11	P3[0]	GPIO/ADC Vref (optional)
12	NC	No internal connection
13	NC	No internal connection
14	OCDE	OCD even data I/O
15	OCDO	OCD odd data output
16	NC	No internal connection
17	NC	No internal connection
18	NC	No internal connection
19	NC	No internal connection
20	NC	No internal connection
21	NC	No internal connection
22	NC	No internal connection
23	P1[7]	I2C Serial Clock (SCL)
24	P1[5]	I2C Serial Data (SDA)
25	NC	No internal connection
26	P1[3]	
27	P1[1][5]	Crystal (XTALin), I2C Serial Clock (SCL)
28	Vss	Ground connection
29	NC	No internal connection
30	NC	No internal connection
31	P1[0][5]	Crystal (XTALout), I2C Serial Data (SDA)
32	P1[2]	
33	P1[4]	Optional External Clock Input (EXTCLK)
34	P1[6]	
35	NC	No internal connection
36	NC	No internal connection
37	P3[1]	GPIO
38	NC	No internal connection
39	NC	No internal connection
40	NC	No internal connection
41	XRES	Active high pin reset with internal pull down
42	HCLK	OCD high speed clock output
43	CCLK	OCD CPU clock output

Figure 4. CY8C24033 OCD PSoC Device
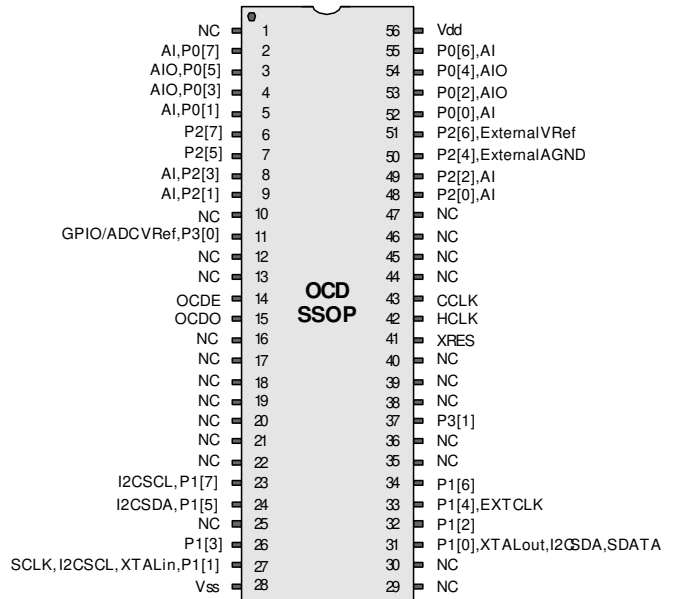
Not For Production

Pin No.	Name	Description
44	NC	No internal connection
45	NC	No internal connection
46	NC	No internal connection
47	NC	No internal connection
48	P2[0]	Direct switched capacitor block input: AI
49	P2[2]	Direct switched capacitor block input: AI
50	P2[4]	External Analog Ground (AGND)
51	P2[6]	External Voltage Reference (VRef)
52	P0[0]	Analog column mux input: AI
53	P0[2]	Analog column mux input and column output: AIO
54	P0[4]	Analog column mux input and column output: AIO
55	P0[6]	Analog column mux input: AI
56	Vdd	Supply voltage

LEGEND A = Analog, I = Input, O = Output.

Note
5. ISSP pin, which is not High Z at POR.

[+] Feedback

Register Reference

[+] Feedback

This section lists the registers of the CY8C24633 PSoC device by using mapping tables, in offset order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#	SARADC_DL	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL0_X	E8	W
DCB02DR1	29	W	SARADC_C0	69	#		A9		MUL0_Y	E9	W
DCB02DR2	2A	RW	SARADC_C1	6A	RW		AA		MUL0_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1 *	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved.   # Access is bit specific.

[+] Feedback

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68		SARADC_TRS	A8	RW	IMO_TR	E8	W
DCB02IN	29	RW		69		SARADC_TRCL	A9	RW	ILO_TR	E9	W
DCB02OU	2A	RW		6A		SARADC_TRCH	AA	RW	BDG_TR	EA	RW
	2B			6B		SARADC_C2	AB	#	ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW	SARADC_LCR	AC	RW		EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

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[+] Feedback

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24633 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.
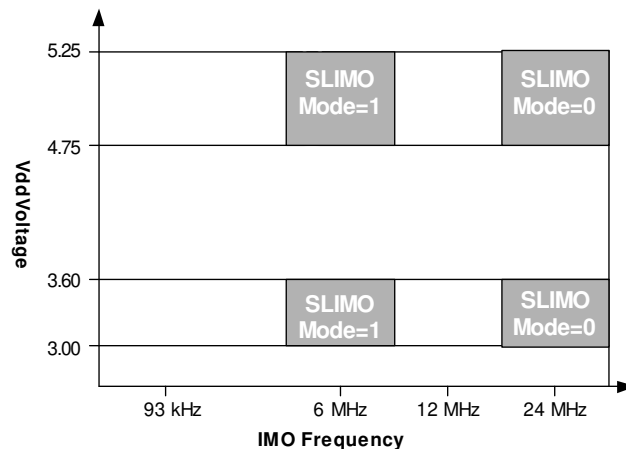
Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

Refer to Table 23 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 5. Voltage versus CPU Frequency
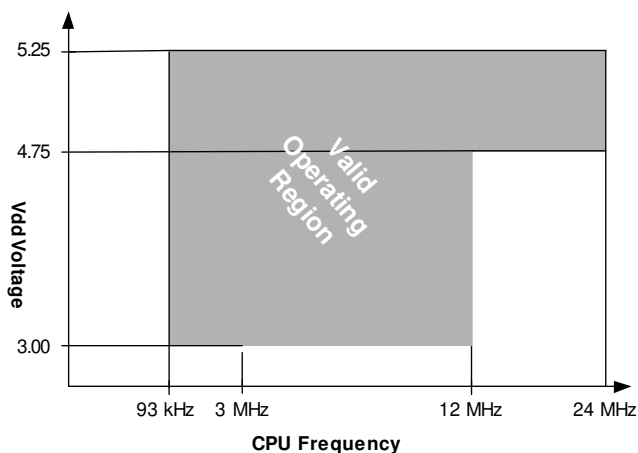
Figure 5a. IMO Frequency Trim Options

The following table lists the units of measure that are used in this section.

Table 7. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	μW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	pico ampere
MΩ	megaohm	pF	pico farad
μA	micro ampere	pp	peak-to-peak
μF	micro farad	ppm	parts per million
μH	micro henry	ps	picosecond
μs	microsecond	sps	samples per second
μV	micro volts	σ	sigma: one standard deviation
μVrms	micro volts root-mean-square	V	volts

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	^oC	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25^oC ± 25^oC. Extended duration storage temperatures above 65^oC degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	^oC	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch Up Current	–	–	200	mA	

Operating Temperature

Table 9. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	^oC	
T_J	Junction Temperature	-40	–	+100	^oC	The temperature rise from ambient to junction is package specific. See Thermal Impedances by Package on page 36. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 10. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See Table 20 on page 23.
I_{DD}	Supply Current	–	5	8	mA	Conditions are Vdd = 5.0V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{DD3}	Supply Current	–	3.3	6.0	mA	Conditions are Vdd = 3.3V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[6]	–	3	6.5	μA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C $\leq T_A \leq$ 55°C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[6]	–	4	25	μA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < $T_A \leq$ 85°C, analog power = off.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[6]	–	4	7.5	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. Vdd = 3.3V, -40 °C $\leq T_A \leq$ 55°C, analog power = off.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[6]	–	5	26	μA	Conditions are with properly loaded, 1μW max, 32.768 kHz crystal. Vdd = 3.3 V, 55 °C < $T_A \leq$ 85°C, analog power = off.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.30	1.33	V	Trimmed for appropriate Vdd. Vdd > 3.0V.

Note
6. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

[+] Feedback

DC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11. 5V and 3.3V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 100 mA maximum combined IOH budget.
I_{OH}	High Level Source Current	10	–	–	mA	
I_{OL}	Low Level Sink Current	25	–	–	mA	
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 12. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	– – –	1.6 1.3 1.2	10 8 7.5	mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	– – –	– – –	V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	– – –	– – –	0.2 0.2 0.5	V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	– – – – –	300 600 1200 2400 4600	400 800 1600 3200 6400	μA μA μA μA μA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	52	80	–	dB	Vss $\leq$ VIN $\leq$ (Vdd - 2.25) or (Vdd - 1.25V) $\leq$ VIN $\leq$ Vdd.

Table 13. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5V Only	– –	1.65 1.32	10 8	mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	– – –	– – –	V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	– – –	– – –	0.2 0.2 0.2	V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	– – – – –	300 600 1200 2400 4600	400 800 1600 3200 6400	μA μA μA μA μA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	52	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd..

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage Range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	μA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	μV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	– –	1 1	– –	W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32Ω to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32Ω to Vdd/2) Power = Low Power = High	– –	– –	0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	– –	1.1 2.6	5.1 8.8	mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	V_{OUT} > (Vdd - 1.25).

Table 16. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	μV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	– –	1 1	– –	W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 kΩ to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 kΩ to Vdd/2) Power = Low Power = High	– –	– –	0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	– –	0.8 2.0	2.0 4.3	mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	V_{OUT} > (Vdd - 1.25).

DC Analog Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 17. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
–	AGND = Vdd/2	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V
–	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

Table 18. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
–	AGND = Vdd/2	Vdd/2 - 0.03	Vdd/2 - 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 19.   DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R$_{CT}$	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register.

Table 20.   DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V$_{PPOR0}$ V$_{PPOR1}$ V$_{PPOR2}$	Vdd Value for PPOR Trip PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	– 	2.36 2.82 4.55	2.40 2.95 4.70	V V V	Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V$_{LVD0}$ V$_{LVD1}$ V$_{LVD2}$ V$_{LVD3}$ V$_{LVD4}$ V$_{LVD5}$ V$_{LVD6}$ V$_{LVD7}$	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.40 2.85 2.95 3.06 4.37 4.50 4.62 4.71	2.45 2.92 3.02 3.13 4.48 4.64 4.73 4.81	2.51[7] 2.99[8] 3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V V V	

Notes
7. Always greater than 50 mV above V$_{PPOR}$ (PORLEV=00) for falling supply.
8. Always greater than 50 mV above V$_{PPOR}$ (PORLEV=01) for falling supply.

[+] Feedback

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 21. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	3.3	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000[9]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[10]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

SAR8 ADC DC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. SAR8 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{ADCVREF}$	Reference Voltage at Pin P3[0] When Configured as ADC Reference Voltage	3.0	–	5.25	V	The voltage level at P3[0] (when configured as ADC reference voltage) should always be maintained to be less than chip supply voltage level on Vdd pin. $V_{ADCVREF}$ < Vdd.
$I_{ADCVREF}$	Current When P3[0] is Configured as ADC V_{REF}	3	–	–	mA	
INL	R-2R Integral Non-Linearity[11]	-1.2	–	+1.2	LSB	The maximum LSB is over a sub-range not exceeding 1/16 of the full-scale range.
DNL	R-2R Differential Non-Linearity[12]	-1	–	+1	LSB	Output is monatonic.

Notes
9. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 2.4V to 3.0V, 3.0V to 3.6V, and 4.75V to 5.25V.
10. A maximum of 36 x 50,000 block endurance cycles is allowed. This can be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
    For the full industrial range, use a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
11. At the 7F and 80 points, the maximum INL is 1.5 LSB.
12. For the 7F to 80 transition, the DNL specification is waived.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 23.   5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	22.8	24	25.2[13],[14],[15]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 5b on page 15. SLIMO mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[13],[14],[15]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 5b on page 15. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.093	24	24.6[13],[14]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.093	12	12.3[14],[15]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[13],[14],[16]	MHz	Refer to the Table 28 on page 30.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[14],[16]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	75	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	–	kHz	
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 °C ≤ T_A ≤ 85 °C.
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[13],[15]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared	–	–	600	ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	NA	–	–	µs	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	
$T_{POWERUP}$	Time from End of POR to CPU Executing Code	–	16	100	ms	

Notes
13. 4.75V < Vdd < 5.25V.
14. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
15. 3.0V < Vdd < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.
16. See the individual user module data sheets for information on maximum frequencies for user modules.

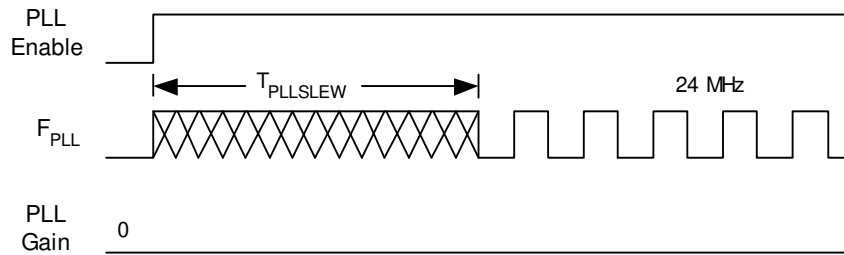**Figure 6. PLL Lock Timing Diagram**
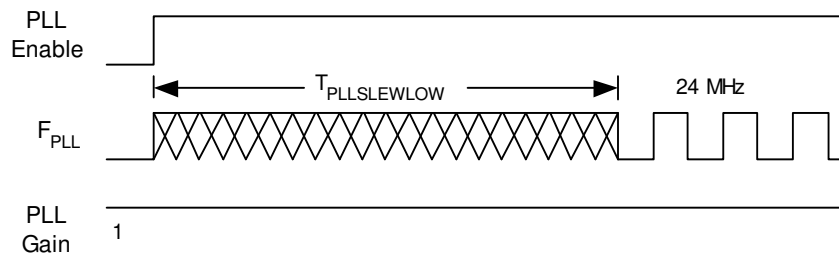

Figure 7. PLL Lock for Low Gain Setting Timing Diagram

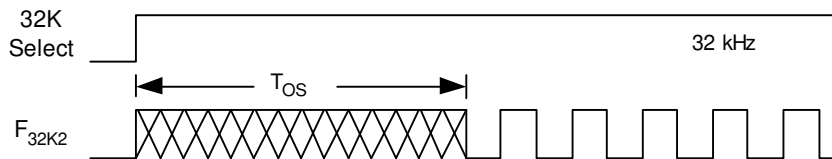**Figure 8. External Crystal Oscillator Startup Timing Diagram**

Figure 9. 24 MHz Period Jitter (IMO) Timing Diagram

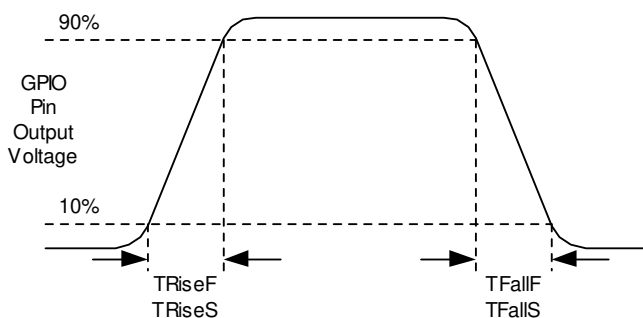**Figure 10. 32 kHz Period Jitter (ECO) Timing Diagram**

AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 24.   5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 11. GPIO Timing Diagram

[+] Feedback

AC Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 25. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	– – –	– – –	3.9 0.72 0.62	μs μs μs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	– – –	– – –	5.9 0.92 0.72	μs μs μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	0.15 1.7 6.5	– – –	– – –	V/μs V/μs V/μs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	0.01 0.5 4.0	– – –	– – –	V/μs V/μs V/μs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	0.75 3.1 5.4	– – –	– – –	MHz MHz MHz	

Table 26. 3.3V AC Operational Amplifier Specifications

| Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	– –	– –	3.92 0.72	μs μs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	– –	– –	5.41 0.72	μs μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	0.31 2.7	– –	– –	V/μs V/μs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	0.24 1.8	– –	– –	V/μs V/μs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	0.67 2.8	– –	– –	MHz MHz	

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 12. Typical AGND Noise with P2[4] Bypass
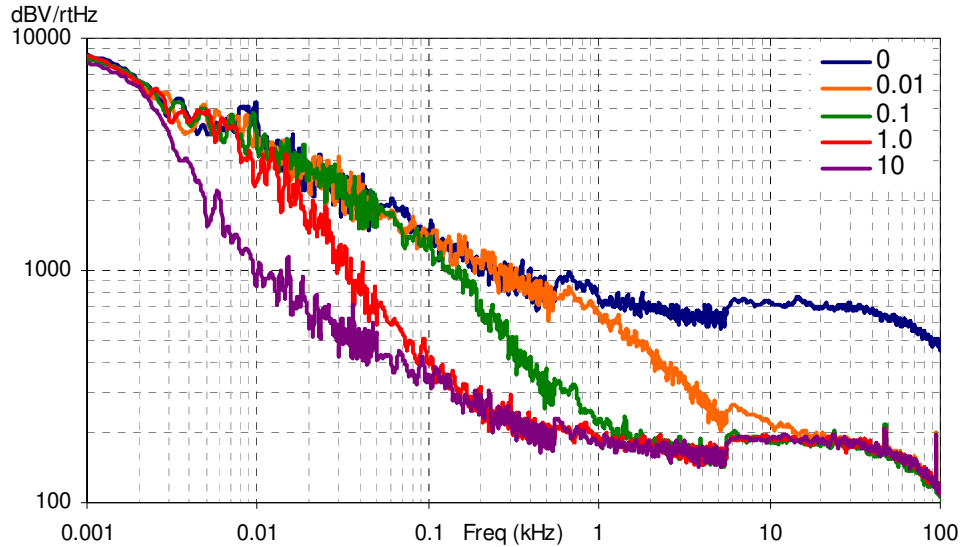
At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 13. Typical Opamp Noise
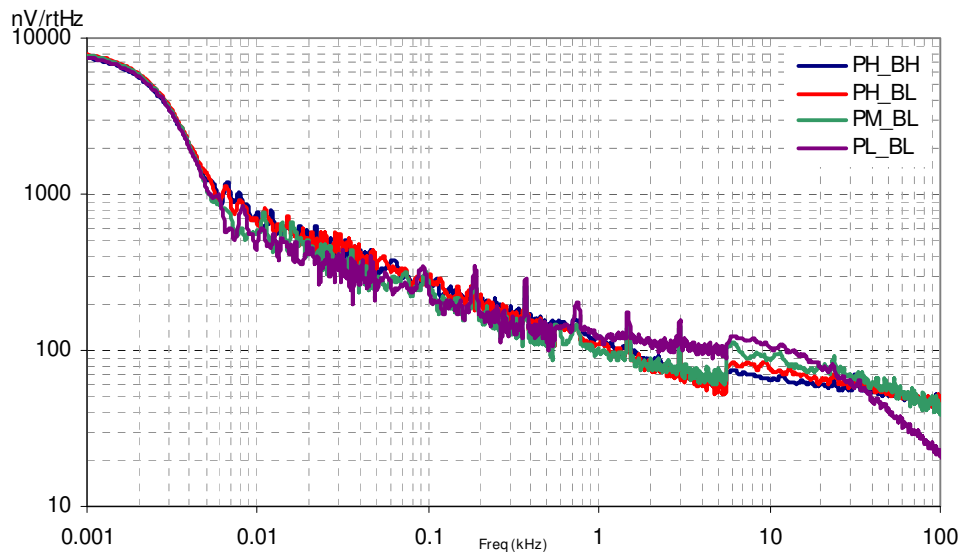
AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 27.   AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 28.   5V and 3.3V AC Digital Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[17]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50[17]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[17]	–	–	ns	
	Disable Mode	50[17]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[17]	–	–	ns	
Trans-mitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd Š 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd Š 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

Note
17. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 29. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.5 2.5	 μs μs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.2 2.2	 μs μs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/μs V/μs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/μs V/μs	
BW_{OB}	Small Signal Bandwidth, 20 mV$_{pp}$, 3dB BW, 100 pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OB}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100 pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz	

Table 30. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 3.8 3.8	 μs μs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.6 2.6	 μs μs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/μs V/μs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/μs V/μs	
BW_{OB}	Small Signal Bandwidth, 20 mV$_{pp}$, 3dB BW, 100 pF Load Power = Low Power = High	 0.7 0.7	 – –	 – –	 MHz MHz	
BW_{OB}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100 pF Load Power = Low Power = High	 200 200	 – –	 – –	 kHz kHz	

[+] Feedback

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 31.   5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	μs	

Table 32.   3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock Divide by 1[18]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU Clock Divide by 2 or Greater[19]	0.186	–	24.6	MHz	
–	High Period with CPU Clock Divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock Divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	μs	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 33.   AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	20	–	ms	
T_{WRITE}	Flash Block Write Time	–	80	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once.
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	200	ms	0°C ≤ T_J ≤ 100°C
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	400	ms	-40°C ≤ T_J ≤ 0°C

Notes
18. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
19. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

SAR8 ADC AC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 34. SAR8 ADC AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$Freq_3$	Input clock frequency 3V	–	–	3.0	MHz	
$Freq_5$	Input clock frequency 5V	–	–	3.0	MHz	

AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 35. AC Characteristics of the I²C SDA and SCL Pins for Vdd > 3.0V

Symbol	Description	Standard-Mode Min	Standard-Mode Max	Fast-Mode Min	Fast-Mode Max	Units	Notes
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	μs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	μs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	μs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	μs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[20]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	μs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	μs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Note
20. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $T_{SUDATI2C}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $T_{SUDATI2C}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

[+] Feedback

Table 36. AC Characteristics of the I^{2}C SDA and SCL Pins for Vdd < 3.0V (Fast-Mode Not Supported)

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F$_{SCLI2C}$	SCL Clock Frequency	0	100	–	–	kHz	
T$_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	μs	
T$_{LOWI2C}$	LOW Period of the SCL Clock	4.7	–	–	–	μs	
T$_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	–	–	μs	
T$_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	–	–	μs	
T$_{HDDATI2C}$	Data Hold Time	0	–	–	–	μs	
T$_{SUDATI2C}$	Data Set-up Time	250	–	–	–	ns	
T$_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	–	–	μs	
T$_{BUFI2C}$	Bus Free Time Between a STOP and START Condition	4.7	–	–	–	μs	
T$_{SPI2C}$	Pulse Width of spikes are suppressed by the input filter.	–	–	–	–	ns	

Figure 14. Definition for Timing for Fast-/Standard-Mode on the I^{2}C Bus
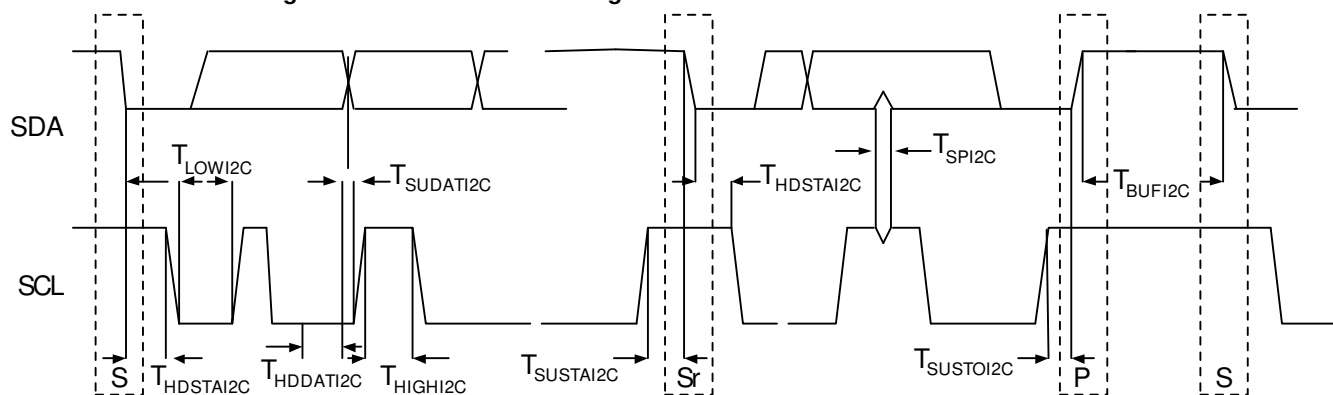
Packaging Information

This section illustrates the packaging specifications for the CY8C24633 PSoC device, along with the thermal impedances for each package, solder reflow peak temperature, and the typical package capacitance on crystal pins.

Figure 15. 28-Pin (210-Mil) SSOP
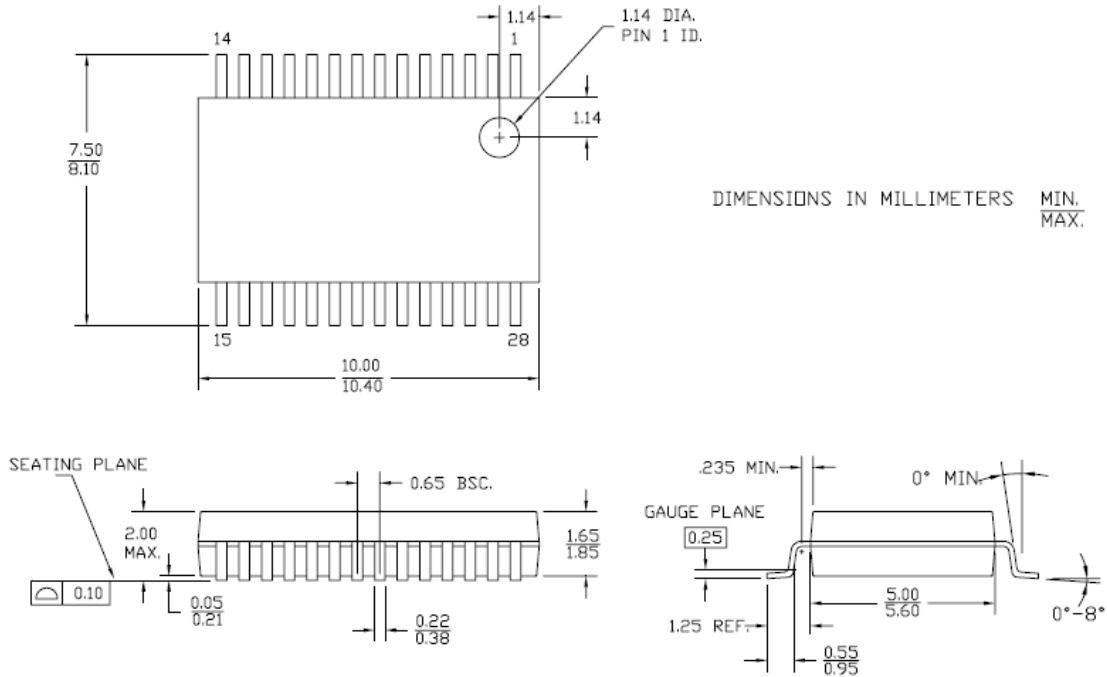
51-85079 *D

Figure 16. 56-Pin (300-Mil) SSOP

51-85062 *D

[+] Feedback
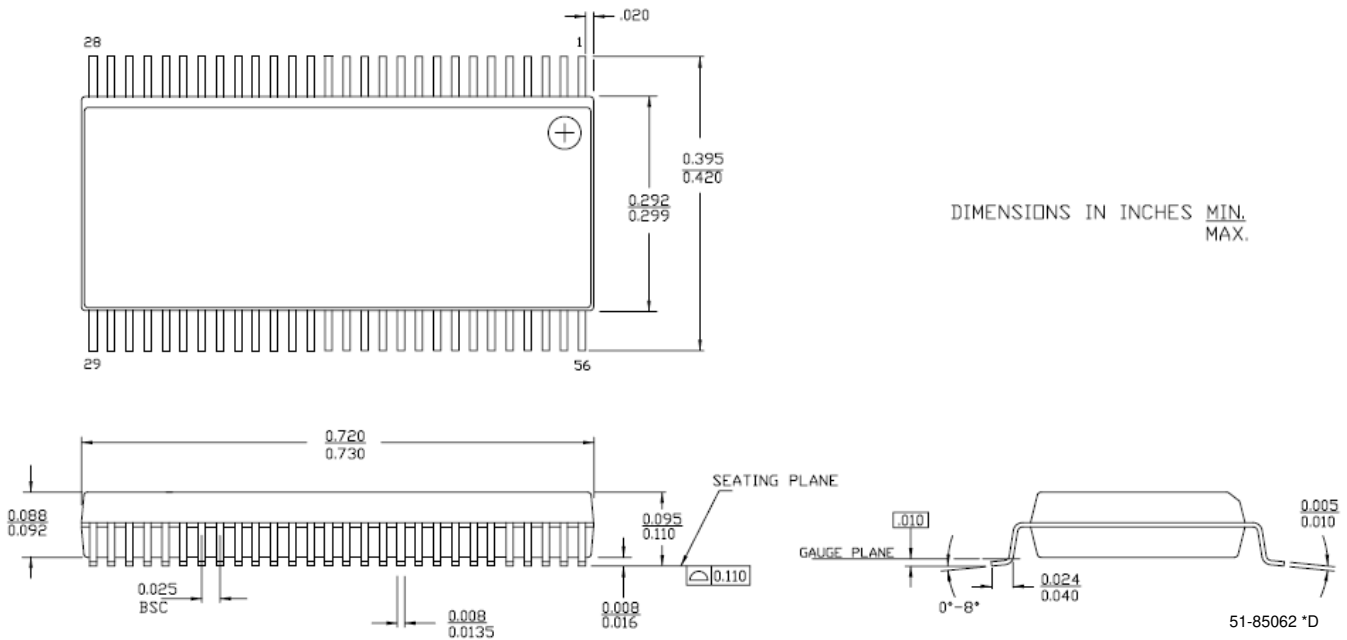
Thermal Impedances

Table 37. Thermal Impedances by Package

Package	Typical θ_{JA} [21]
28 SSOP	95 ^{o}C/W
56 SSOP	67 ^{o}C/W

Capacitance on Crystal Pins

Table 38. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance	
28 SSOP	2.8 pF	
56 SSOP	Pin 27 0.33 pF	Pin 31 0.35 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 39. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [22]	Maximum Peak Temperature
28 SSOP	240°C	260°C
56 SSOP	240°C	260°C

Ordering Information

The following table lists the CY8C24633 PSoC device family key package features and ordering codes.

Table 40. CY8C24x33 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-Pin (210 Mil) SSOP	CY8C24633-24PVXI	8	256	-40°C to +85°C	4	4	25	12	2	Yes
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C24633-24PVXIT	8	256	-40°C to +85°C	4	4	25	12	2	Yes
56-Pin OCD SSOP	CY8C24033-24PVXI[23]	8	256	-40°C to +85°C	4	4	24	12	2	Yes

Notes
21. $T_J = T_A + POWER \times \theta_{JA}$.
22. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.
23. This part may be used for in-circuit debugging. It is NOT available for production.

Document History Page

Document Title: CY8C24633 PSoC® Programmable-System-on-Chip				
Document Number: 001-20160				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1411003	HMT	See ECN	New spec. Separate device from 001-14643.
*A	1648723	HMT	See ECN	Update SAR ADC electrical specs. Update INL, DNL, and VOL specs. Finetune specs. Add 56 SSOP package capacitance data. Change title. Make data sheet Final.
*B	2763970	POA/AESA	09/16/2009	Update Getting Started, Development Tools, and Designing with PSoC Designer sections.
*C	2871212	JHU/HMT	02/04/2010	■ Add Table of Contents. ■ Update DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: ❏ Add IOH, IOL. Existing parameter. Previously only in "Notes" section of VOH/VOL. Now added as a separate line item for ease of location in data sheet. ❏ Add Flash Endurance Note regarding the programming and verifying Flash should be in the same voltage range. Added to clarify Flash behavior for the customer. ❏ Add F32K_U to clarify minimum ILO frequency out before the part boots up. ❏ Add DCILO upon request from a few customers. ❏ Add TPOWERUP, typical amount of time taken by PSoC to begin executing code out of Flash after powerup. Added to clarify PSoC behavior at startup for customer. ❏ Revise FIMO6 limits. No impact to form, fit, function, or customer application. ❏ Revise TRAMP from 0 to NA. Replace TRAMP (time) with SRPOWER_UP to accurately define the powerup requirement. ❏ Add SRPOWER_UP, change from no limitation to limitations based on test equipment ratings, to which the part will now be tested. ❏ Add TPROGRAM_HOT of maximum time it takes to erase and program a block when die temperature is >0°C. Added to clarify Flash behavior to the customer. ❏ Add TPROGRAM_COLD of maximum time it takes to erase and program a block over the full temperature range (–40°C to 85°C). Added to clarify Flash behavior to the customer. ❏ Revise TWRITE to align with recommended values for third party programmers. Data sheet now matches the typical value as recommended. ■ Update copyright and Sales, Solutions, and Legal Information URLs. ■ Update 28-Pin SSOP package diagram.

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