20 GHz to 54 GHz, GaAs, pHEMT, MMIC, 31 dBm (1 W) Power Amplifier

FEATURES

- Output P1dB: 30 dBm typical at 22 GHz to 40 GHz
- P_{SAT}: 31 dBm typical at 22 GHz to 40 GHz
- Gain: 17.5 dB typical at 22 GHz to 40 GHz
- Input return loss: 12 dB typical at 22 GHz to 40 GHz
- Output return loss: 9.5 dB typical at 22 GHz to 40 GHz
- Output IP3: 37 dBm typical at 22 GHz to 40 GHz
- Supply voltage: 5 V typical at 1500 mA
- 50 Ω matched input and output
- 18-terminal, 7 mm × 7 mm, ceramic leadless chip carrier with heat sink [LCC_HS]
- Integrated power detector

APPLICATIONS

- Aerospace and defense
- Test instrumentation
- Communications

GENERAL DESCRIPTION

The ADPA7008 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), 31 dBm saturated output power (P_{SAT}, 1 W) distributed power amplifier with an integrated temperature compensated on-chip power detector that operates from 20 GHz to 54 GHz. The amplifier provides 17.5 dB of small signal gain, an output power for 1 dB compression (P1dB) of 30 dBm with an excellent IP3 of 37 dBm typical from 22 GHz to 40 GHz. The ADPA7008 is ideal for linear applications such as electronic countermeasure and instrumentation applications requiring 31 dBm of efficient P_{SAT}. The ADPA7008 requires 1500 mA from a 5 V supply voltage (V_{DD}). The RF input and outputs are internally matched and dc blocked for ease of integration into higher level assemblies. The ADPA7008 is housed in a 7 mm × 7 mm, ceramic leadless package with heat sink [LCC_HS] that exhibits low thermal resistance and is compatible with surface-mount manufacturing techniques.

FUNCTIONAL BLOCK DIAGRAM

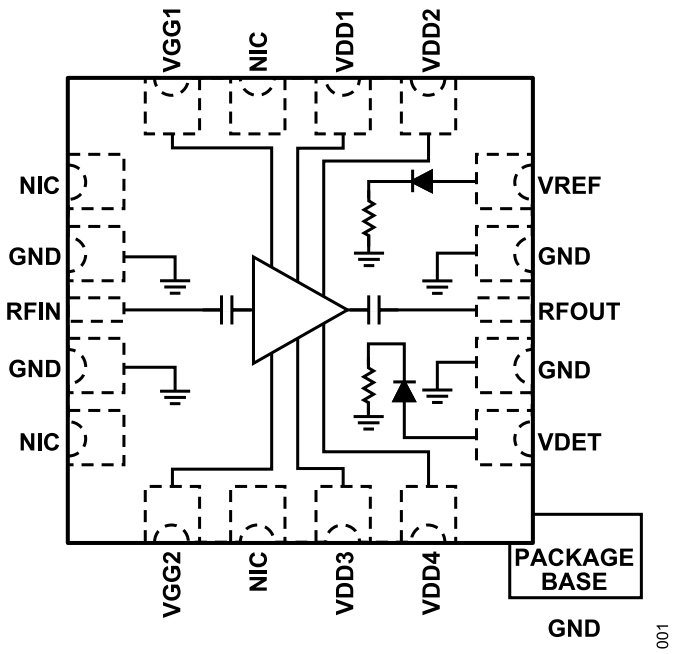

Figure 1.

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REVISION HISTORY

7/2021—Revision 0: Initial Version

SPECIFICATIONS

20 GHZ TO 22 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, quiescent supply current (I_{DQ}) = 1500 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GG1} from −1.5 V to −0.4 V to achieve I_{DQ} = 1500 mA typical.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		22	GHz	
GAIN		14.5	17		dB	
Gain Flatness			±0.3		dB	
Gain Variation Over Temperature			0.022		dB/°C	
NOISE FIGURE			8		dB	
RETURN LOSS						
Input			14		dB	
Output			12		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	26.5	29		dBm	
Saturated Output Power	P_{SAT}		30		dBm	
Output Third-Order Intercept	IP3		34		dBm	Output power (P_{OUT}) per tone = 14 dBm with 1 MHz tone spacing
POWER ADDED EFFICIENCY	PAE		10		%	Measured at P_{SAT}
SUPPLY						
Quiescent Current	I_{DQ}		1500		mA	Adjust V_{GG1}, from −1.5 V up to −0.4 V to achieve the desired I_{DQ}, VGGx = −0.63 V typical to achieve I_{DQ}= 1500 mA
Voltage	V_{DD}	4	5		V	

22 GHZ TO 40 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 1500 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GG1} from −1.5 V to −0.4 V to achieve I_{DQ} = 1500 mA typical.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		22		40	GHz	
GAIN		15	17.5		dB	
Gain Flatness			±1.2		dB	
Gain Variation Over Temperature			0.022		dB/°C	
NOISE FIGURE			7.0		dB	
RETURN LOSS						
Input			12		dB	
Output			9.5		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	27.5	30		dBm	
Saturated Output Power	P_{SAT}		31		dBm	
Output Third-Order Intercept	IP3		37		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
POWER ADDED EFFICIENCY	PAE	11.5			%	Measured at P_{SAT}
SUPPLY						
Quiescent Current	I_{DQ}		1500		mA	Adjust V_{GG1}, from −1.5 V up to −0.4 V to achieve the desired I_{DQ}, V_{GGx} = −0.63 V typical to achieve I_{DQ}= 1500 mA
Voltage	V_{DD}	4	5		V	

SPECIFICATIONS

40 GHZ TO 50 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 1500 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GG1} from −1.5 V to −0.4 V to achieve I_{DQ} = 1500 mA typical.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		40		50	GHz	
GAIN			16		dB	
Gain Flatness			±1.1		dB	
Gain Variation Over Temperature			0.039		dB/°C	
NOISE FIGURE			7		dB	
RETURN LOSS						
Input			15		dB	
Output			13		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		27.5		dBm	
Saturated Output Power	P_{SAT}		29		dBm	
Output Third-Order Intercept	IP3		36		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
POWER ADDED EFFICIENCY	PAE		7		%	Measured at P_{SAT}
SUPPLY						
Quiescent Current	I_{DQ}		1500		mA	Adjust V_{GG1}, from −1.5 V up to −0.4 V to achieve the desired I_{DQ}, V_{GGx} = −0.63 V typical to achieve I_{DQ}= 1500 mA
Voltage	V_{DD}	4	5		V	

50 GHZ TO 54 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 1500 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GG1} from −1.5 V to −0.4 V to achieve I_{DQ} = 1500 mA typical.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		50		54	GHz	
GAIN			15.5		dB	
Gain Flatness			±1.0		dB	
Gain Variation Over Temperature			0.049		dB/°C	
RETURN LOSS						
Input			10		dB	
Output			9		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		24.5		dBm	
Saturated Output Power	P_{SAT}		27		dBm	
Output Third-Order Intercept	IP3		35		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
POWER ADDED EFFICIENCY	PAE		4		%	Measured at P_{SAT}
SUPPLY						
Quiescent Current	I_{DQ}		1500		mA	Adjust V_{GG1}, from −1.5 V up to −0.4 V to achieve the desired I_{DQ}, V_{GGx} = −0.63 V typical to achieve I_{DQ} = 1500 mA
Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DDx})	6.0 V
V_{GGx}	−1.6 V to 0 V
RF Input Power (RFIN)	22 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 123 mW/°C Above 85°C)	11.1 W
Temperature	
Maximum Channel to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Quiescent Channel (T_J = 85°C, V_{DD} = 5 V, I_{DQ} = 1500 mA)	130°C
Storage	−65°C to +150°C
Operating	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance (the channel to the exposed metal ground pad on the underside of the device).

Table 6. Thermal Resistance

Package Type[1]	θ_{JC}	Unit
EH-18-1		
Quiescent, T_{BASE} = 85°C	6.0	°C/W
Worst Case[2], T_{BASE} = 85°C	8.1	°C/W

[1] The thermal resistance varies with operating conditions.

[2] The worst case across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA7008

Table 7. ADPA7008, 18-Terminal LCC_HS

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

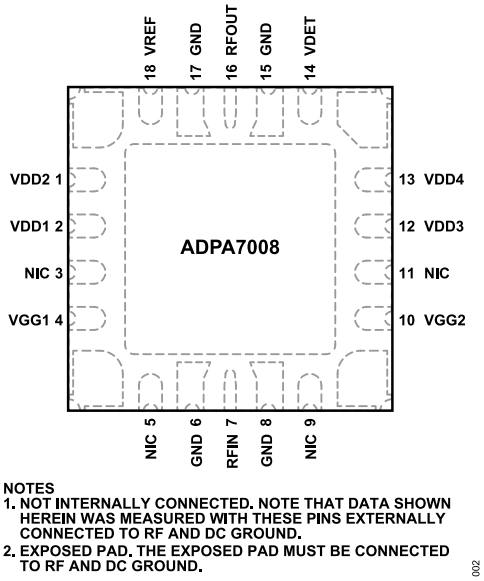

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 12, 13	VDD1 to VDD4	Drain Biases for the Amplifier. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required for these pins. See Figure 9 for the interface schematic.
3, 5, 9, 11	NIC	Not Internally Connected. The NIC pins have no internal connections.
4, 10	VGG1, VGG2	Amplifier Gate Controls. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required for these pins. Adjust V_{GG1} from −1.5 V to −0.4 V to achieve the desired I_{DQ}. See Figure 7 for the interface schematic .
6, 8, 15, 17	GND	Ground Pins. Connect the GND pins to RF and dc ground.
7	RFIN	RF Signal Input. The RFIN pin is ac-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
14	VDET	Detector Diode Used for Measuring the RF Output Power. Detection via the VDET pin requires the application of a dc bias voltage through an external series resistor. Used in combination with VREF, the difference detector voltage, VREF − VDET, is a temperature compensated dc voltage proportional to the RF output power (P_{OUT}). See Figure 5 for the interface schematic.
16	RFOUT	RF Signal Output. The RFOUT pin is ac-coupled and matched to 50 Ω. See Figure 8 for the interface schematic.
18	VREF	Reference Diode Voltage. Use the VREF pin for temperature compensation of the VDET RF P_{OUT} measurements. Used in combination with VDET, this voltage provides temperature compensation to the VDET RF P_{OUT} measurements. See Figure 4 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

Figure 4. VREF Interface Schematic

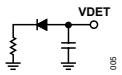

Figure 5. VDET Interface Schematic

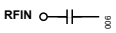

Figure 6. RFIN Interface Schematic

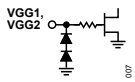

Figure 7. VGG1, VGG2 Interface Schematic

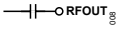

Figure 8. RFOUT Interface Schematic

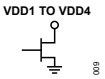

Figure 9. VDD1 to VDD4 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

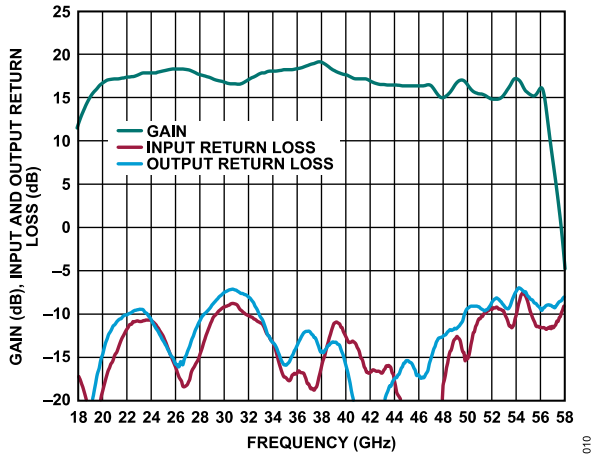

Figure 10. Gain and Input and Output Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 1500 mA

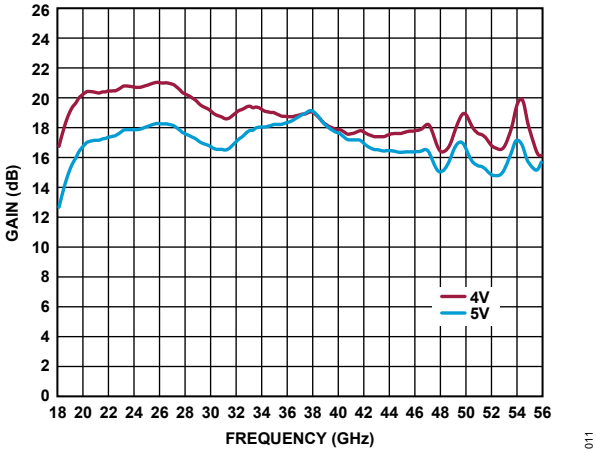

Figure 11. Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 1500 mA

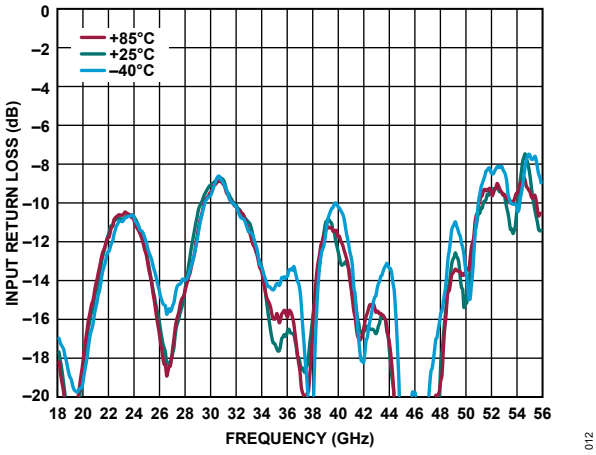

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

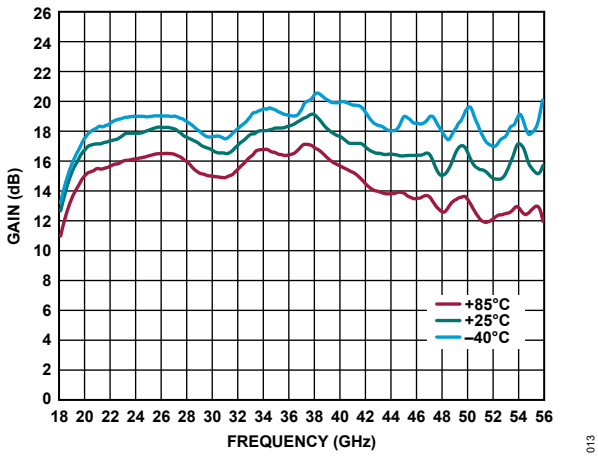

Figure 13. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

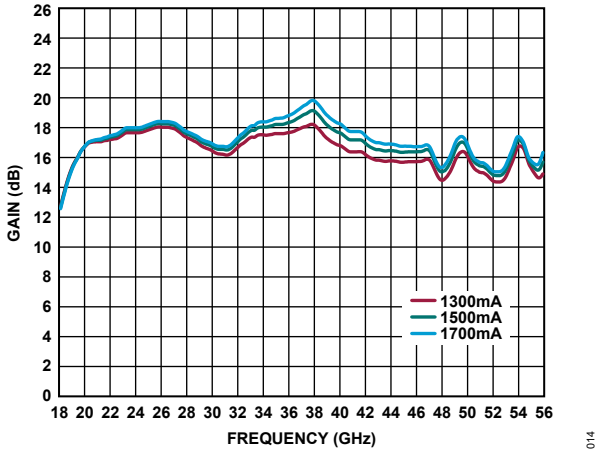

Figure 14. Gain vs. Frequency for Various Supply Currents, V_{DD} = 5 V

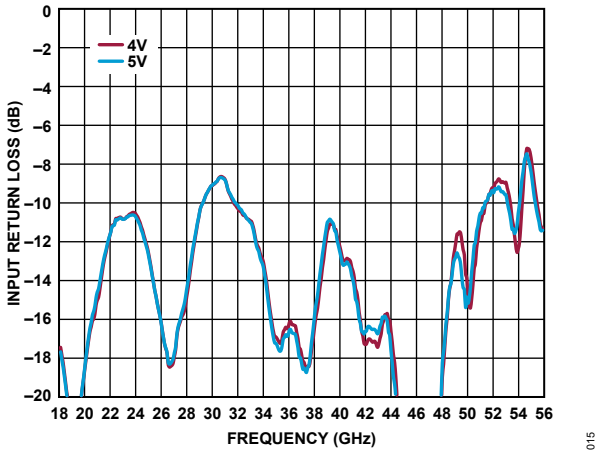

Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 1500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

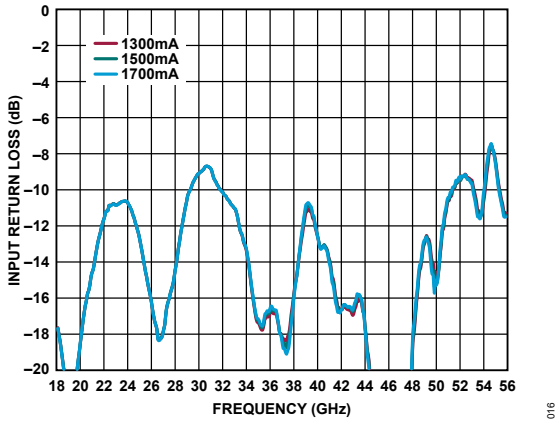

Figure 16. Input Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 5 V

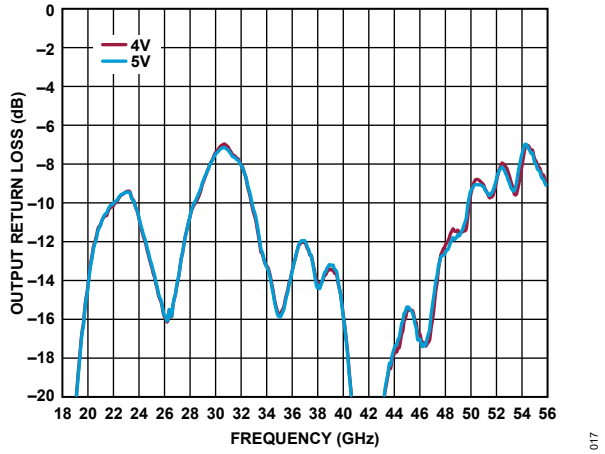

Figure 17. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 1500 mA

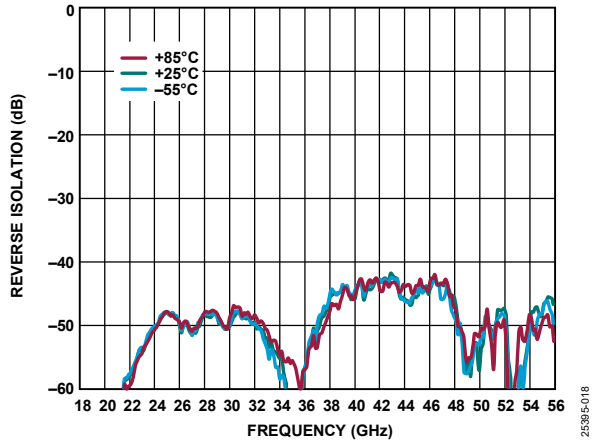

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

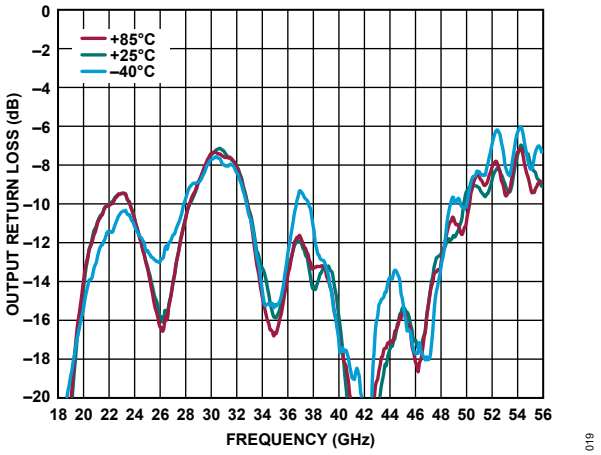

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

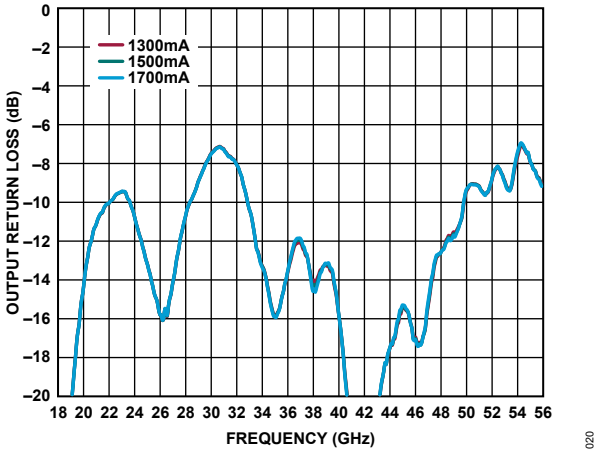

Figure 20. Output Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 5 V

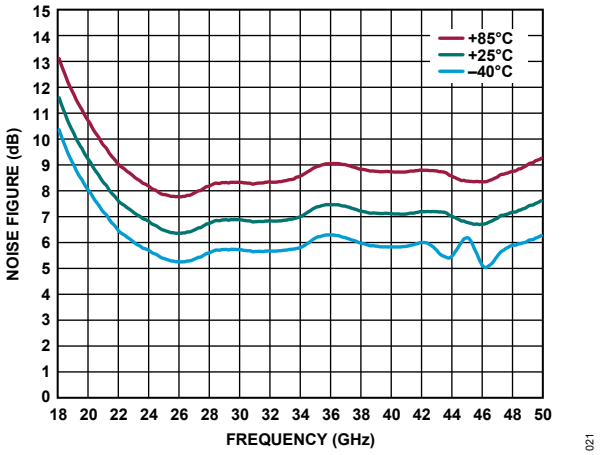

Figure 21. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

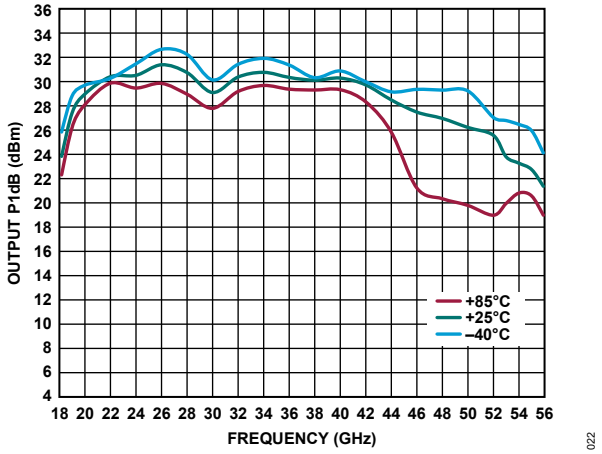

Figure 22. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

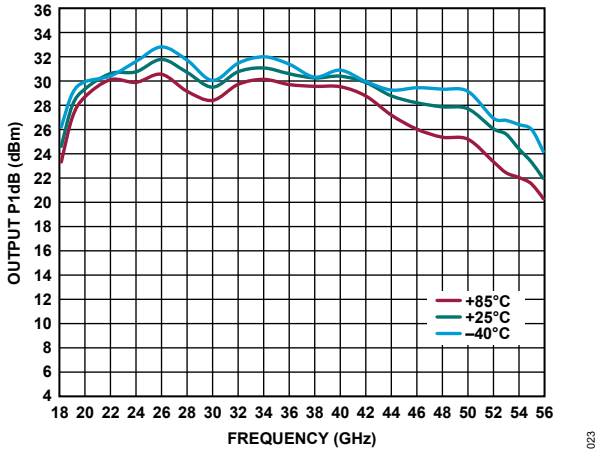

Figure 23. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1700 mA

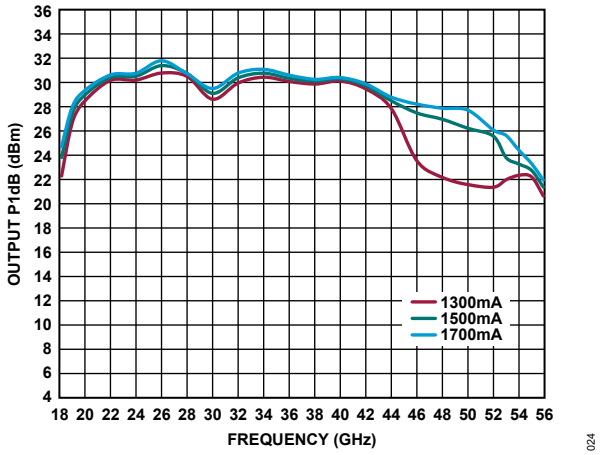

Figure 24. Output P1dB vs. Frequency for Various Supply Currents, V_{DD} = 5 V

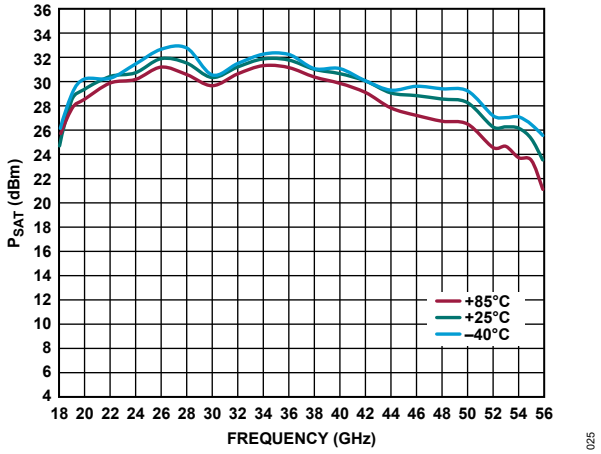

Figure 25. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

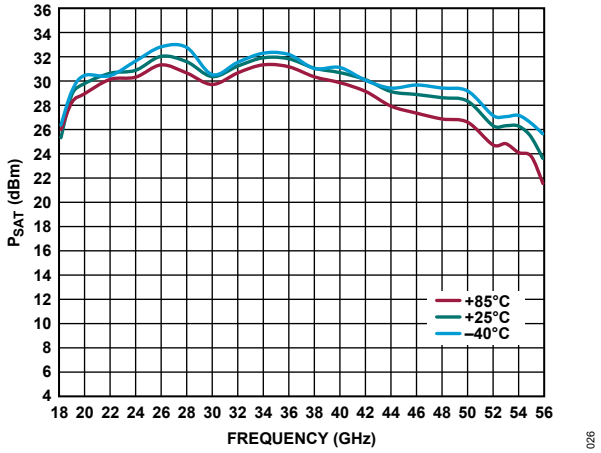

Figure 26. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1700 mA

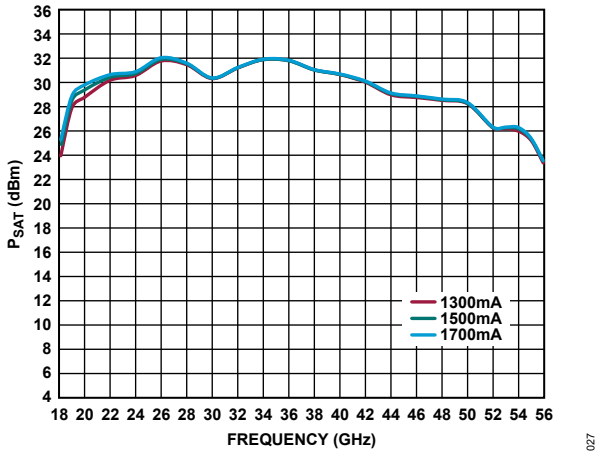

Figure 27. P_{SAT} vs. Frequency for Various Supply Currents, V_{DD} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

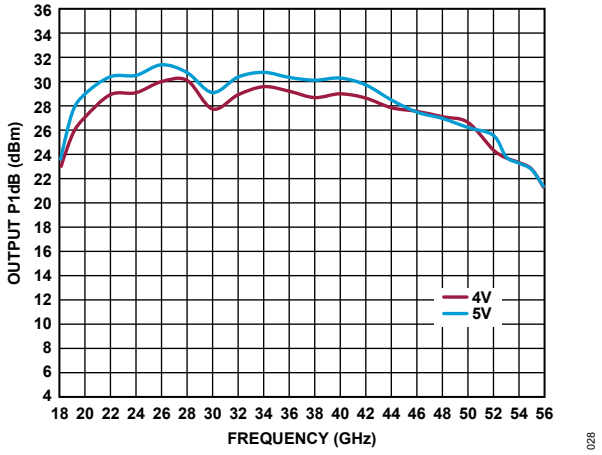

Figure 28. Output P1dB vs. Frequency for Various Supply Voltages, I_{DQ} = 1500 mA

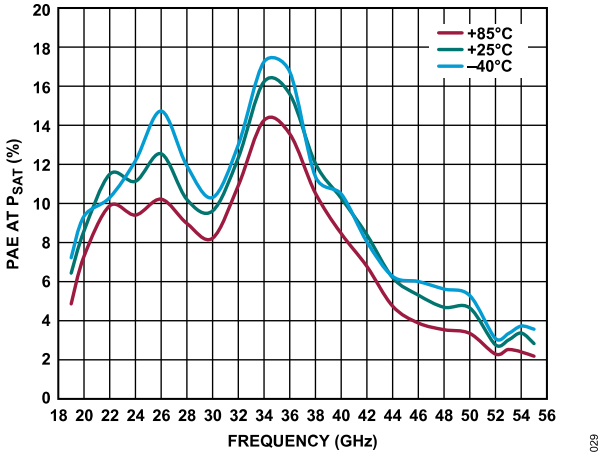

Figure 29. Power Added Efficiency (PAE) at P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1500 mA

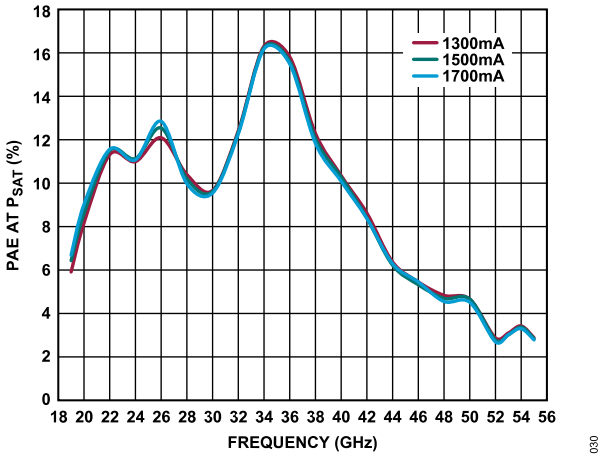

Figure 30. PAE at P_{SAT} vs. Frequency for Various Supply Currents, V_{DD} = 5 V

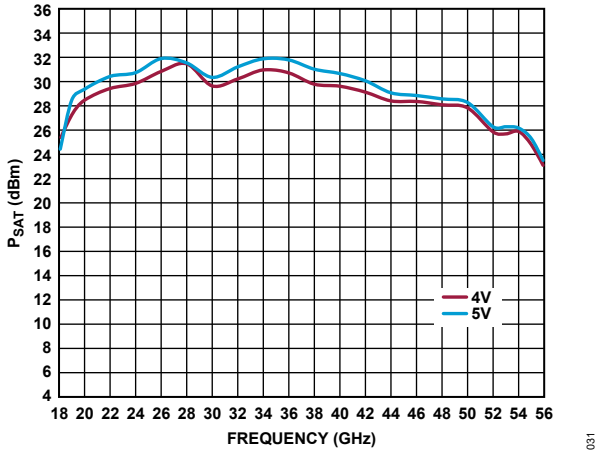

Figure 31. P_{SAT} vs. Frequency for Various Voltages, I_{DQ} = 1500 mA

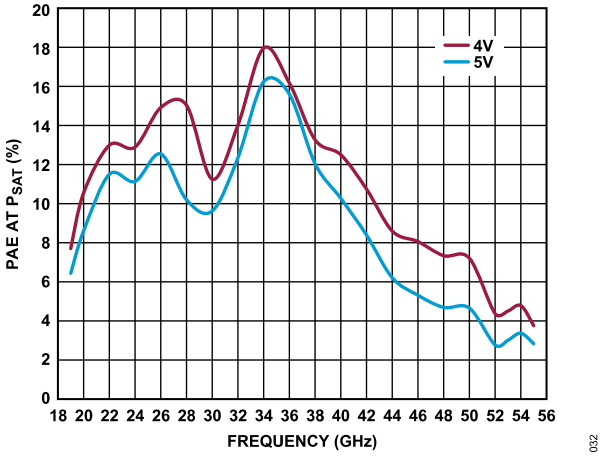

Figure 32. PAE at P_{SAT} vs. Frequency for Various Supply Voltages, I_{DQ} = 1500 mA

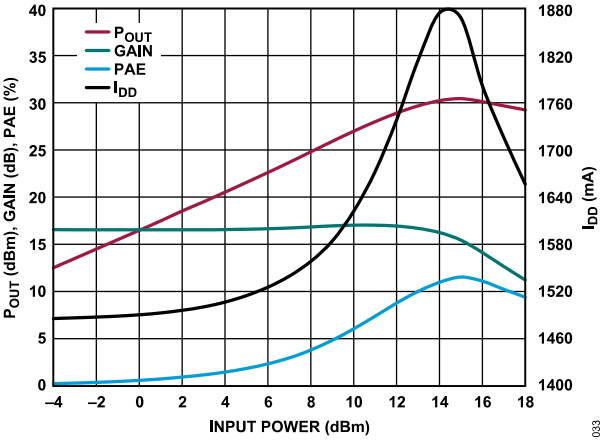

Figure 33. P_{OUT}, Gain, PAE, and Drain Current with RF Applied (I_{DD}) vs. Input Power, 22 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

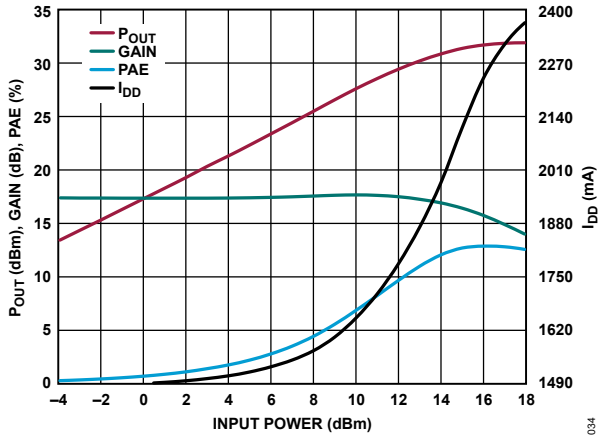

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 26 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

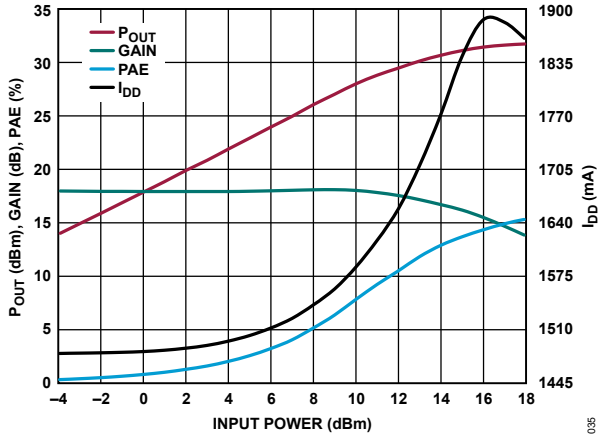

Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 36 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

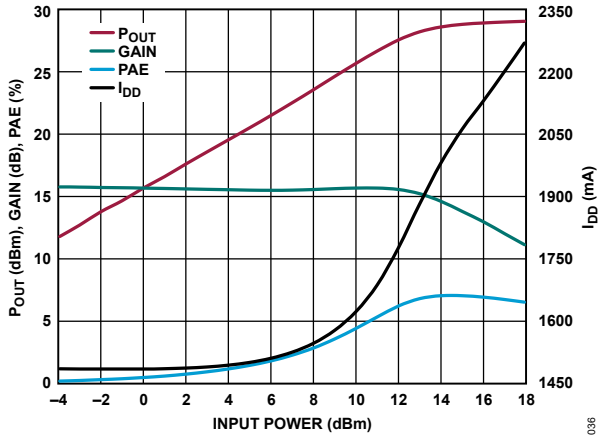

Figure 36. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 44 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

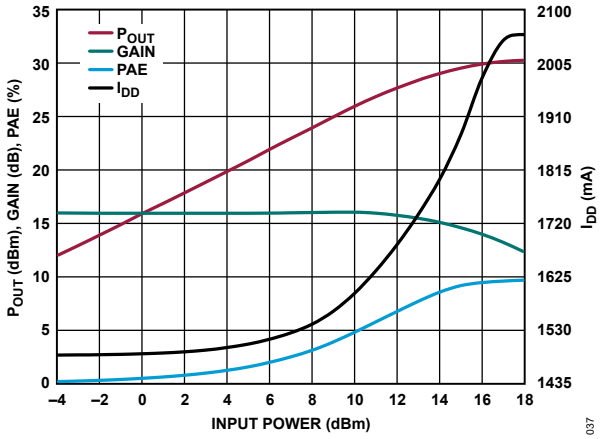

Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 30 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

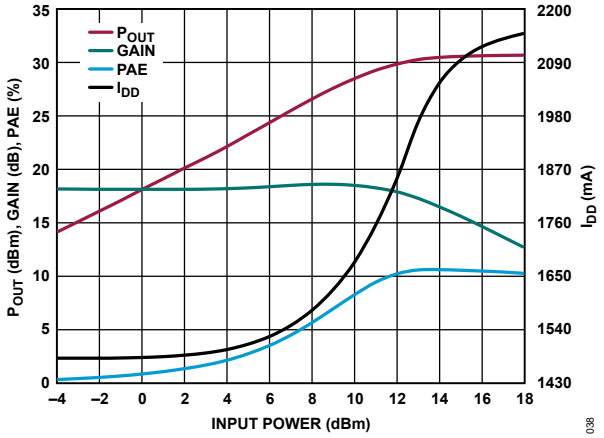

Figure 38. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 40 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

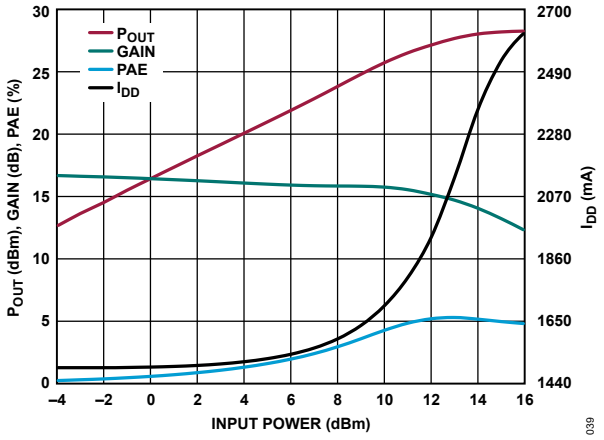

Figure 39. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 50 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

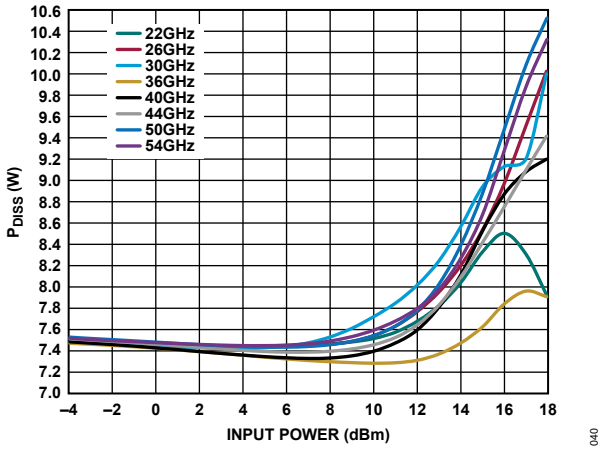

Figure 40. P_{DISS} vs. Input Power for Various Frequencies at T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 1500 mA

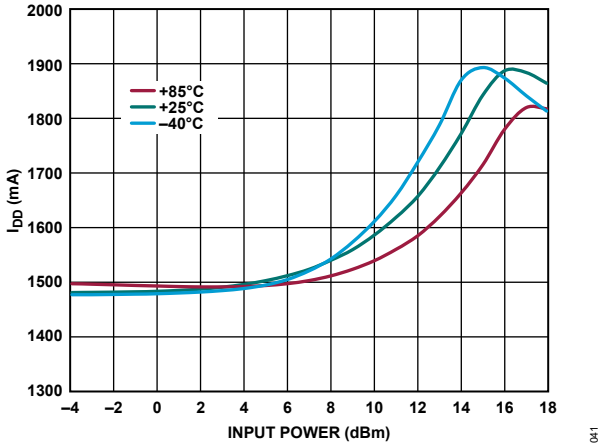

Figure 41. I_{DD} vs. Input Power at Various Temperatures, 36 GHz, V_{DD} = 5 V, I_{DQ} = 1500 mA

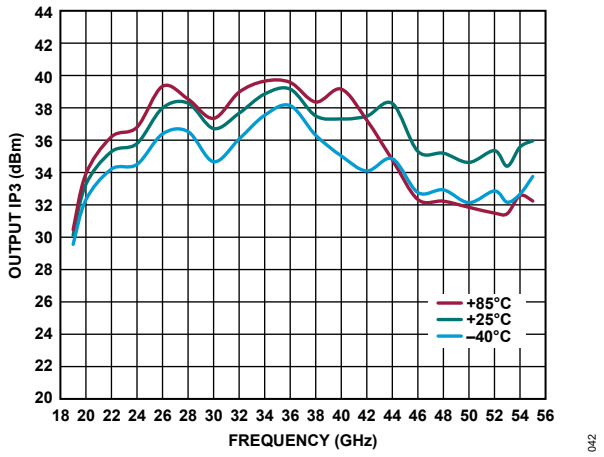

Figure 42. Output IP3 vs. Frequency at Various Temperatures, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 1500 mA

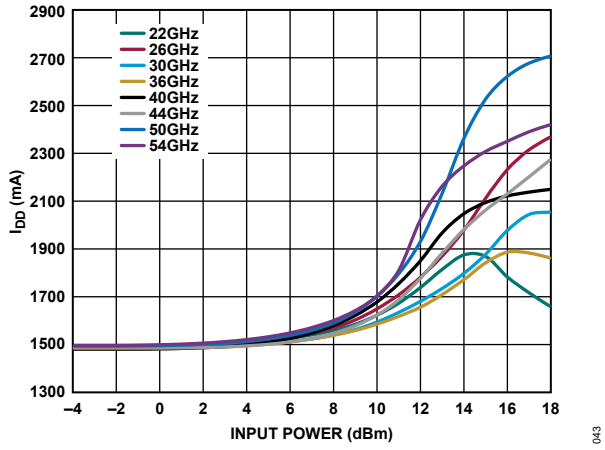

Figure 43. I_{DD} vs. Input Power at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 1500 mA

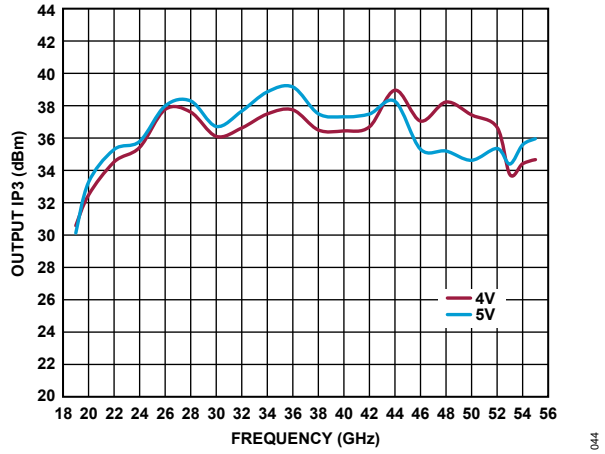

Figure 44. Output IP3 vs. Frequency for Various Supply Voltages, P_{OUT} per Tone = 14 dBm, I_{DQ} = 1500 mA

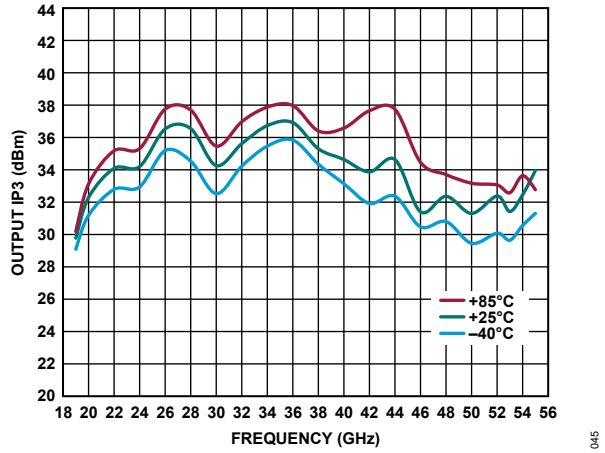

Figure 45. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 1700 mA

TYPICAL PERFORMANCE CHARACTERISTICS

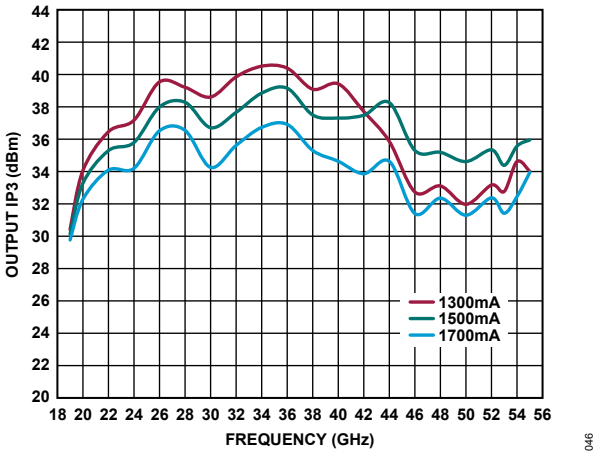

Figure 46. Output IP3 vs. Frequency for Various Supply Currents, P_{OUT} per Tone, V_{DD} = 5 V, I_{DQ} = 1500 mA

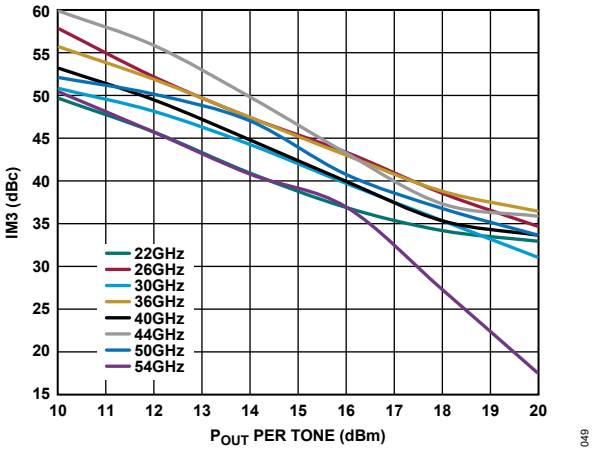

Figure 49. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 4 V, I_{DQ} = 1500 mA

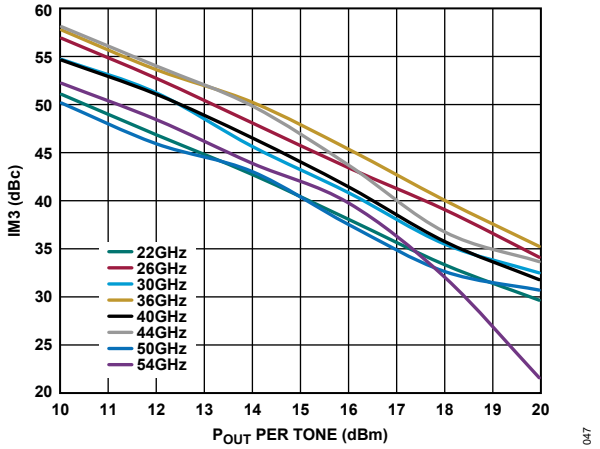

Figure 47. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, I_{DQ} = 1500 mA

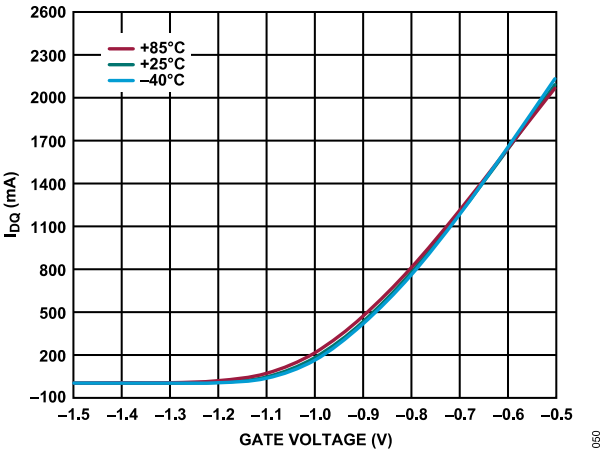

Figure 50. I_{DQ} vs. Gate Voltage for Various Temperatures, V_{DD} = 5 V

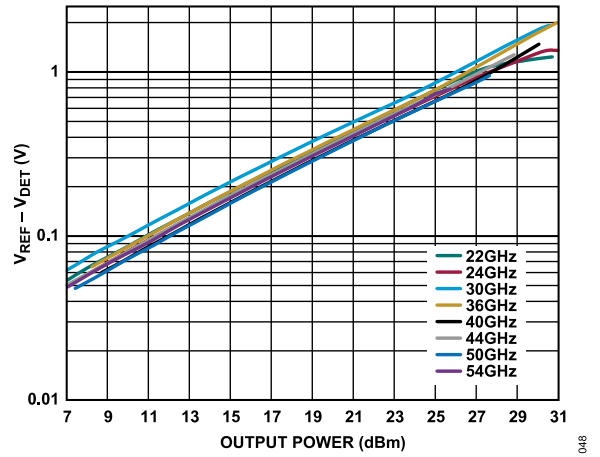

Figure 48. Detector Voltage (V_{REF} – V_{DET}) vs. Output Power for Various Frequencies

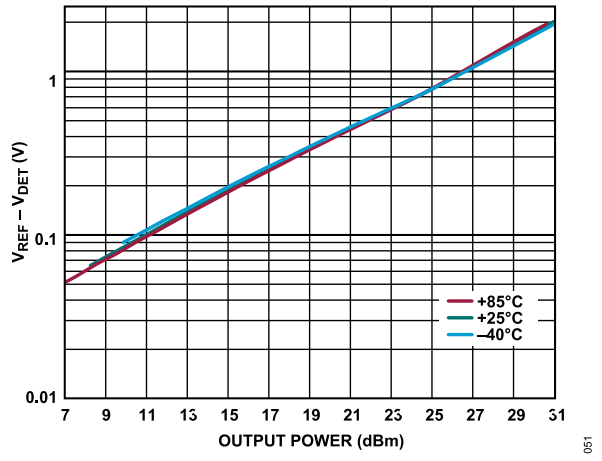

Figure 51. Detector Voltage (V_{REF} – V_{DET}) vs. Output Power for Various Temperatures at 36 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

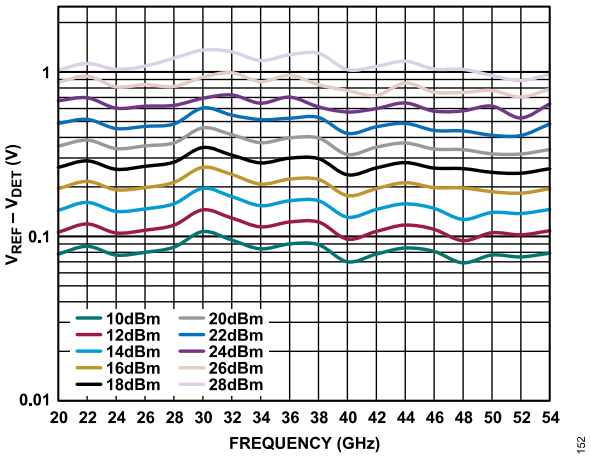

Figure 52. Detector Voltage (V_{REF} − V_{DET}) vs. Frequency for Various Output Powers

TYPICAL PERFORMANCE CHARACTERISTICS

LOWER BIAS OPERATION

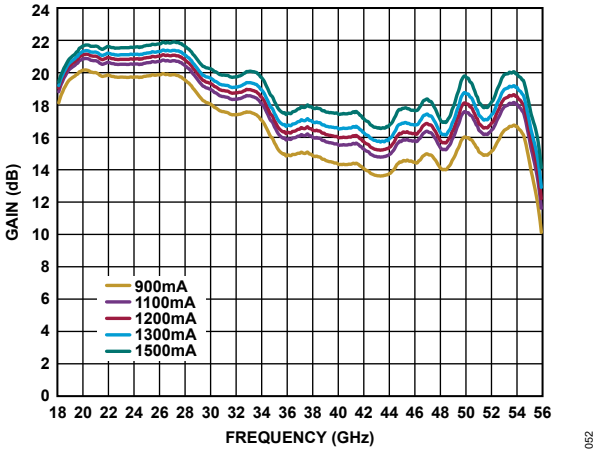

Figure 53. Gain vs. Frequency for Various Supply Currents, V_{DD} = 3 V

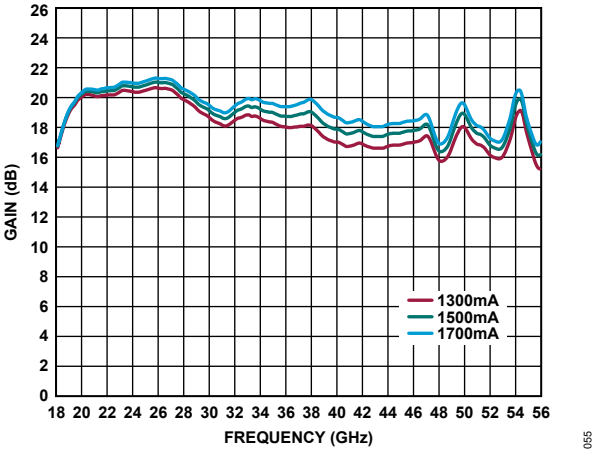

Figure 56. Gain vs. Frequency for Various Supply Currents, V_{DD} = 4 V

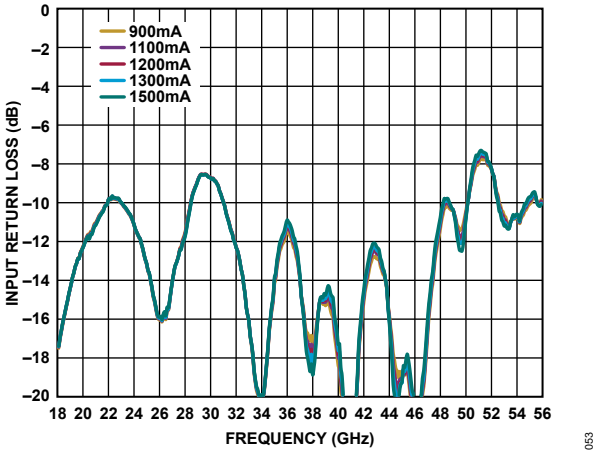

Figure 54. Input Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 3 V

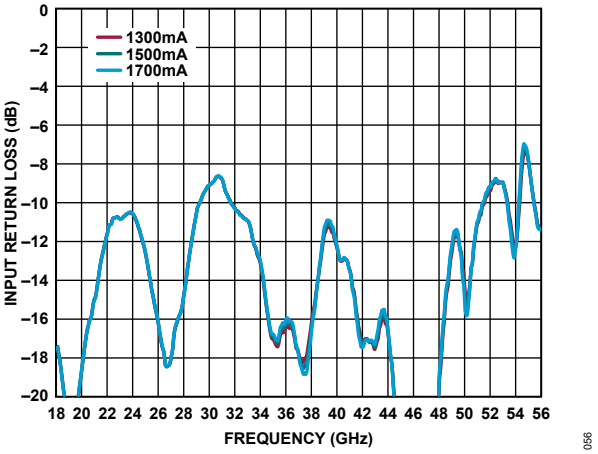

Figure 57. Input Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 4 V

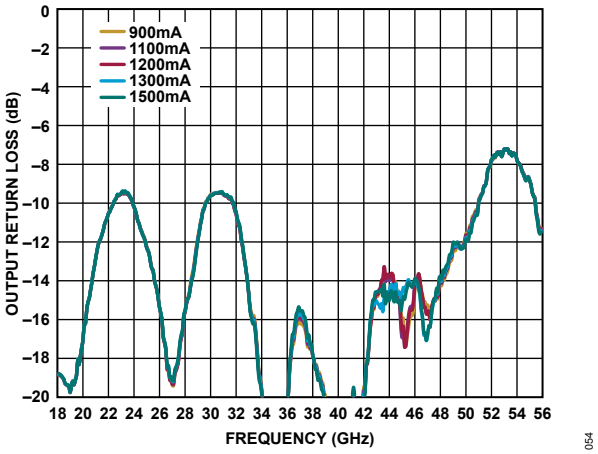

Figure 55. Output Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 3 V

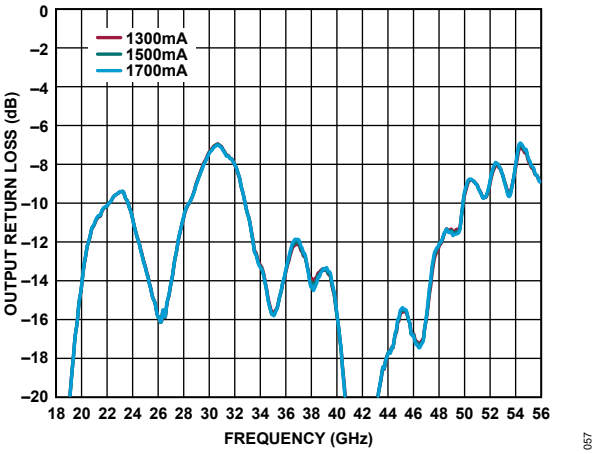

Figure 58. Output Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 4 V

TYPICAL PERFORMANCE CHARACTERISTICS

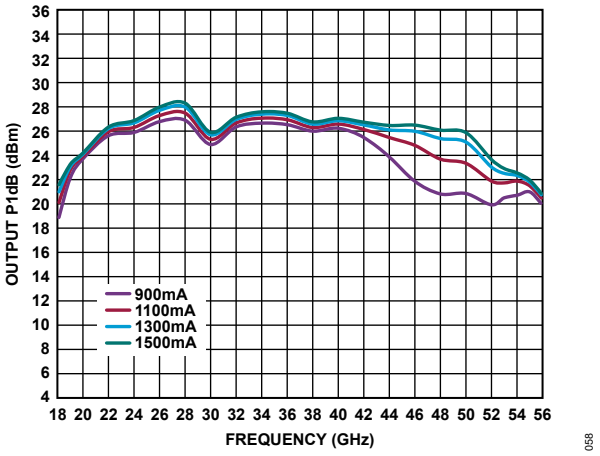

Figure 59. Output P1dB vs. Frequency for Various Supply Currents, V_{DD} = 3 V

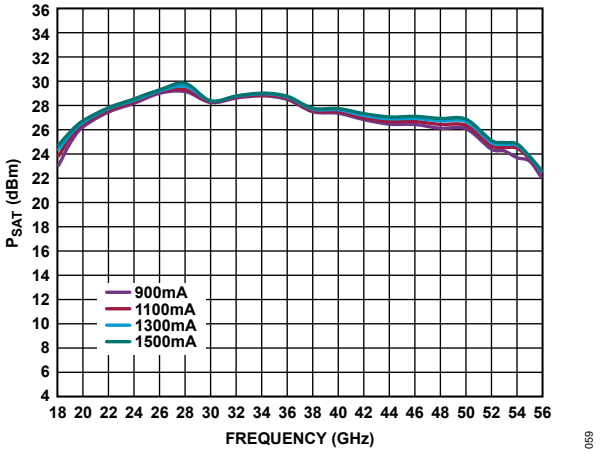

Figure 60. P_{SAT} vs. Frequency for Various Supply Currents, V_{DD} = 3 V

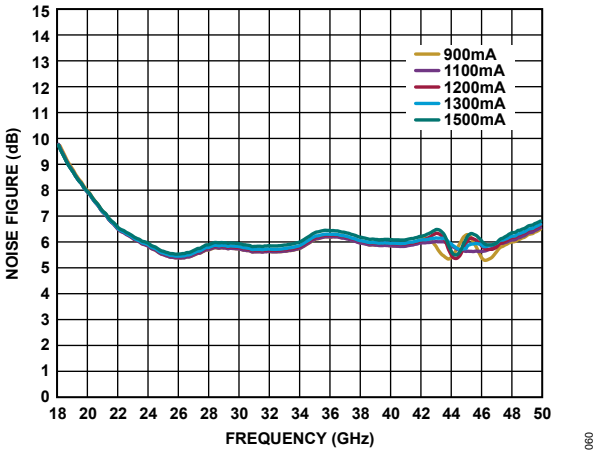

Figure 61. Noise Figure vs. Frequency for Various Supply Currents, V_{DD} = 3 V

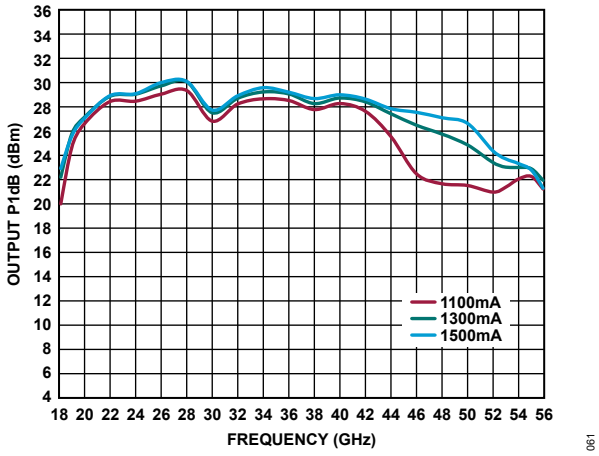

Figure 62. Output P1dB vs. Frequency for Various Supply Currents, V_{DD} = 4 V

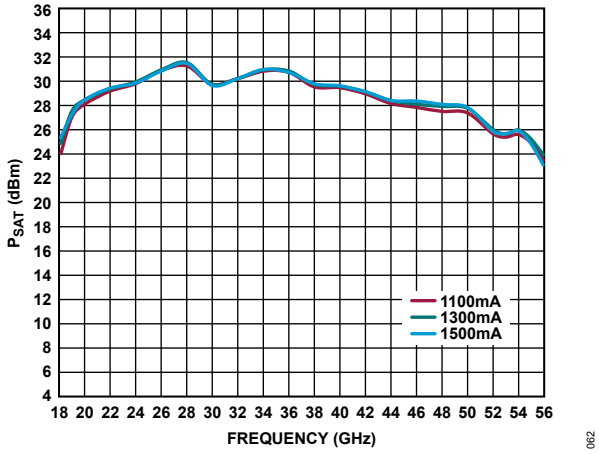

Figure 63. P_{SAT} vs. Frequency for Various Supply Currents, V_{DD} = 4 V

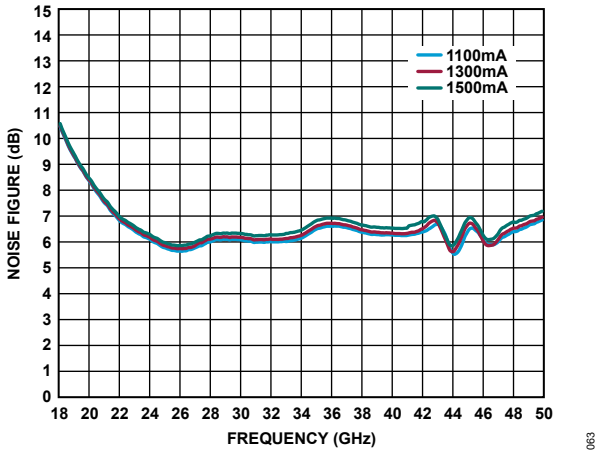

Figure 64. Noise Figure vs. Frequency for Various Supply Currents, V_{DD} = 4 V

TYPICAL PERFORMANCE CHARACTERISTICS

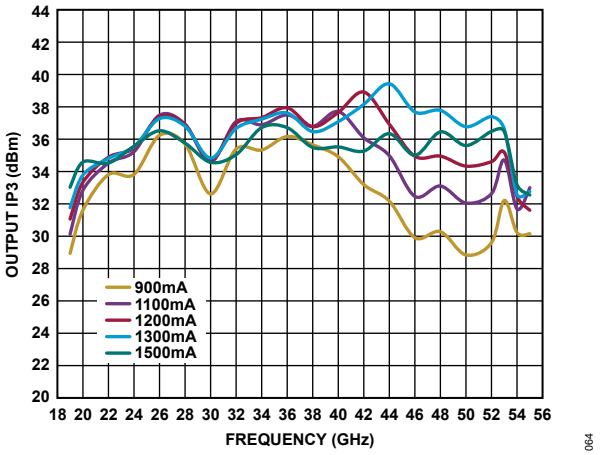

Figure 65. Output IP3 vs. Frequency for Various Supply Currents, P_{OUT} per Tone = 14 dBm, V_{DD} = 3 V

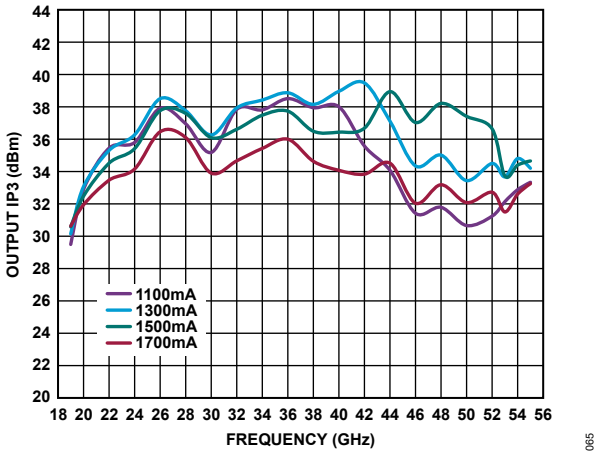

Figure 66. Output IP3 vs. Frequency for Various Supply Currents, P_{OUT} per Tone = 14 dBm, V_{DD} = 4 V

THEORY OF OPERATION

The architecture of the ADPA7008, a medium power amplifier, is shown in Figure 67. The ADPA7008 uses two cascaded, four-stage amplifiers operating in quadrature between six 90° hybrids.

The input signal is divided evenly into two, and then each signal is divided into two again. Each of these new paths are amplified through four independent gain stages. The amplified signals are then combined at the output. This balanced amplifier approach forms an amplifier with a combined gain of 17.5 dB and a P_{SAT} value of 31 dBm.

The quadrature hybrid couplers ensure good broadband input and output return loss matching across the full 20 GHz to 54 GHz frequency range of the ADPA7008. See the application circuits shown in Figure 68 and Figure 69 for further details on biasing the various blocks.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF P_{OUT}. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output (see Figure 67).

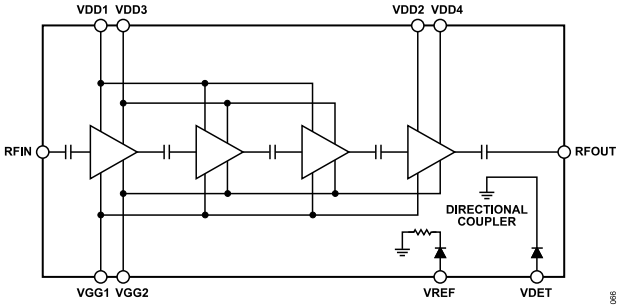

Figure 67. ADPA7008 Architecture

APPLICATIONS INFORMATION

Figure 68 shows the basic connections for operation when the gate voltage is applied on the north side of the device to Pin 4 (VGG1). Figure 69 shows the basic connections for operation when the gate voltage is applied on the south side to Pin 10 (VGG2). While the gate voltage bias signal can be applied to either VGG1 or to VGG2 (the unused pin is left open), the drain supply must be applied to all VDDx pins. The power supply decoupling scheme shown can be simplified by combining the larger capacitance values. For example, C13 and C14 can be combined into a single 4.7 µF capacitor (C18 and C29 can be combined in the same manner). Each VDDx pin must have at least one dedicated 100 pF capacitor.

All measurements for this device were taken using the application circuit (see Figure 68).

The recommended power-up bias sequence is as follows:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, V_{GG1} or V_{GG2}, to −1.5 V.
3. Set all drain bias voltages, V_{DDx}, to 5 V.
4. Increase the gate bias voltages, V_{GG1} or V_{GG2}, to achieve an I_{DQ} of 1500 mA.
5. Apply the RF signal.

The recommended power-down bias sequence is as follows:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, V_{GG1} or V_{GG2}, to −1.5 V to achieve an I_{DQ} = 0 mA (approximately).
3. Decrease all the drain bias voltages, V_{DDx}, to 0 V.
4. Increase the gate bias voltages, V_{GG1} or V_{GG2}, to 0 V.

The V_{DD} = 5 V and I_{DQ} = 1500 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions and basic connections schematic with north side gate biasing (see Figure 68). See Figure 69 for the application circuit for the south side gating biasing configuration.

Operation of the ADPA7008 at different bias conditions provides performance that differs from what is shown in Table 1, Table 2, Table 3, and Table 4. Biasing the ADPA7008 for higher drain current typically results in higher P1dB and gain at the expense of increased power consumption (see Table 9). Data was taken for Table 9 at the following nominal bias conditions: V_{DD} = 5 V, T_A = 25°C, and frequency = 36 GHz.

Table 9. Power Selection Table

I_{DQ} (mA)	Gain (dB)	P1dB (dBm)	Output IP3 (dBm)	P_{DISS} (W) at P_{SAT}	V_{GGx} (V)[1]
1300	17.7	30.1	40.4	7.7	−0.68
1500	18.4	30.3	39.2	7.9	−0.63
1700	18.8	30.6	36.9	8.0	−0.59

[1] Adjust V_{GG1} from −1.5 V to 0.4 V to achieve the desired drain current.

TYPICAL APPLICATION CIRCUITS

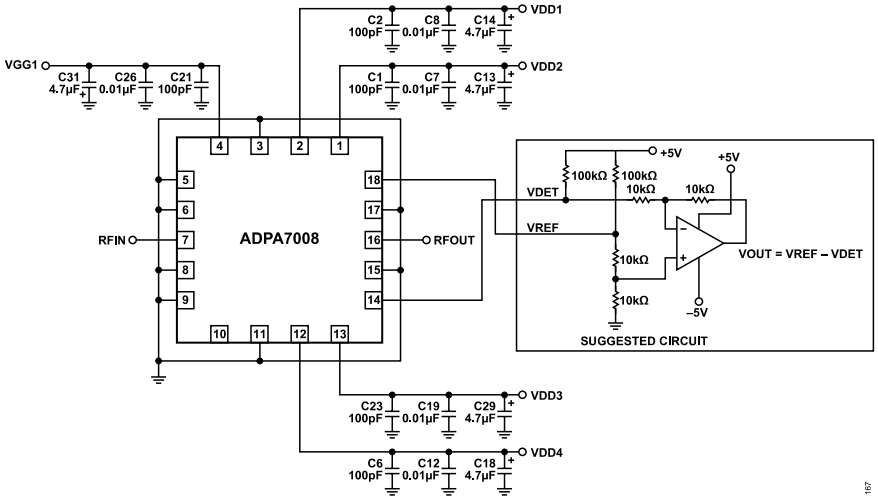

Figure 68. Basic Connections for Operation with the North Side Gate Voltage Biasing

APPLICATIONS INFORMATION

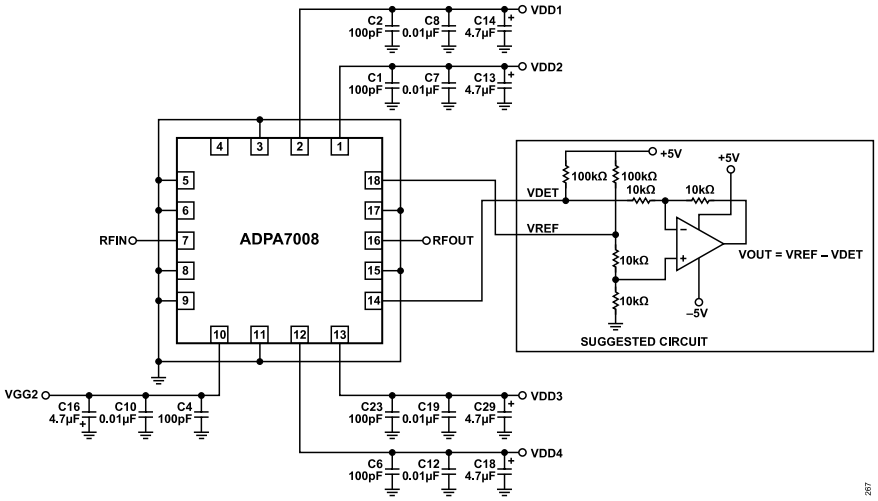

Figure 69. Basic Connections for Operation with the South Side Gate Voltage Biasing

BIASING THE ADPA7008 WITH THE LOW NOISE LTM8063

The LTM8063 is a Silent Switcher voltage regulator that meets the bias requirement for the positive drain supply of the ADPA7008. The regulator provides a drain bias voltage that is constant over load current variations. Figure 70 shows a circuit that derives the 5 V V_{DD} supply voltage from an input rail that can vary from 6.5 V to 40 V (which is the V_{IN} range of the LTM8063). The LTC8063 is configured using external components to generate a 5 V V_{DD} supply capable of up to 2 A. Figure 71 shows a plot of the measured noise figure vs. frequency of this circuit with a comparison to that measured with a bench supply, for reference.

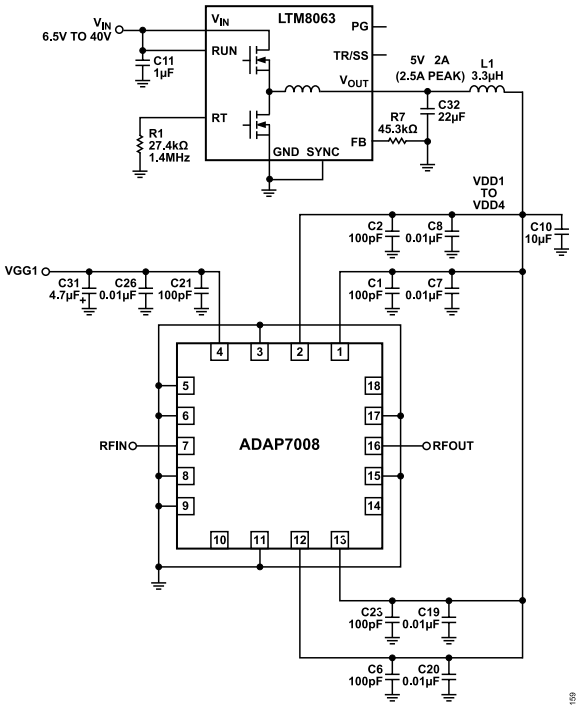

Figure 70. Application Circuit Using the LTM8063 for Low Noise Drain Voltage Generation for the ADPA7008

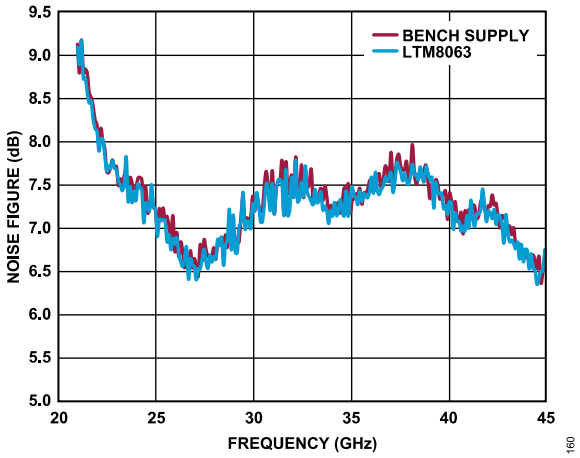

Figure 71. ADPA7008 Noise Figure vs. Frequency Measured for VDD Using the LTM8063 vs. a Bench Supply for Reference

A low current (<<1 mA) negative V_{GG} is also required to provide the constant V_{GG} bias voltage. For this, the ADP5600 is recommended.

As previously noted, the ADPA7008 V_{DD} and V_{GG} voltages must be correctly sequenced during power-on and power-off.

Figure 72 shows a complete circuit that includes positive drain voltage generation, negative gate voltage generation, and the power-on and power-off sequencing. This circuit supports an external input voltage (V_{IN}) range of 12 V to 16 V.

BIASING THE ADPA7008 WITH THE LOW NOISE LTM8063

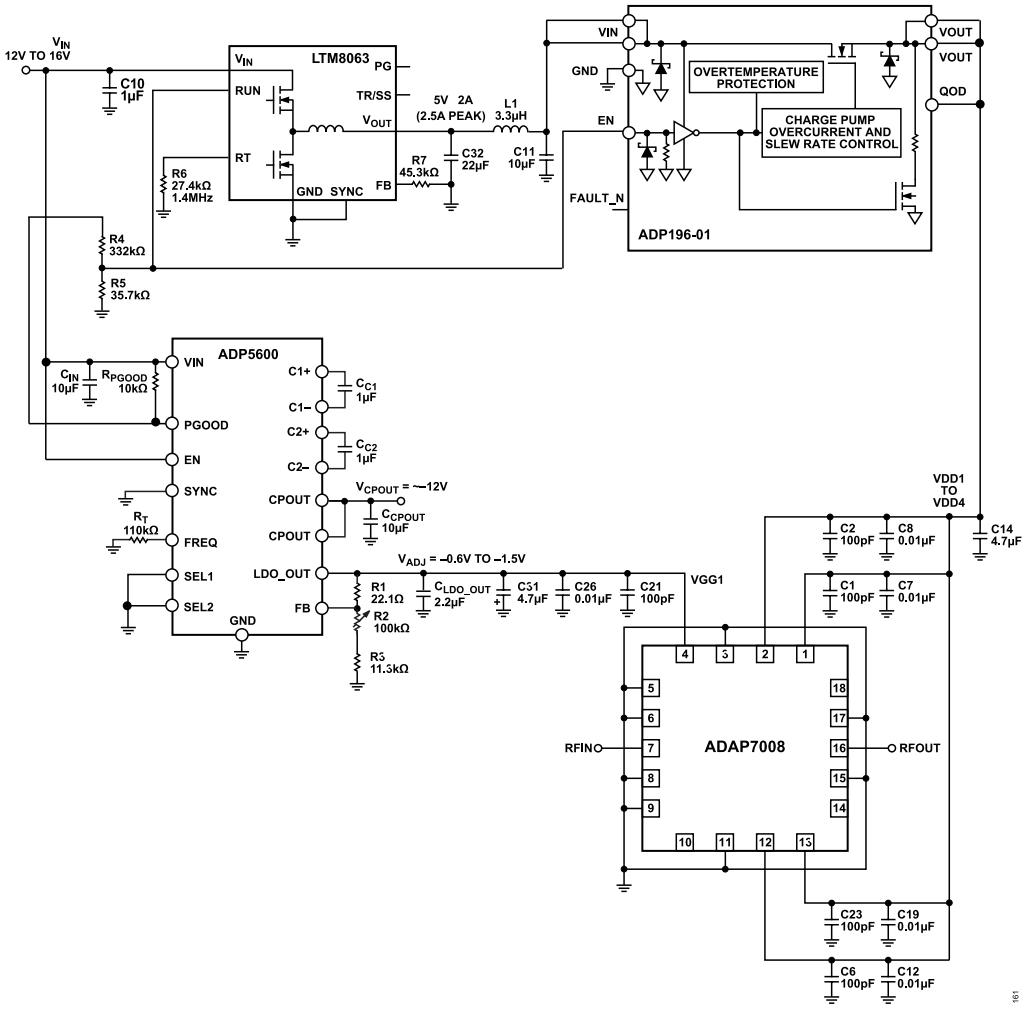

Figure 72. A Complete Gate and Drain Voltage Biasing Circuit for the ADPA7008

As shown in Figure 72, the drain voltage is generated by the LTM8063. The negative gate voltage is generated by the ADP5600. The exact gate voltage is set by a resistor divider between the LDO_OUT and FB pins on the ADP5600. The equation for setting the gate voltage is VGG1 = −0.5(1 + R1/(R2 + R3)), where R2 is a potentiometer. To achieve a drain voltage of 1500 mA, the recommended value for VGG1 is −0.63 V. To set this voltage, R1 and R3 were set to 22.1 kΩ and 11.3 kΩ, respectively, and the R2 potentiometer was set to 100 kΩ, which allows VGG1 to swing from approximately −1.5 V to −0.6 V. To ensure that the gate voltage is active before the drain voltage, the PGOOD signal from the ADP5600 is used to gate all devices in the drain voltage generation path. The ADP5600 PGOOD output signal is scaled using a resistor divider such that the LTM8063 drain voltage generator turns on after the ADP5600 output does. Figure 73 shows the turn on sequence and turn off sequence. Notice how V_{DD} turns on a few milliseconds after V_{GG}. This sequencing is controlled by the scaled PGOOD signal.

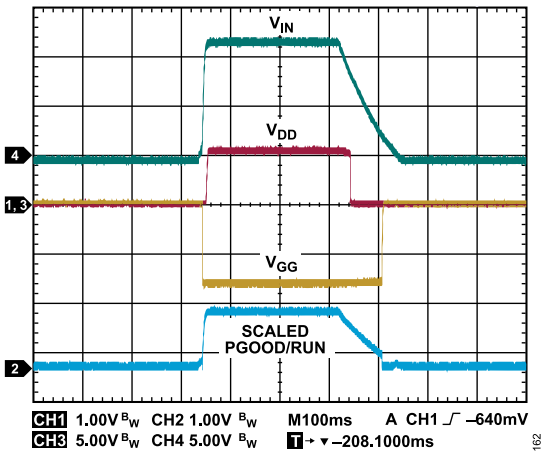

Figure 73. Turn On Sequence and Turn Off Sequence

BIASING THE ADPA7008 WITH THE LOW NOISE LTM8063

To ensure clean circuit turn off when V_{IN} (Figure 73) turns off, the ADP196-01 load switch with quick output discharge has been added to the drain voltage generation path. The ADP196-01 ensures that V_{DD} turns off fully when V_{IN} is around 8.5 V before V_{GG} turns off when V_{IN} is at 2.54 V. The ADP196-01 has a very small package (1 mm × 1.5 mm WLCSP) and requires no external components, resulting in a minimal increase in PCB area.

BIASING ADPA7008 WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirements for enhancement mode and depletion mode amplifiers such as the ADPA7008. The controller provides constant drain current biasing over temperature and device to device variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self protection in the event of a short circuit, an internal charge pump that generates the negative voltage needed on the gate of the ADPA7008, and the option to use an external negative voltage source.

The HMC980LP4E is also available in die form as the HMC980-Die.

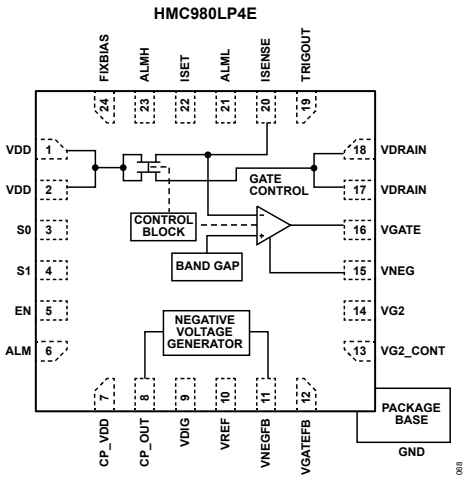

Figure 74. Functional Diagram of HMC980LP4E

APPLICATION CIRCUIT SETUP

Figure 75 is the schematic of an application circuit using the HMC980LP4E to control the ADPA7008. When using an external negative supply for VNEG, refer to the schematic in Figure 76.

In the application circuit shown in Figure 75, the ADPA7008 drain voltage, V_{DRAIN}, and drain current, I_{DRAIN}, are set by the following equations:

$$V_{DD} = V_{DRAIN} + (I_{DRAIN} \times 0.7\ \Omega) \quad (1)$$

V_{DD} = 5 V + (1.6 A × 0.7 Ω) = 6.12 V

where:

V_{DD} and V_{DRAIN} are in volts.

I_{DRAIN} is in amperes.

$$R10 = (150\Omega \times A) \div (I_{DRAIN}) \quad (2)$$

R10 = (150 Ω × A) ÷ (1.6 A) = 94 Ω

where:

R10 is in ohms.

I_{DRAIN} is in amperes.

LIMITING VGATE FOR THE ADPA7008 VGGX ABSOLUTE MAXIMUM RATING REQUIREMENT

When using the HMC980LP4E to control the ADPA7008, the minimum voltages for VNEG and VGATE must be −1.5 V to keep the voltages within the absolute maximum rating limit for the VGGx pin of the ADPA7008. To set the minimum voltages, set R15 and R16 to the values shown in Figure 75 and Figure 76. Refer to the AN-1363 for more information and calculations for R15 and R16.

The HMC980LP4E application circuits for biasing figures in the AN-1363 are two examples of how the HMC980LP4E is used as an active bias controller. Both application circuits within the AN-1363 show the R5 and R7 resistors, which are analogous to the R15 and R16 resistor shown in Figure 75 and Figure 76.

BIASING ADPA7008 WITH THE HMC980LP4E

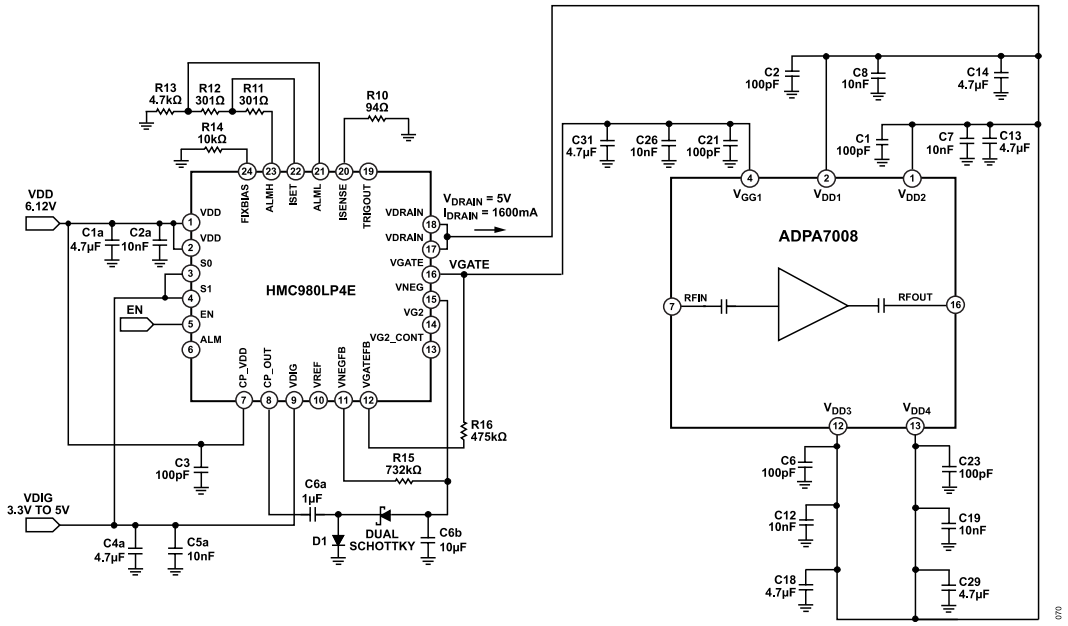

Figure 75. Application Circuit Using HMC980LP4E with ADPA7008 (Internal Negative Voltage Source)

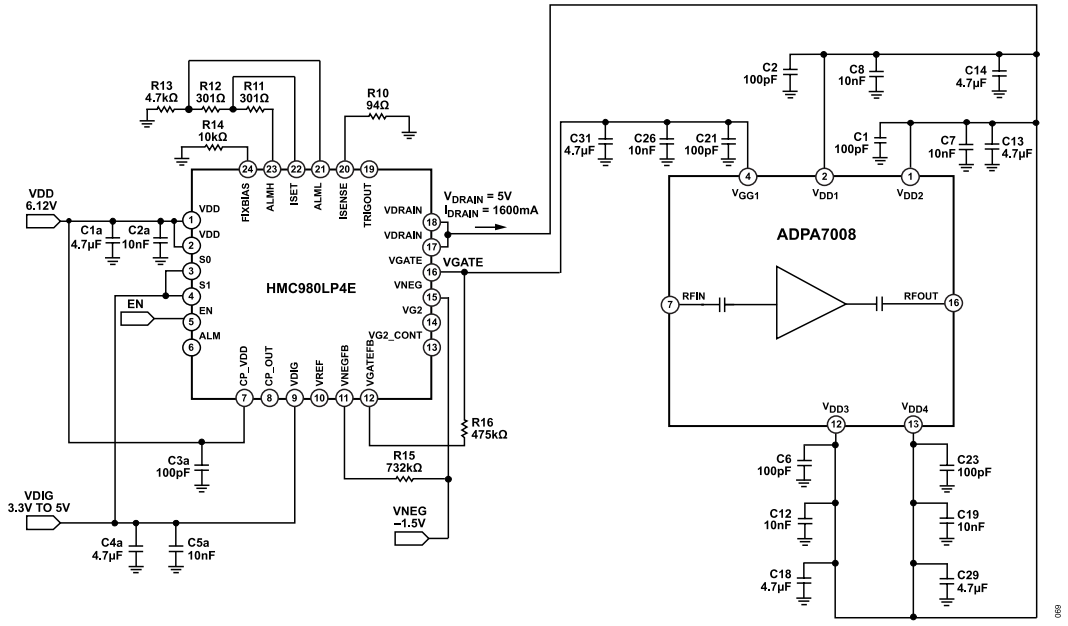

Figure 76. Application Circuit Using HMC980LP4E with ADPA7008 (External Negative Voltage Source)

HMC980LP4E BIAS SEQUENCE

When using the HMC980LP4E to control the ADPA7008, the dc supply sequences described in the Power-Up Sequence section and the Power-Down Sequence section are recommended to prevent damage to the HMC980LP4E and the ADPA7008.

Power-Up Sequence

The power-up sequence for the HMC980LP4E is as follows:

1. Set EN = 0 V to ensure that the HMC980LP4E powers up without turning on the VGATE and VDRAIN pins.
2. Set VDIG = 3.3 V.
3. Set S0 and S1 = 3.3 V. The Sx pins are internally pulled up to VDIG; therefore, this step is optional
4. Set V_{DD} = 6.12 V.
5. Set VNEG = −1.5 V. Note that this step is unnecessary if using the internally generated negative voltage.
6. Set EN = 3.3 V, which turns on the VGATE and VDRAIN pins.

BIASING ADPA7008 WITH THE HMC980LP4E

Power-Down Sequence

The power-down sequence for the HMC980LP4E is as follows:

1. Set EN = 0 V, which causes the HMC980LP4E to power-down the VDRAIN pins and sets the VGATE = −1.5 V.
2. Set VNEG = 0 V. Note that this step is unnecessary if using the internally generated negative voltage.
3. Set VDD = 0 V.
4. Set S0 and S1 = 0 V. The Sx pins are internally pulled up to VDIG; therefore, this step is optional.
5. Set VDIG = 0 V.

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7008 on or off by applying 3.3 V or 0 V, respectively, to the EN pin. When setting EN = 3.3 V, VGATE becomes less negative as the control loop closes, and VDRAIN turns on at 5 V. VGATE then stabilizes at the voltage required to achieve I_{DRAIN} = 1600 mA, and the closed control loop then continues to regulate I_{DRAIN} at 1600 mA. When setting EN = 0 V, VGATE is set to −1.5 V, and VDRAIN is set to 0 V.

CONSTANT DRAIN CURRENT BIASING VS. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses closed-loop feedback to continuously adjust VGATE to maintain a constant drain current bias over dc supply variation, temperature, and device to device variation. In addition, constant drain current bias is the optimum method for reducing time in calibration procedures and for maintaining consistent performance over time. By comparing the constant drain current bias with a constant gate voltage bias where the current is driven to increase when RF power is applied, a slightly lower output P1dB is seen with a constant drain current bias. This output P1dB is shown in Figure 84, where the RF performance is slightly lower than the constant gate voltage bias operation due to a lower drain current at the high input powers as the device reaches 1 dB compression.

To increase the output P1dB performance for the constant drain current bias toward the constant gate voltage bias performance, increase the set current toward the I_{DD} value this performance reaches under the RF drive in the constant gate voltage bias condition, as shown in Figure 84. The limit of increasing I_{DQ} under the constant drain current operation is set by the thermal limitations found in Table 5 with the maximum power dissipation specification. As I_{DD} increase continues, the actual output P1dB does not continue to increase indefinitely, and the power dissipation increases. Therefore, when using constant drain current biasing, note this exchange between power dissipation and the output P1dB performance into consideration.

CONSTANT I_{DD} OPERATION

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 1700 mA for nominal operation, unless otherwise noted. Figure 77 to Figure 80 are biased with the HMC980LP4E active bias controller. See the Biasing ADPA7008 with the HMC980LP4E section for biasing details.

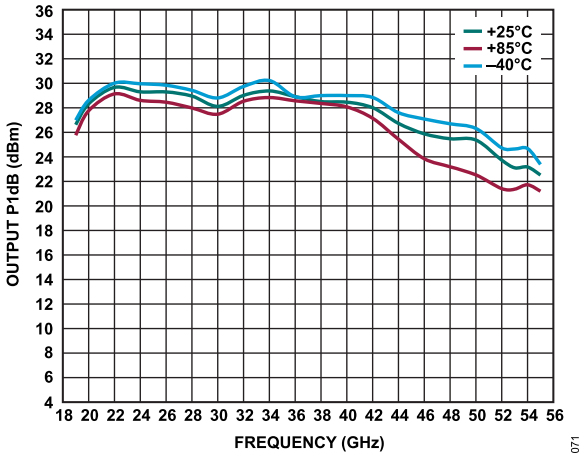

Figure 77. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

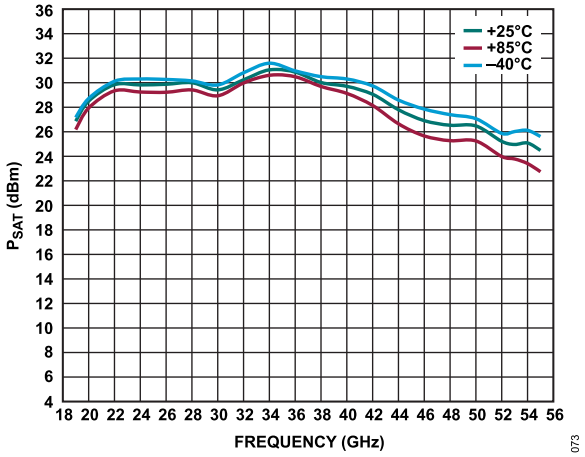

Figure 78. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

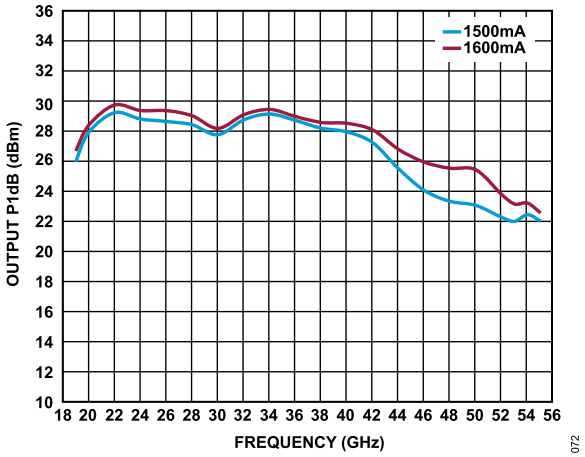

Figure 79. Output P1dB vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

BIASING ADPA7008 WITH THE HMC980LP4E

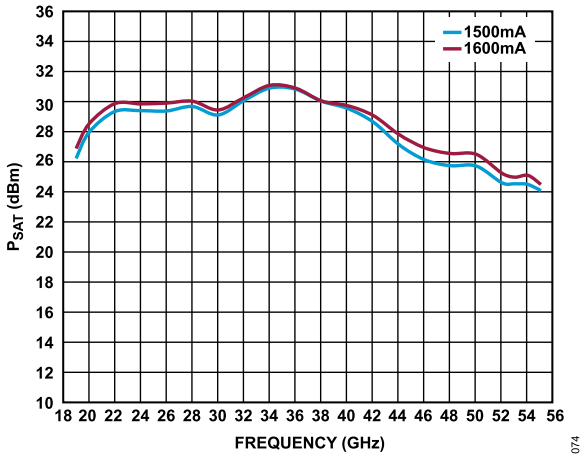

Figure 80. P_{SAT} vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

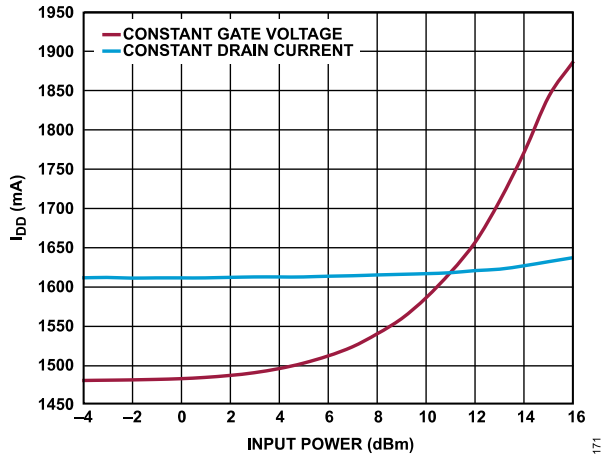

Figure 81. I_{DD} vs. Input Power, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1600 mA) and Constant Gate Voltage Bias (V_{GG} = −0.63 V)

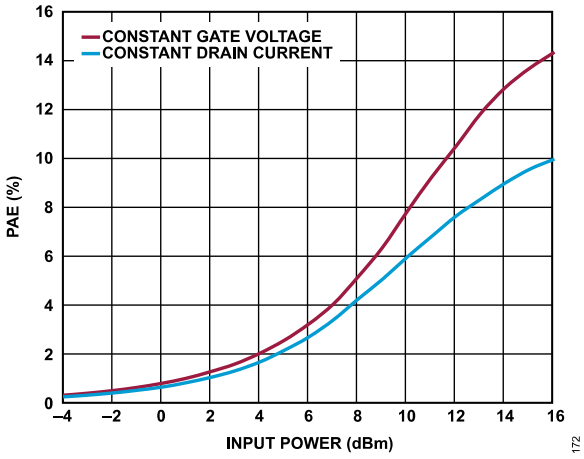

Figure 82. PAE vs. Input Power, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1600 mA) and Constant Gate Voltage Bias (V_{GG} = −0.63 V)

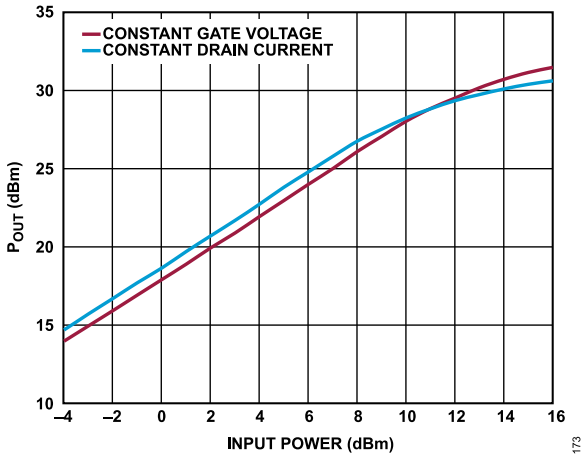

Figure 83. P_{OUT} vs. Input Power, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1600 mA) and Constant Gate Voltage Bias (V_{GG} = −0.63 V)

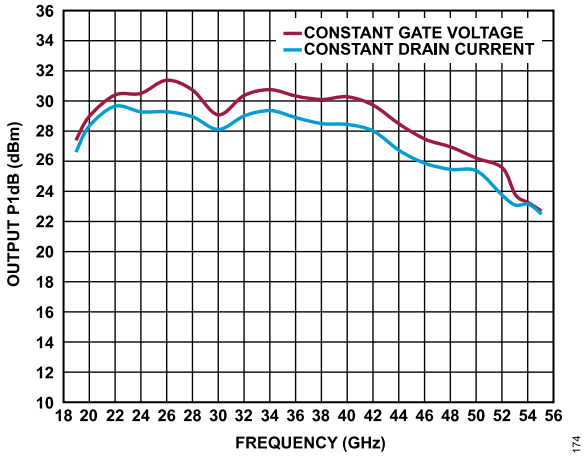

Figure 84. Output P1dB vs. Frequency, V_{DD} = 5 V, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1600 mA) and Constant Gate Voltage Bias (V_{GG} = −0.63 V)

OUTLINE DIMENSIONS

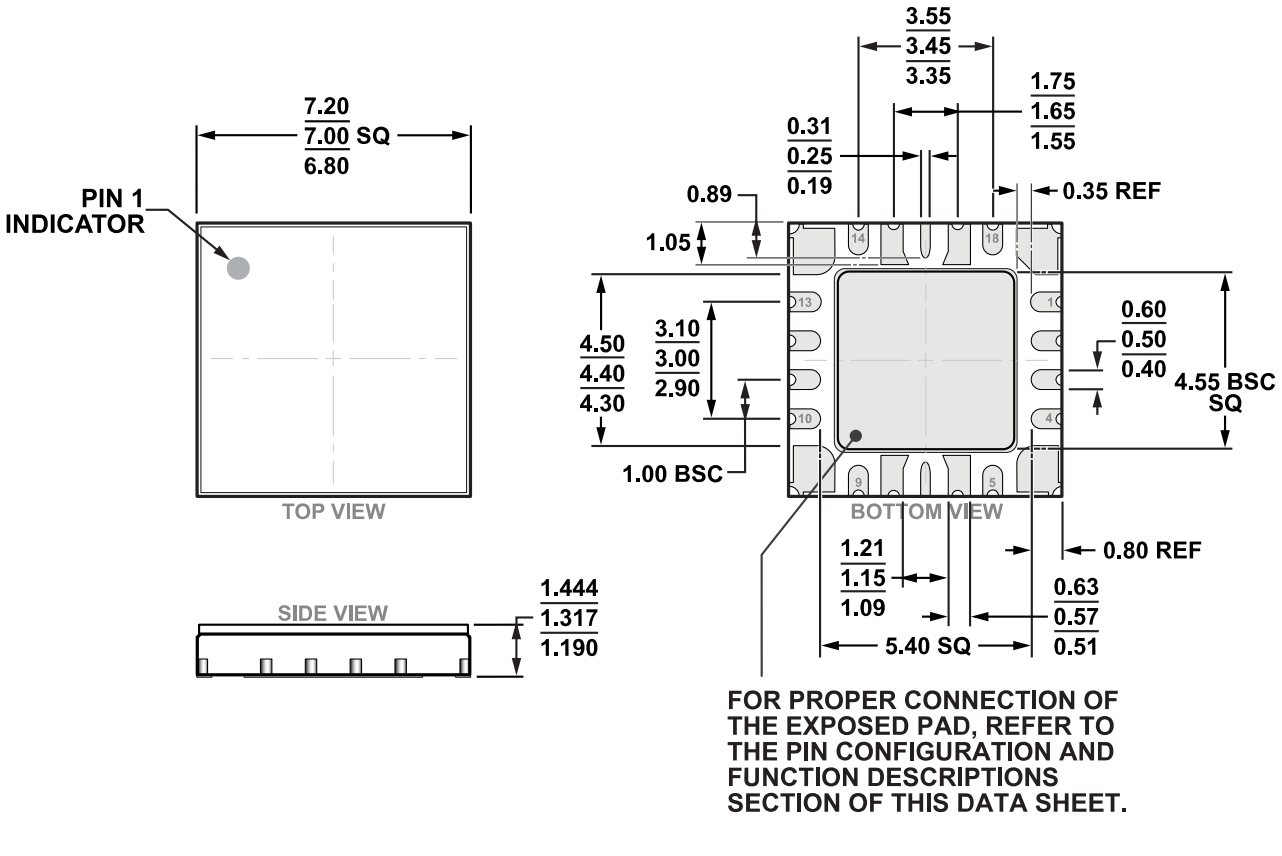

Figure 85. 18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HC]
(EH-18-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADPA7008AEHZ	−40°C to +85°C	18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-18-1
ADPA7008AEHZ-R7	−40°C to +85°C	18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-18-1

[1] Z = RoHS Compliant Part.

[2] For the ADPA7008AEHZ and the ADPA7008AEHZ-R7, the MSL Rating is MSL3.

EVALUATION BOARDS

Model[1]	Description
ADPA7008-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.