RFB18N10CS/ CSVM/CSHM

Current Sensing N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 18A, 100V
- $r_{DS(ON)}$ 0.1Ω
- Built-In Current Sensing Ratio ..... 1560 ± 2.5%
- UIS SOA Rating Curve (Single Pulse)
- -55°C to +175°C Operating and Storage Temperature

Description

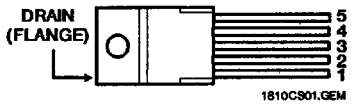
The RFB18N10CS, RFB18N10CSVM, RFB18N10CSHM are n-channel enhancement-mode silicon-gate power field-effect transistors which have a built-in current sensing function. The current sense lead provides an accurate fraction of the drain current that can be used as a feedback signal for control and/or protection. These devices can be repeatedly and economically produced on the standard PowerMOS production line.

The RFB-series are supplied in various lead configurations of the TS-001 (5 lead) case style plastic package.

Because of space limitations, branding (marking) on types RFB18N10CS, RFB18N10CSVM and RFB18N10CSHM is F18N10CS.

Package

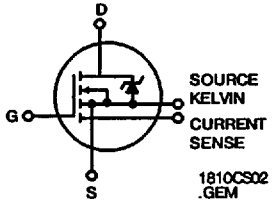
TS-001 (5 LEAD)
TOP VIEW



TERMINAL CONNECTIONS
1 - Gate
2 - Current Sense
3 - Drain
4 - Source Kelvin
5 - Source

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	RFB18N10CS RFB18N10CSVM RFB18N10CSHM	UNITS
Drain-Source Voltage ..... V_{DSS}	100	V
Drain-Gate Voltage ..... V_{DGR}	100	V
Gate-Source Voltage ..... V_{GS}	±20V	V
Drain Current, Continuous ..... I_D	18	A
Drain Current, Pulsed ..... I_{DM}	56	A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve (Figure 10)		
Power Dissipation Total @ T_C = +25°C ..... P_D	79	W
Power Dissipation Derating T_C > +25°C	0.53	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2430.2

Specifications RFB18N10CS, RFB18N10CSVM, RFB18N10CSHM

T-39-90

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = +25°C, Unless Otherwise Specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	ID = 0.25 mA, VGS = 0V	100	-	V
Gate Threshold Voltage	VGS(th)	VGS = VDS, ID = 0.25 mA	2	4	V
Zero Gate Voltge Drain Current	IDSS	VGS = 0V VDS = 100V, Tc = 25°C VDS = 80V, Tc = 175°C	- -	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = ±20V, VDS = 0V	-	±500	nA
Static Drain-Source On Resistance	rDS(on)	ID = 9A, VGS = 10V	-	0.10	Ω
Forward Transconductance	gfs	ID = 9A, VDS = 15V	4.7	-	S(℧)
Current Sensing Ratio	r	ID= 14A, VGS = 10V	1480	1640	
Turn-On Delay Time	td(on)	VDS =50V	-	14	ns
Rise Time	tr	ID = 14A	-	63	ns
Turn-Off Delay Time	td(off)	VGS = 10V	-	33	ns
Fall Time	tr	Rgs = 12Ω	-	38	ns
Total Gate Charge	Qg (total)	ID = 14A, VDS = 80V VGS = 10V	-	20	nC
Thermal Resistance, Junction-to-Case	RθJC		-	1.9	°C/W
Thermal Resistance, Junction-to-Ambient	RθJA		-	75	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	VSD	ISD = 14A	-	1.5	V
Reverse Recovery Time	trr	ISD = 14A, dISD/dt = 100A/µs	-	310	ns

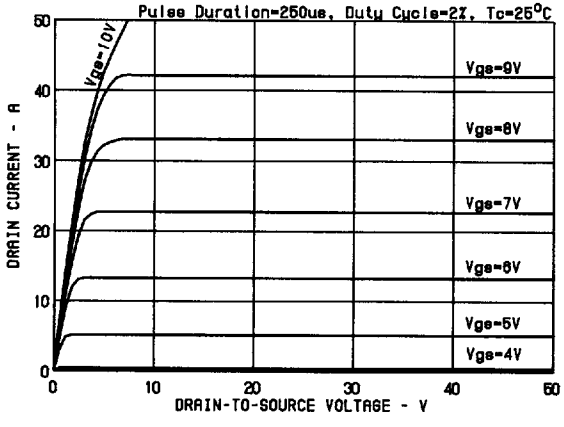


Figure 1 - Typical output characteristics.

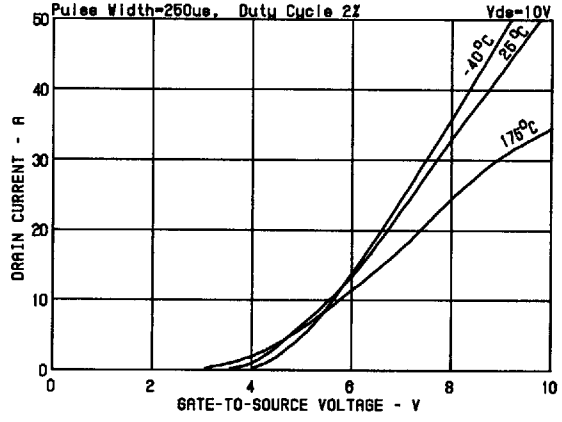


Figure 2 - Typical transfer characteristics.

INTELLIGENT DISCRETES

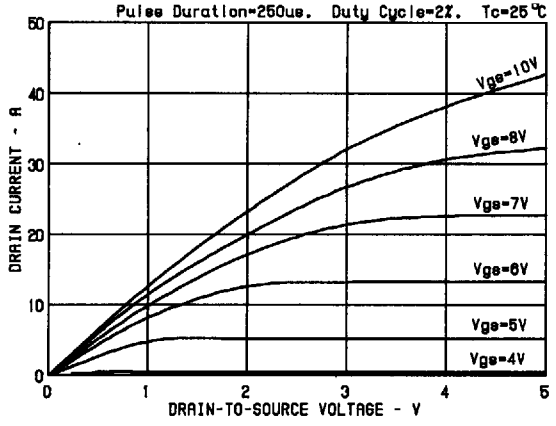


Figure 3 – Typical saturation characteristics.

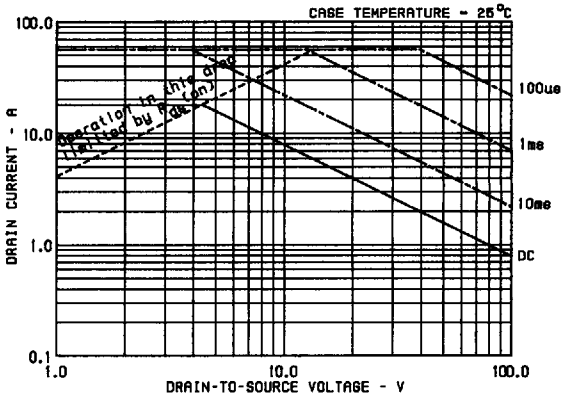


Figure 4 – Maximum safe operating area.
(Curves must be derated linearly with increase in case temperature.)

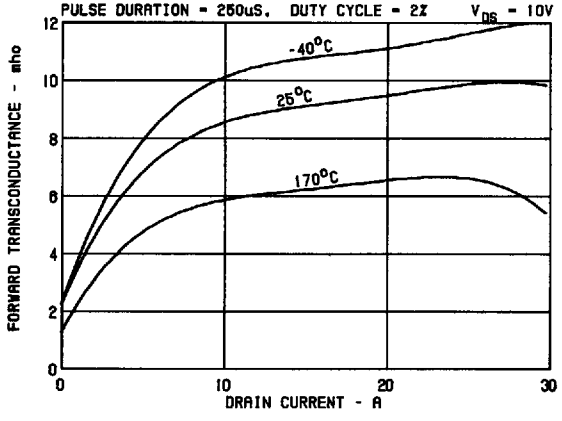


Figure 5 – Typical transconductance vs drain current.

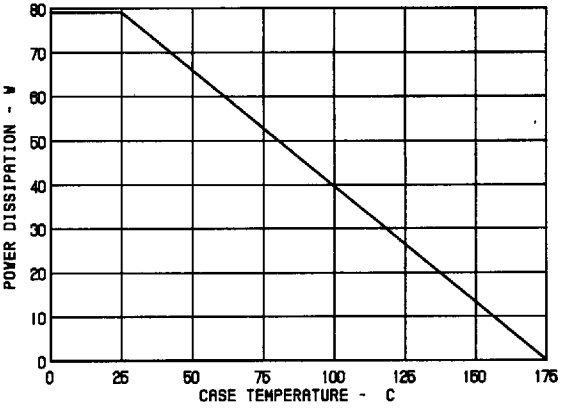


Figure 6 – Power dissipation vs case temperature derating curve.

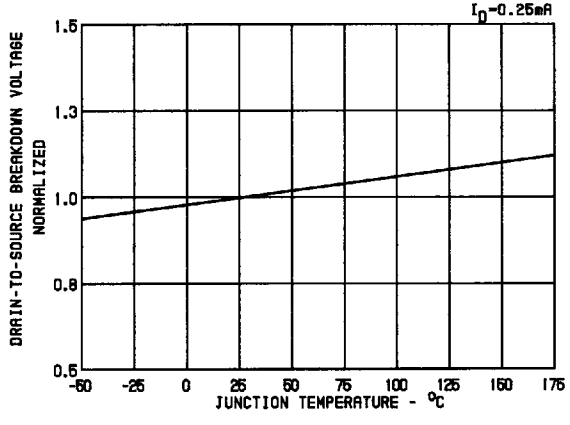


Figure 7 – Normalized breakdown voltage vs temperature.

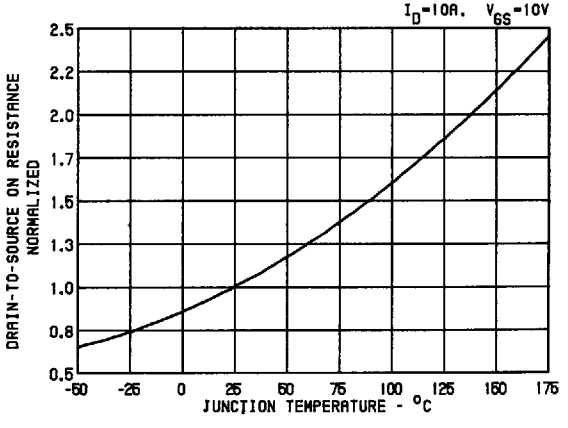


Figure 8 – Normalized on-resistance vs temperature.

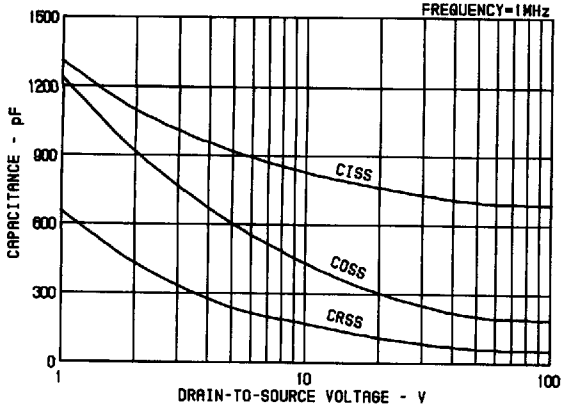


Figure 9 - Typical capacitance vs drain-to-source voltage.

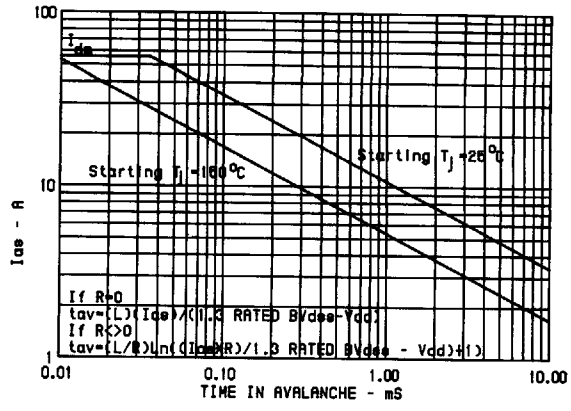


Figure 10 - Unclamped-Inductive switching safe operating area.

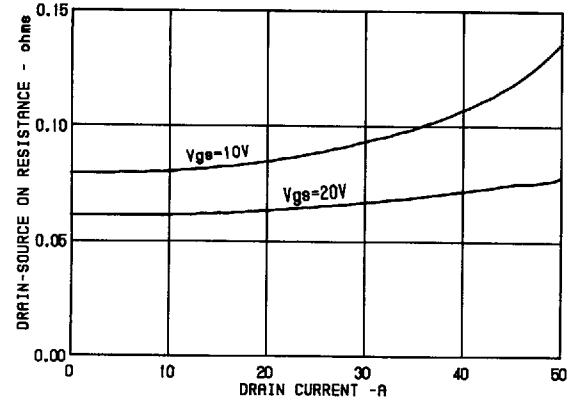


Figure 11 - Typical on-resistance vs drain current.

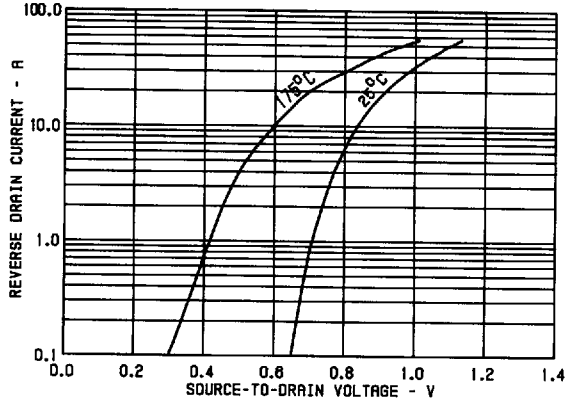


Figure 12 - Typical source-drain-diode forward voltage.

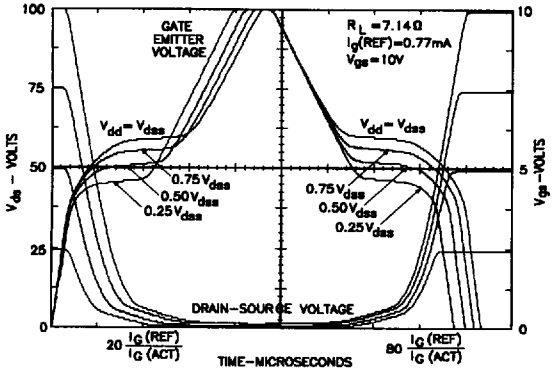


Figure 13 - Normalized switching waveforms for constant gate-current. (Refer to Harris application notes AN7254 and AN7260.)

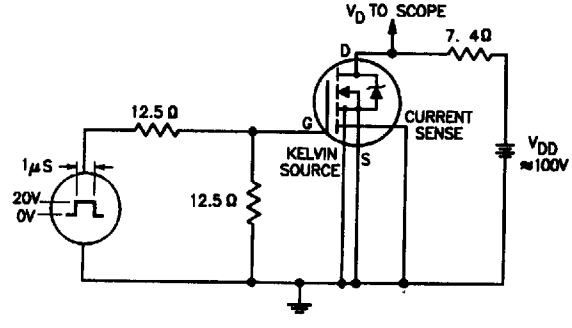


Figure 14 - Switching timetest circuit.

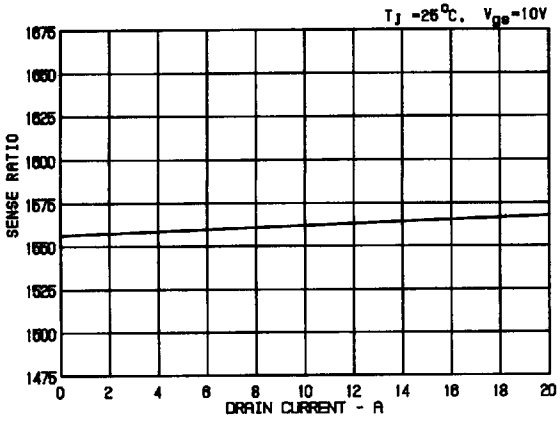


Figure 15 - Current sense ratio vs drain current.

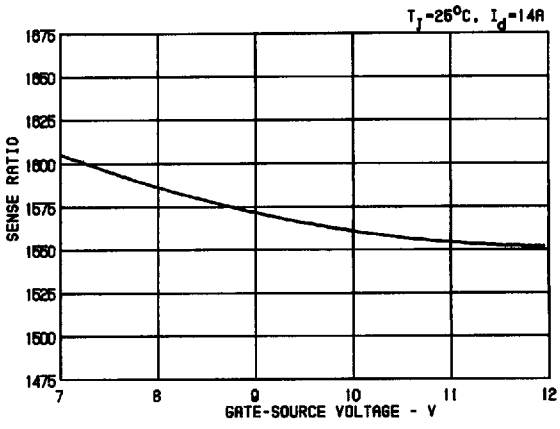


Figure 16 - Current sense ratio vs gate voltage.

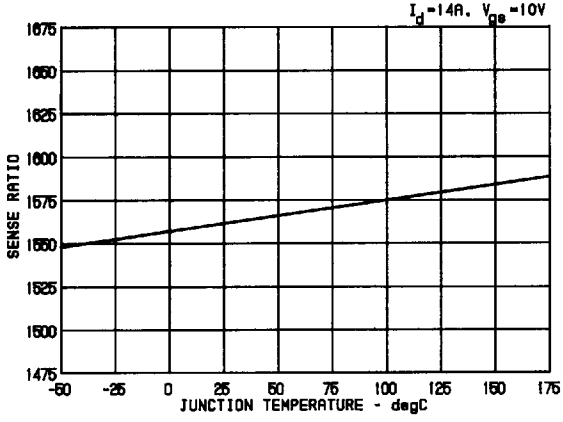


Figure 17 - Current sense ratio vs junction temperature.

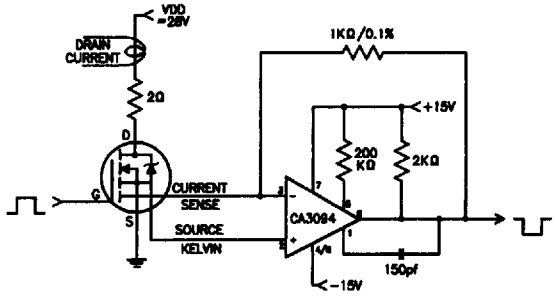


Figure 18 - Current sense ratio test circuit.

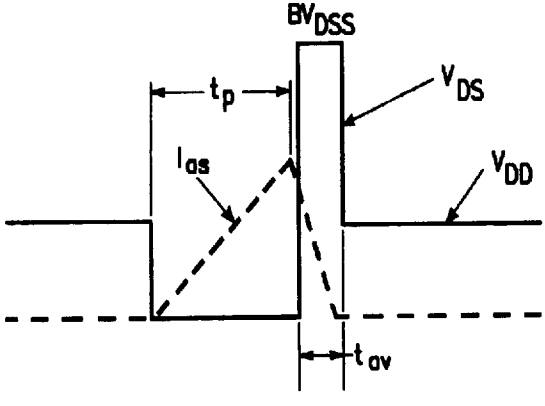


Figure 19 - UIS waveforms.

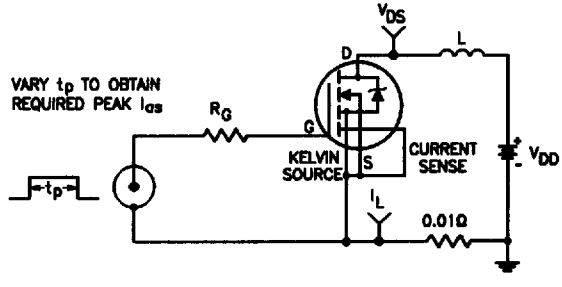


Figure 20 - UIS test circuit.