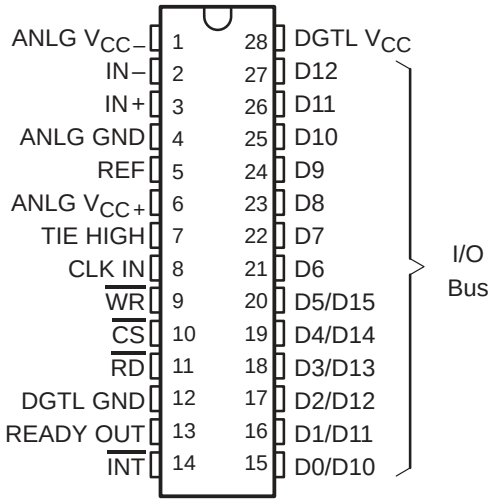
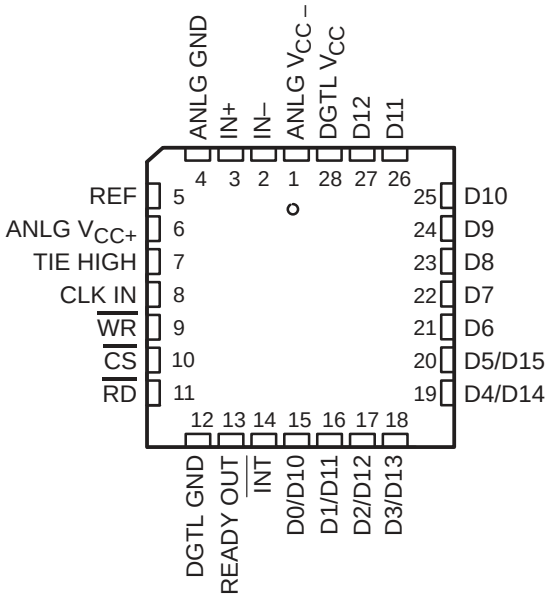
- **Advanced LinCMOS™ Technology**
- **Self Calibration Eliminates Expensive Trimming at Factory and Offset Adjustment in the Field**
- **12-Bit-Plus-Sign Resolution**
- **12-Bit Linearity**
- **12-μs Conversion Period at f_{clock} = 2 MHz†**
- **Compatible With All Microprocessors**
- **Single 5-V and ±5-V Supply Operation**
- **True Differential Analog Voltage Inputs With $-V_{ref}$ to V_{ref} Differential Input Range**
- **For Single 5-V Supply, Input Common-Mode Voltage Range is 0 V to 5 V**
- **For ±5-V Supplies, Input Common-Mode Voltage Range is –5 V to 5 V**
- **Unipolar or Bipolar Operation**
- **2s-Complement Output**
- **Low Power**
  - **85 mW Max on TLC1225I**
  - **87.5 mW Max on TLC1225M**

J OR NW PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



description

The TLC1225I and TLC1225M converters are manufactured with Texas Instruments highly efficient Advanced LinCMOS™ technology. The TLC1225I and TLC1225M CMOS analog-to-digital converters (ADCs) can be operated with a single 5-V supply or with ±5-V supplies. The differential input range is $-V_{ref}$ to V_{ref} in both supply configurations. The common-mode input range is ANLG V_{CC-} to ANLG V_{CC+}. For single 5-V supply operation, grounding IN– corresponds to standard unipolar conversion. For ±5-V supply operation, grounding IN– corresponds to standard bipolar conversion. Conversion is performed via the successive-approximation method. The TLC1225x outputs the converted data in a parallel word and interfaces directly to a 16-bit data bus. Negative numbers are given in the 2s-complement data format. All digital signals are fully TTL and CMOS compatible.

This converter uses a self-calibration technique by which seven of the internal capacitors in the capacitive array of the A/D conversion circuitry can be automatically calibrated. The internal capacitors are calibrated during a nonconversion capacitor-calibrate cycle in which all seven of the internal capacitors are calibrated at the same time. A conversion period requires only 24 clock cycles. Self calibration requires 300 clock cycles. The calibration or conversion cycle can be initiated at any time by issuing the proper command word to the data bus. The self-calibrating technique eliminates the need for expensive trimming of thin-film resistors at the factory and provides excellent performance at low cost.

† The conversion period is the reciprocal of the conversion rate and includes the access, sample, setup, and A/D conversion times.
Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

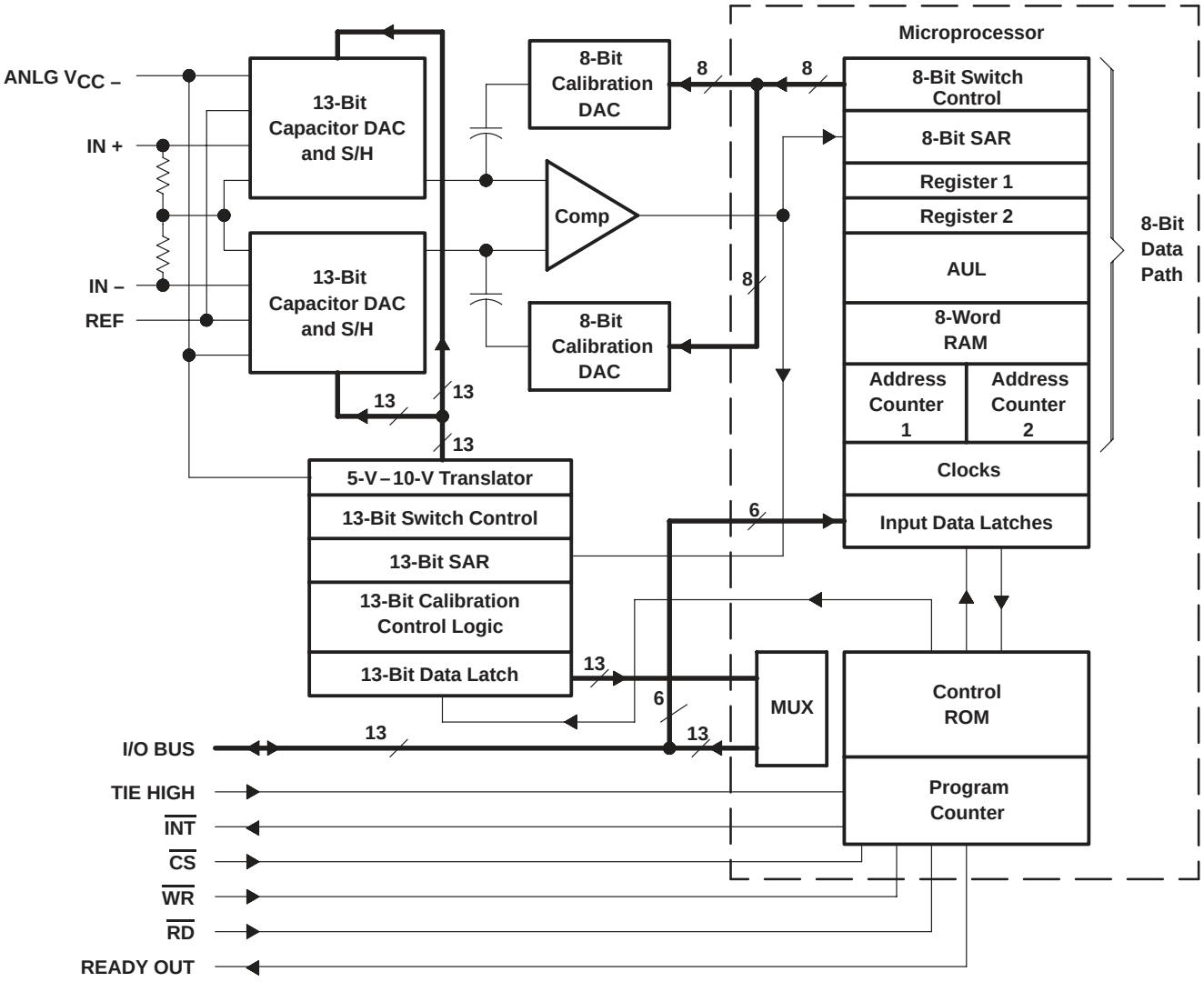
description (continued)

The TLC1225I is characterized for operation from –40°C to 85°C. The TLC1225M is characterized over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	CERAMIC CHIP CARRIER (FK)	PLASTIC CHIP CARRIER (FN)	CERAMIC DIP (J)	PLASTIC DIP (NW)
–40°C to 85°C		TLC1225IFN		TLC225INW
–55°C to 125°C	TLC1225MFK		TLC1225MJ	

functional block diagram



detailed description

calibration of comparator offset

The following actions are performed to calibrate the comparator offset:

1. The IN+ and IN– inputs are internally shorted together so that the converter input is zero. A coarse comparator offset calibration is performed by storing the offset voltages of the interconnecting comparator stages on the coupling capacitors that connect these stages (see Figure 1). The storage of offset voltages is accomplished by closing all switches and then opening switches A and A', then switches B and B', and then C and C'. This process continues until all interconnecting stages of the comparator are calibrated. After this action, some of the comparator offset remains uncalibrated.

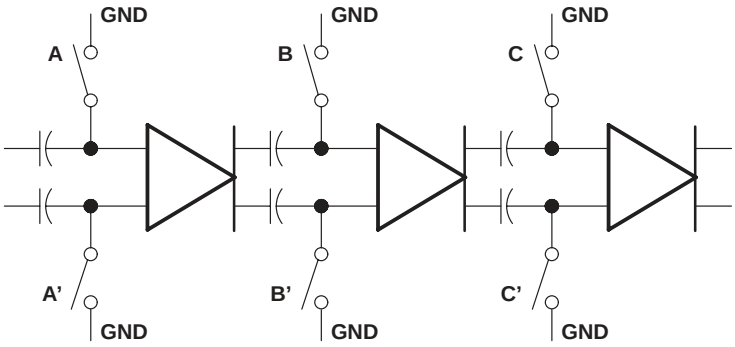


Figure 1. Comparator Offset Null

2. An A/D conversion is done on the remaining offset with the 8-bit calibration digital-to-analog converters (DACs) and 8-bit successive-approximation register (SAR), and the result is stored in the RAM.

calibration of the ADC capacitive capacitor array

The following actions are performed to calibrate capacitors in the 13-bit DACs that comprise the ADC's capacitive array:

1. IN+ and IN– are internally disconnected from the 13-bit DACs.
2. The most significant bit (MSB) capacitor is tied to REF, while the rest of the array capacitors are tied to GND. The A/D conversion result for the remaining comparator offset, obtained in step 2 above, is retrieved from the RAM and is input to the 8-bit DACs.
3. Step 1 of the calibration of comparator offset sequence is performed. The 8-bit DAC input is returned to zero, and the remaining comparator offset is then subtracted; thus, the comparator offset is completely corrected.
4. The MSB capacitor is tied to GND, while the rest of the array capacitors (C_X), are tied to REF. An MSB capacitor voltage error (see Figure 2) on the comparator output occurs if the MSB capacitor does not equal the sum of the other capacitors in the capacitive array. This error voltage is converted to an 8-bit word from which a capacitor error is computed and stored in the RAM.
5. The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above steps 1–4 while using the next most significant capacitor instead of the MSB capacitor. The seven most significant capacitors are calibrated in this manner.

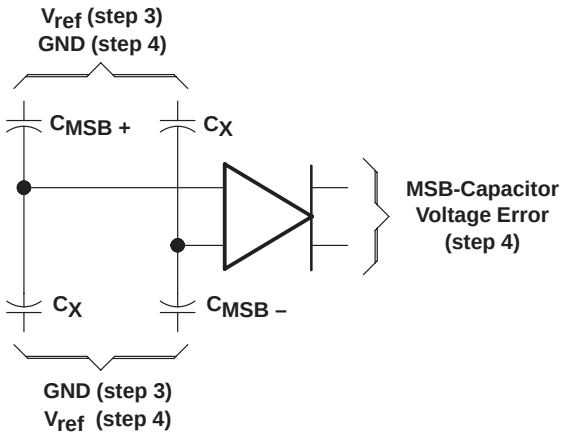


Figure 2. Capacitor Array Null

analog-to-digital conversion

The following steps are performed in the analog-to-digital conversion process:

- Step 1 of the calibration of comparator offset sequence is performed. The A/D conversion result for the remaining comparator offset, obtained in step 2 of the calibration of comparator offset, is retrieved from the RAM and is input to the 8-bit DACs. The comparator offset is completely corrected.
- IN+ and IN– are sampled into the 13-bit capacitive arrays.
- The 13-bit analog-to-digital conversion is performed. As the successive-approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in a register. This register controls the 8-bit DACs so the total accumulated error for these capacitors is subtracted out during the conversion process.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (ANLG V_{CC+} and DGTL V_{CC}) (see Note 1)	7.5 V
Supply voltage, ANLG V_{CC-}	–7.5 V
Differential supply voltage, ANLG V_{CC+} – ANLG V_{CC-}	15 V
Clock input voltage range	–0.3 V to V_{CC} + 0.3 V
Control input voltage range	–0.3 V to V_{CC} + 0.3 V
Analog input (IN+, IN–) voltage range, V_{I+} and V_{I-}	ANLG V_{CC-} –0.3 V to ANLG V_{CC+} +0.3 V
Reference voltage range, V_{ref}	–0.3 V to ANLG V_{CC+} +0.3 V
Voltage range, TIE HIGH	–0.3 V to ANLG V_{CC+} +0.3 V
Output voltage range	–0.3 V to DGTL V_{CC} +0.3 V
Input current (per pin)	±5 mA
Input current (per package)	±20 mA
Continued total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC1225I	–40°C to 85°C
TLC1225M	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK or FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: NW package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All analog voltages are referred to ANLG GND, and all digital voltages are referred to DGTL GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880mW	715 mW	275 mW
FN	1400 mW	11.2 mW/°C	896 mW	728 mW	280 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage	ANLG V_{CC+}	4.5	5.5	V
	ANLG V_{CC-}	–5.5	ANLG GND	
	DGTL V_{CC}	4.5	5.5	
High-level input voltage, V_{IH} (ANLG V_{CC} = DGTL V_{CC} = 4.75 to 5.25 V)	All digital inputs except CLK IN	2		V
	CLK IN	3.5		
Low-level input voltage, V_{IL} (ANLG V_{CC} = DGTL V_{CC} = 4.75 to 5.25 V)	All digital inputs except CLK IN		0.8	V
	CLK IN		1.4	
Analog input voltage, V_{I+}, V_{I-}		ANLG V_{CC-} – 0.05	ANLG V_{CC+} 0.05	V
High-level input voltage, TIE HIGH, V_{IH}	ANLG V_{CC} = DGTL V_{CC} = 5 V	2		V
Clock input frequency, f_{clock}	ANLG V_{CC} = DGTL V_{CC} = 5 V	0.3	2.6	MHz
Clock duty cycle	ANLG V_{CC} = DGTL V_{CC} = 5 V	40%	60%	
Pulse duration, $\overline{CS}$ and $\overline{WR}$ low, t_w	ANLG V_{CC} = DGTL V_{CC} = 5 V	15		ns
Setup time, I/O bus in before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_{su}	ANLG V_{CC} = DGTL V_{CC} = 5 V	60		ns
Hold time, I/O bus in after $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_h	ANLG V_{CC} = DGTL V_{CC} = 5 V	50		ns
Operating free-air temperature, T_A	TLC1225I	–40	85	°C
	TLC1225M	–55	125	

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = –5 V or ANLG GND (unless otherwise noted) (see Note 2)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage		DGTL V_{CC} = 4.75 V	I_O = –1.8 mA	2.4		V
				I_O = –50 µA	4.5		
V_{OL}	Low-level output voltage	TLC1225I	DGTL V_{CC} = 4.75 V, See Note 3	I_O = 3.2 mA,		0.4	V
		TLC1225M				0.45	
r_{ref}	Input resistance, REF				1	10	MΩ
I_{IH}	High-level input current		V_I = 5 V			5	µA
I_{IL}	Low-level input current		V_I = 0			–5	µA
I_{OZ}	High-impedance-state output leakage current		V_O = 0			–3	µA
			V_O = 5 V			3	
I_O	Output current		V_O = 0		–6		mA
			V_O = 5 V		8		
DGTL I_{CC}	Supply current from DGTL V_{CC}		f_{clock} = 2 MHz,	$\overline{CS}$ high		6	mA
ANLG I_{CC+}	Supply current from ANLG V_{CC+}	TLC1225I	f_{clock} = 2 MHz,	$\overline{CS}$ high		9	mA
		TLC1225M				8.5	
ANLG I_{CC-}	Supply current from ANLG V_{CC-}		f_{clock} = 2 MHz,	$\overline{CS}$ high		–3	mA

NOTES: 2. The input voltage range is defined as: V_{I+} = –5.05 V to 5.05 V, V_{I-} = –5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = –5 V. The input voltage range is defined as: V_{I+} = –0.05 V to 5.05 V, V_{I-} = –0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V when ANLG V_{CC-} = ANLG GND.

3. I_O = 4 mA for READY OUT, $\overline{INT}$, and D12.

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = –5 V or ANLG GND, f_{clock} = 2 MHz (unless otherwise noted) (see Note 2)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Integral linearity error					±0.012%	FSR‡
E_D	Differential linearity		–5 V < (IN+ – IN–) < 5 V, V_{CC+} = 5 V, V_{CC-} = – 5 V	≥–1		1	LSB§
			0 < (IN+ – IN–) < 5.05 V, V_{CC+} = 5 V, V_{CC-} = 0	≥–1		1	
	Zero error	TLC1225I				±1.5	LSB
		TLC1225M				±1	
	Unadjusted positive and negative full-scale error					± 2	LSB
	Temperature coefficient of gain				15		ppm/°C
	Temperature coefficient of offset point				1.5		ppm/°C
k_{SVS}	Supply voltage sensitivity	Zero error	ANLG V_{CC+} = 5 V ±5%, ANLG V_{CC-} = –5 V ±5%, DGTL V_{CC} = 5 V ±5%		± 0.75		LSB
		Positive and negative full-scale error			± 0.75		
		Linearity error			± 0.25		
CMRR	Common-mode rejection ratio		IN– = IN+ = –5 V to 5 V		65		dB
	Common-mode rejection (maximum code change from code 0000000000000)		IN– = IN+ = –5 V to 5 V		2		LSB
t_{conv}	Conversion period ($1/f_{clock}$) (see Notes 4 and 5)		f_{clock} = 2.6 MHz			24	clock cycles
t_a	Access time (delay from falling edge of $\overline{CS} \cdot \overline{RD}$ to data output)		C_L = 100 pF, f_{clock} = 2.6 MHz			95	ns
t_{dis}	Disable time, output (delay from rising edge of RD to high-impedance state)		R_L = 2 kΩ, C_L = 100 pF, f_{clock} = 2.6 MHz			90	ns
$t_{d1(READY)}$	Delay time, control signal edge to READY OUT		f_{clock} = 2.6 MHz	100			ns
$t_{d2(READY)}$	Delay time, control signal edge to READY OUT		f_{clock} = 2.6 MHz			100	ns
$t_{d(INT)}$	Delay time, $\overline{RD}$ or $\overline{WR}$ to reset of $\overline{INT}$		f_{clock} = 2.6 MHz			100	ns

† All typical values are at T_A = 25°C.
‡ FSR is full-scale range: 0.012% FSR linearity error is equivalent to 1 LSB = 1.22 mV.
§ No missing codes

NOTES: 2. The input voltage range is defined as: V_{I+} = –5.05 V to 5.05 V, V_{I-} = –5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \le 5.05$ V when ANLG V_{CC-} = –5 V. The input voltage range is defined as: V_{I+} = –0.05 V to 5.05 V, V_{I-} = –0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \le 5.05$ V when ANLG V_{CC-} = ANLG GND.

4. If $\overline{INT}$ and $\overline{RD}$ go low within the same f_{clock} period, $\overline{INT}$ is not reset until $\overline{WR}$ is brought low. If $\overline{INT}$ and $\overline{RD}$ do not go low within the same f_{clock} period, $\overline{INT}$ is reset.
5. The conversion period is the reciprocal of the conversion rate and includes the access, sample, setup, and A/D conversion times.

PARAMETER MEASUREMENT INFORMATION

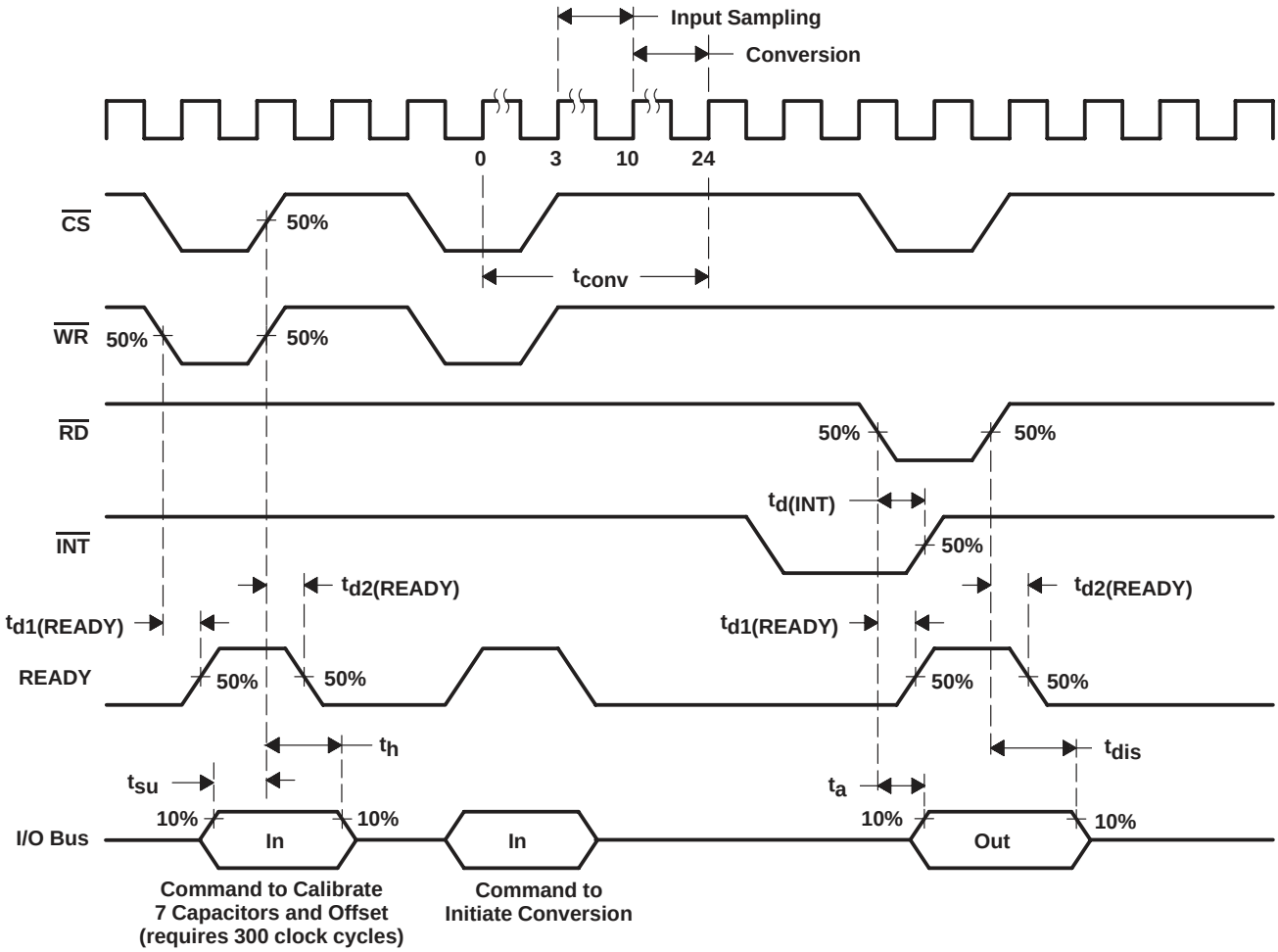


Figure 3. Timing Diagram

PARAMETER MEASUREMENT INFORMATION

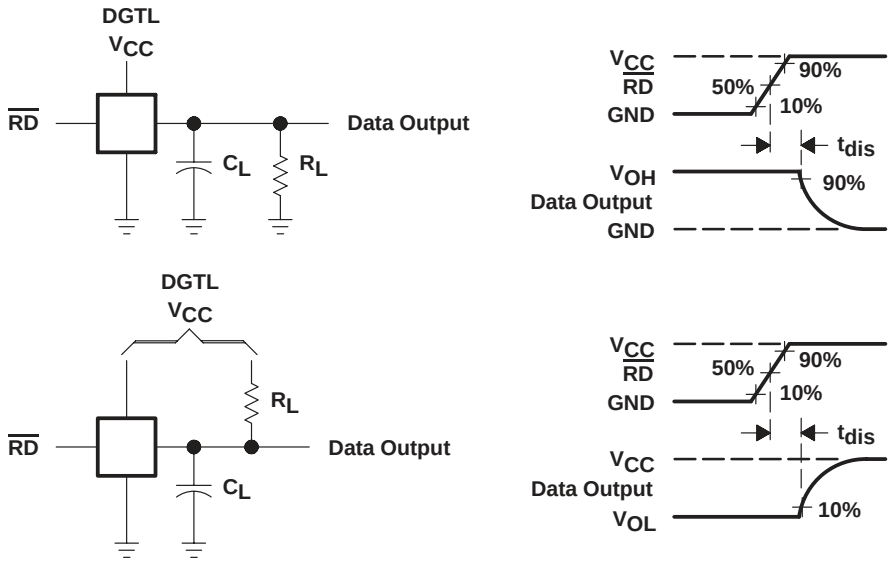


Figure 4. Load Circuits and Waveforms

APPLICATION INFORMATION

unipolar and bipolar operation

For single-ended signal input, the IN+ input is connected to the analog source and the IN– input is connected to ANLG GND. In the unipolar configuration, the ADC uses a single 5-V supply and the analog input voltage range is 0 V to 5 V. Data bit D12 always remains low. In the bipolar configuration, the ADC uses ±5-V supplies and the analog input voltage range is –5 V to 5 V. Data bit D12 indicates the sign of the input signal. In both configurations, the 13-bit data format is extended sign with 2s-complement, right-justified data.

power-up sequence

Calibration is not automatic on power up. Calibration is initiated by writing control words to the six least significant bits of the data bus. V_{ref} must have fully settled before calibration is initiated. If addressed or initiated, conversion can begin after the first clock cycle; however, full A/D conversion accuracy is not established until after internal capacitor calibration.

conversion period start sequence

The writing of the conversion command word to the six least significant bits of the data bus when either $\overline{CS}$ or $\overline{WR}$ goes high initiates the conversion sequence.

analog sampling sequence

Sampling of the input signal occurs during clock cycles 3 through 10 of the conversion sequence.

completed A/D conversion

When $\overline{INT}$ goes low, conversion is complete and the A/D result can be read. A new conversion period can begin immediately. The A/D conversion is complete at the end of clock cycle 24 of the conversion period.

APPLICATION INFORMATION

aborting a conversion period in process and beginning a new conversion

If a conversion period is initiated while a conversion sequence is in process, the ongoing conversion is aborted and a new conversion period begins.

reading the conversion result

When both $\overline{CS}$ and $\overline{RD}$ go low, all 13 bits of conversion data are output to the I/O bus. The format of the output is extended sign with 2s-complement, right-justified data. The sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative.

general

reset $\overline{INT}$

When reading the conversion data, the falling edge of the first low-going combination of $\overline{CS}$ and $\overline{RD}$ reset $\overline{INT}$. The falling edge of the low-going combination of $\overline{CS}$ and $\overline{WR}$ also reset $\overline{INT}$.

ready out

For high-speed microprocessors, READY OUT allows the TLC1225 to insert a wait state in the microprocessor's read or write cycle.

reference voltage (V_{ref})

This voltage defines the range for $|V_{I+} - V_{I-}|$. When $|V_{I+} - V_{I-}|$ equals V_{ref}, the highest conversion data value results. When $|V_{I+} - V_{I-}|$ equals 0, the conversion data value is zero. For a given input, the conversion data changes ratiometrically with changes in V_{ref}. Calibration should be performed with the same value of V_{ref} that is used during conversion.

TIE HIGH

TIE HIGH is a digital input and should be tied high.

calibration and conversion period considerations

Calibration of the internal capacitors and A/D conversion are two separate actions. Each action is independently initiated. A calibration command should be initiated prior to subsequent conversions; it is not necessary to recalibrate before each conversion. Capacitor calibration is expected to last indefinitely as long as the clock signal and power are not interrupted. The offset calibration may drift with temperature changes. The temperature coefficient of the offset point is shown in the electrical characteristics table. Periodic calibration is recommended. Calibration and conversion commands require 300 and 24 clock cycles, respectively.

The calibrate and conversion commands are initiated by writing control words on the six least significant bits of the data bus. These control words are written into the IC when either $\overline{CS}$ or $\overline{WR}$ goes high. The initiation of these commands is illustrated in Figure 3. The bit patterns for the commands are shown in Table 1.

Table 1. Conversion Commands

COMMAND	$\overline{CS}$ + $\overline{WR}$	I/O BUS						REQUIRED NUMBER OF CLOCK CYCLES
		D15	D14	D13	D12	D11	D10	
Conversion	↑	H	L	X	X	X	L	24
Calibrate†	↑	L	X	L	L	L	L	300

† Calibration is lost when the clock is stopped.

APPLICATION INFORMATION

analog inputs

differential inputs provide common-mode rejection

The differential inputs reduce common-mode noise. Common-mode noise is noise common to both IN+ and IN– inputs, such as 60-Hz noise. There is no time interval between the sampling of the IN+ and IN–, so these inputs are truly differential. No conversion errors result from a time interval between the sampling of the IN+ and IN– inputs.

input bypass capacitors

Input bypass capacitors can be used for noise filtering; however, the charge on these bypass capacitors is depleted during the input sampling sequence when the internal sampling capacitors are charged. The charging of the bypass capacitors through the differential source resistances must keep pace with the charge depletion of the bypass capacitors during the input sampling sequence. Higher source resistances reduce the amount of charging current for the bypass capacitors. Also fast, successive conversion has the greatest charge depletion effect on the bypass capacitors. The above phenomenon becomes more significant as source resistances and the conversion rate (i.e., higher clock frequency and conversion initiation rate) increase.

In addition, if the above phenomenon prevents the bypass capacitors from fully charging between conversions, voltage drops across the source resistances result due to the ongoing bypass capacitor charging currents. The voltage drops cause a conversion error. Also, the voltage drops increase with higher $|V_{I+} - V_{I-}|$ values, higher source resistances, and lower charge on the bypass capacitors (i.e., faster conversion rate).

For low-source-resistance applications ($R_{source} < 100\ \Omega$), a 0.001-µF bypass capacitor at the inputs prevents pickup due to the series lead inductance of a long wire. A 100-Ω resistor can be placed between the capacitor and the output of an operational amplifier to isolate the capacitor from the operational amplifier.

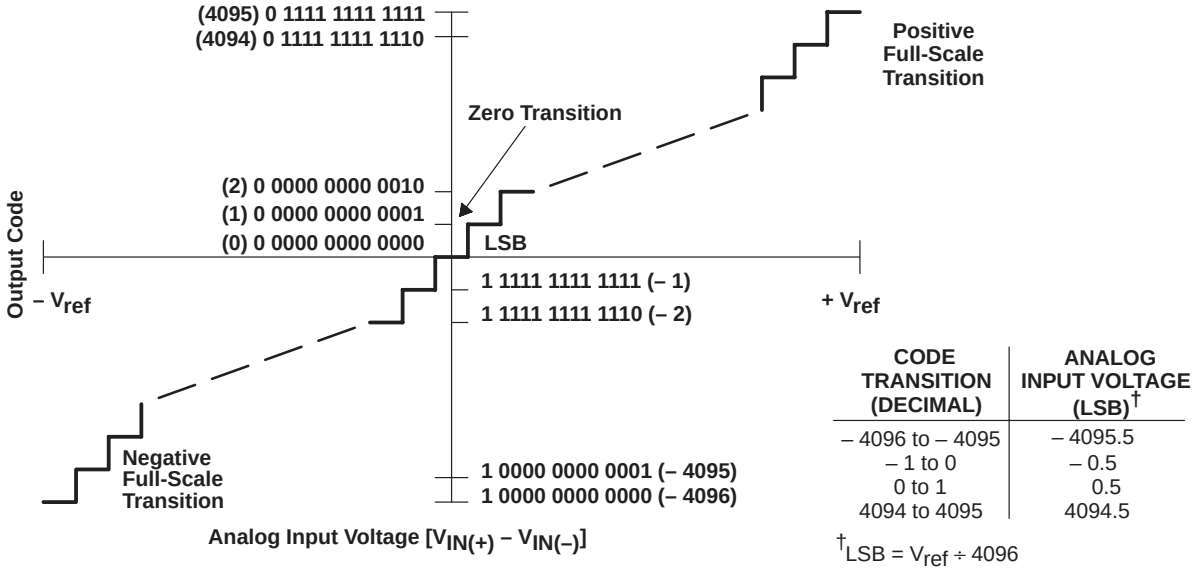
input leads

The input leads should be kept as short as possible since the coupling of noise and digital clock signals to the the inputs can cause errors.

power supply considerations

Noise spikes on the V_{CC} lines can cause conversion error. Low-inductance tantalum capacitors (> 1 µF) with short leads should be used to bypass ANLG V_{CC} and DGTL V_{CC}. A separate regulator for the TLC1225 and other analog circuitry greatly reduces digital noise on the supply line. A ferrite bead or equivalent inductance can be used between the analog and digital ground planes if the digital ground noise is excessive.

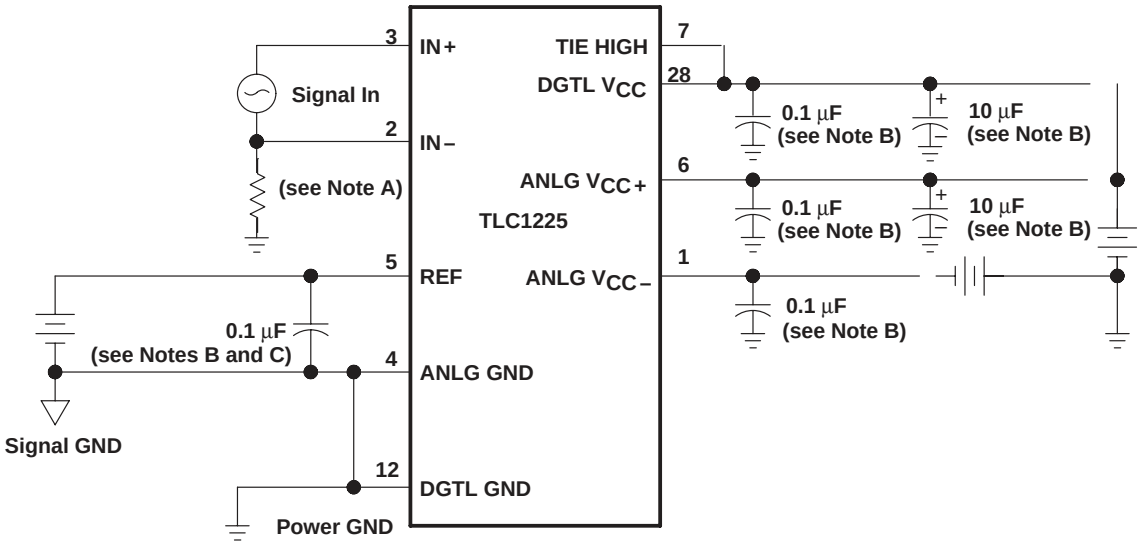
APPLICATION INFORMATION



CODE TRANSITION (DECIMAL)	ANALOG INPUT VOLTAGE (LSB)†
– 4096 to – 4095	– 4095.5
– 1 to 0	– 0.5
0 to 1	0.5
4094 to 4095	4094.5

†LSB = V_{ref} ÷ 4096

Figure 5. Transfer Characteristic



NOTES: A. The analog input must have some current return path to ANLG GND.
B. Bypass capacitor leads must be as short as possible.
C. For high-accuracy applications, use a larger capacitor to reduce reference noise.

Figure 6. Analog Considerations

APPLICATION INFORMATION

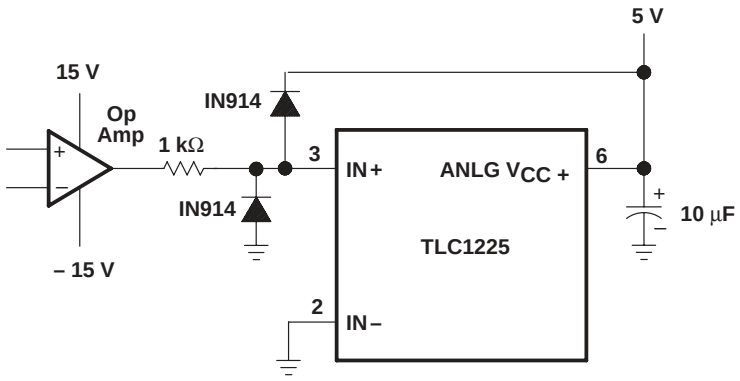
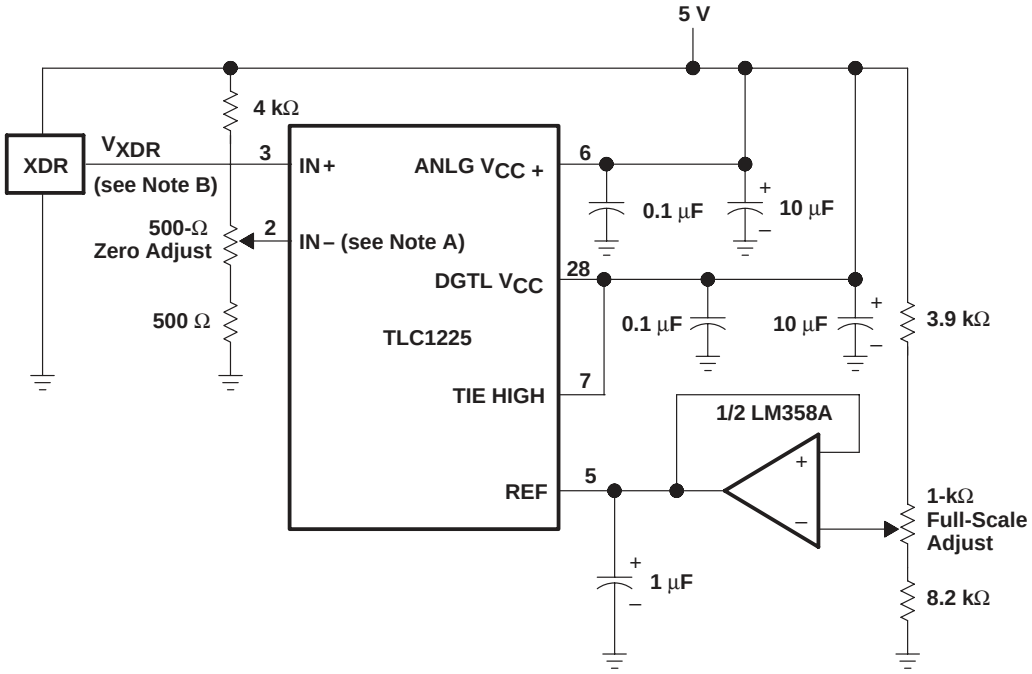


Figure 7. Input Protection



NOTES: A. $V_I = 0.15 \times \text{ANLG } V_{CC+}$
B. 15% of ANLG $V_{CC} \le V_{XDR} \le$ 85% of ANLG V_{CC}

Figure 8. Operating With Ratiometric Transducers

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