

## Automotive 3-Phase Isolator MOSFET Driver

### FEATURES AND BENEFITS

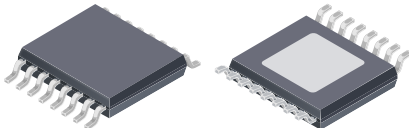
- Three floating N-channel MOSFET drives
- Maintains  $V_{GS}$  with 100 k $\Omega$  gate-source resistors
- Integrated charge pump controller
- 4.5 to 50 V supply voltage operating range
- Two independent activation inputs
- Single phase-enable input
- VCP and VGS undervoltage protection
- 150°C ambient (165°C junction) continuous

### APPLICATIONS

- 3-phase disconnect for up to ASIL D level systems
- Electric power steering (EPS)
- Electric braking
- 3-phase solid-state relay driver

### PACKAGE:

16-lead TSSOP with exposed thermal pad (suffix LP)



*Not to scale*

### DESCRIPTION

The A6862 is an N-channel power MOSFET driver capable of controlling MOSFETs connected as a 3-phase solid-state relay in phase-isolation applications. It has three independent floating gate drive outputs to maintain the power MOSFETs in the on-state over the full supply range with high phase-voltage slew rates. An integrated charge pump regulator provides the above battery supply voltage necessary to maintain the power MOSFETs in the on-state continuously when the phase voltage is equal to the battery voltage. The charge pump will maintain sufficient gate drive (>7.5 V) for battery voltages down to 4.5 V with 100 k $\Omega$  gate source resistors.

The three gate drives can be controlled by a single logic-level input. In typical applications, the MOSFETs will be switched on within 8  $\mu$ s and will switch off within 1  $\mu$ s.

Two independent activation inputs can be used to put the A6862 into a low-power sleep mode with the charge pump disabled.

Undervoltage monitors check that the pumped supply voltage and the gate drive outputs are high enough to ensure that the MOSFETs are maintained in a safe conducting state.

The A6862 is supplied in a 16-lead TSSOP (LP) with exposed pad for enhanced thermal dissipation. They are lead (Pb) free, with 100% matte-tin leadframe plating.

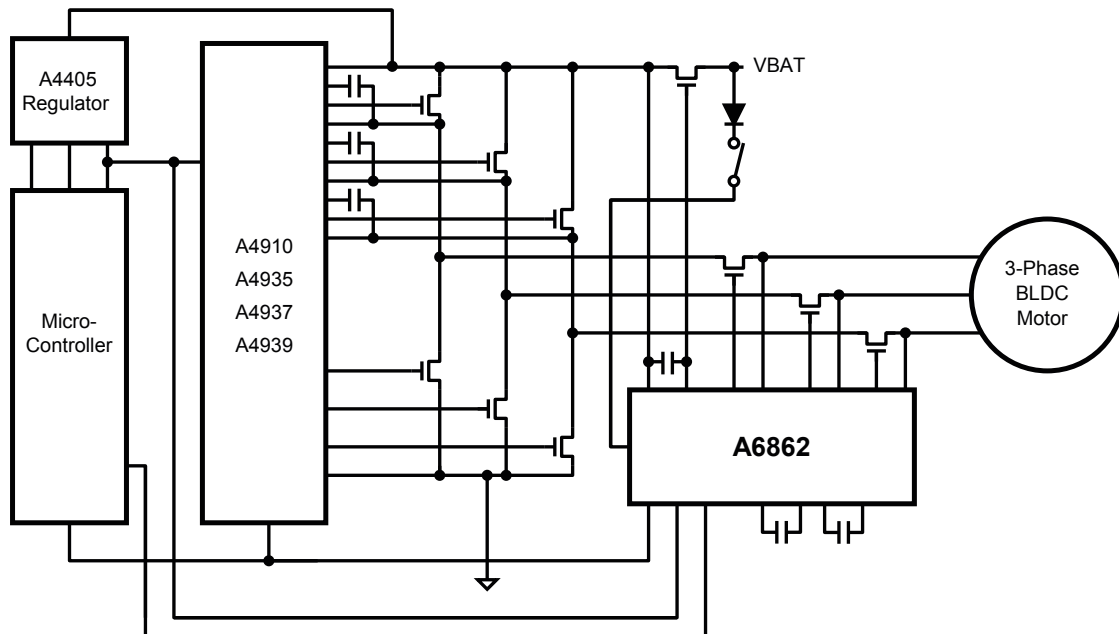


Figure 1: Typical Application Diagram

## SELECTION GUIDE

Part Number	Packing	Package
A6862KLPTR-T	4000 pieces per 13-inch reel	16-lead TSSOP with exposed thermal pad, 4.4 mm × 5 mm case

## SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Units
Load Voltage Supply	$V_{BB}$		-0.3 to 50	V
Terminal VCP	$V_{CP}$		$V_{BB} - 0.3$ to $V_{BB} + 12$	V
Terminal CP1	$V_{CP1}$		$V_{BB} - 12$ to $V_{BB} + 0.3$	V
Terminal CP2	$V_{CP2}$		$V_{BB} - 0.3$ to $V_{CP4} + 0.3$	V
Terminal CP3	$V_{CP3}$		$V_{BB} - 12$ to $V_{BB} + 0.3$	V
Terminal CP4	$V_{CP4}$		$V_{CP2} - 0.3$ to $V_{CP} + 0.3$	V
Terminal IG, POK, ENA	$V_I$		-0.3 to 50	V
Terminal GU, GV, GW	$V_{GX}$		$V_{SX} - 0.3$ to $V_{SX} + 12$	V
Terminal SU, SV, SW	$V_{SX}$		-6 to 55	V
Operating Ambient Temperature	$T_A$	Limited by power dissipation	-40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	$T_{Jt}$	Overtemperature event not exceeding 10 seconds; lifetime duration not exceeding 10 hours; guaranteed by design characterization.	175	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

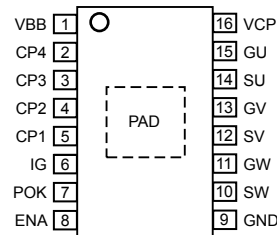
[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.

## THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [2]	Value	Units
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	34	°C/W
		1-layer PCB with copper limited to solder pads	43	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

[2] Additional thermal data available on the Allegro Web site.

## PINOUT DIAGRAM AND TERMINAL LIST TABLE

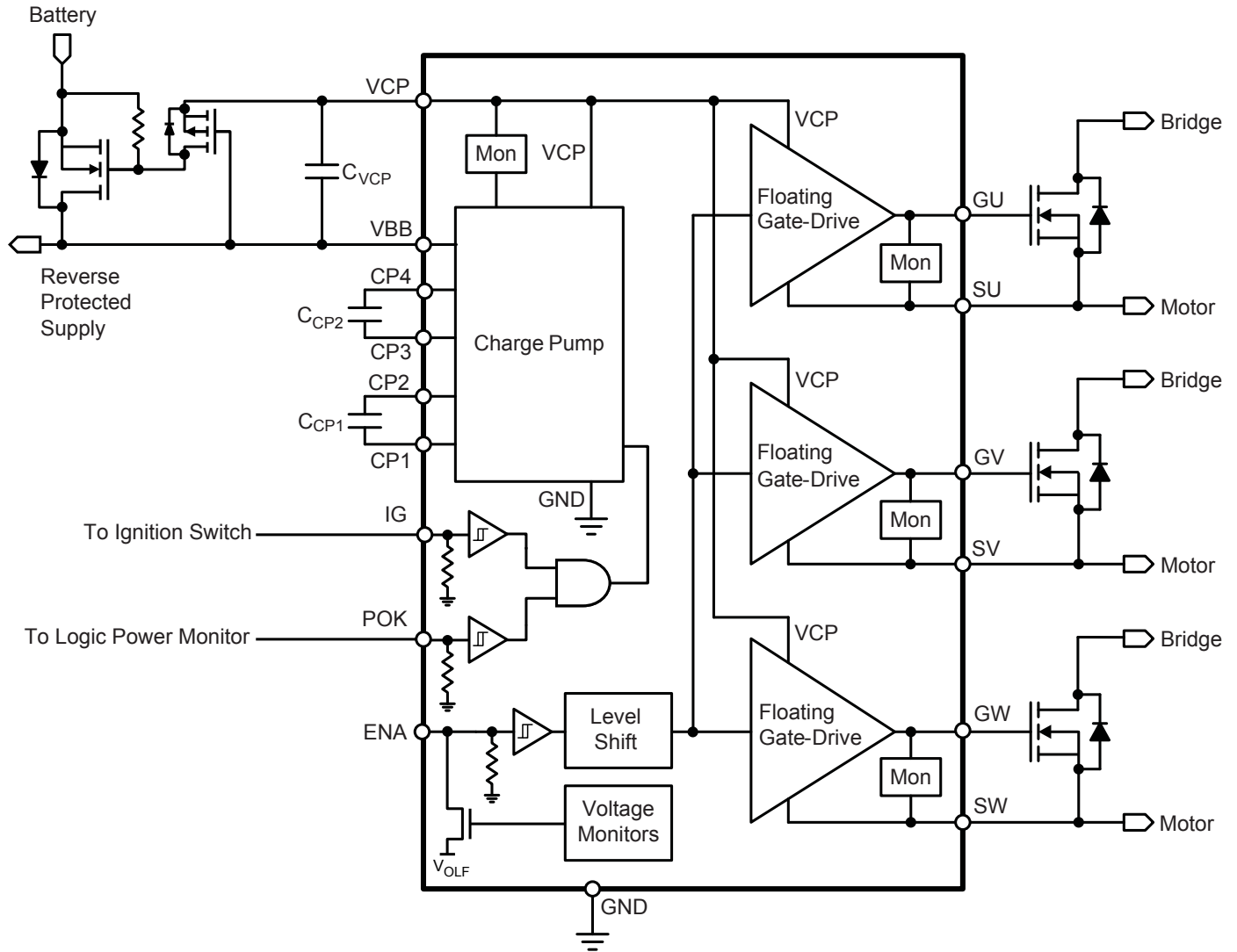


Package LP, 16-Pin TSSOP Pinout Diagram

## Terminal List Table

Name	Number	Description
CP1	5	Pump capacitor connection
CP2	4	Pump capacitor connection
CP3	3	Pump capacitor connection
CP4	2	Pump capacitor connection
ENA	8	Phase enable input
GND	9	Ground
GU	15	U-phase MOSFET gate drive
GV	13	V-phase MOSFET gate drive
GW	11	W-phase MOSFET gate drive
IG	6	Ignition input
POK	7	Power OK input
SU	14	U-phase MOSFET source reference
SV	12	V-phase MOSFET source reference
SW	10	W-phase MOSFET source reference
VBB	1	Main power supply
VCP	16	Pumped supply
PAD	–	Exposed pad; connect to GND

FUNCTIONAL BLOCK DIAGRAM



**ELECTRICAL CHARACTERISTICS:** Valid at  $T_J = -40$  to  $150^\circ\text{C}$ ,  $V_{BB} = 4.5$  to  $50$  V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
<b>SUPPLY</b>						
VBB Functional Operating Range <sup>[1]</sup>	$V_{BB}$	Operating; outputs active	4.5	–	50	V
		Operating; outputs disabled	4	–	50	V
		No undefined states	0	–	50	V
VBB Supply Current	$I_{BB}$	Gate drive active, $V_{BB} = 12$ V	–	11	15	mA
	$I_{BBQ}$	Gate drive inactive, $V_{BB} = 12$ V	–	6	9	mA
	$I_{BBS}$	IG or POK $< 0.8$ V, $V_{BB} = 12$ V	–	–	10	$\mu\text{A}$
VCP Output Voltage w.r.t. $V_{BB}$	$V_{CP}$	$V_{BB} > 9$ V, $I_{VCP} > -1$ mA <sup>[2]</sup>	9	10	11	V
		$6$ V $< V_{BB} \leq 9$ V, $I_{VCP} > -1$ mA <sup>[2]</sup>	8	10	11	V
		$4.5$ V $< V_{BB} \leq 6$ V, $I_{VCP} > -800$ $\mu\text{A}$ <sup>[2]</sup>	7.5	9.5	–	V
VCP Static Load Resistor	$R_{CP}$	Between VCP and VBB (using $\pm 1\%$ tolerance resistor)	100	–	–	k $\Omega$
<b>GATE DRIVE</b>						
Turn-On Time	$t_r$	$C_{LOAD} = 10$ nF, 20% to 80%	–	5	–	$\mu\text{s}$
Turn-Off Time	$t_f$	$C_{LOAD} = 10$ nF, 80% to 20%	–	0.5	–	$\mu\text{s}$
Propagation Delay – Turn On <sup>[3]</sup>	$t_{PON}$	$C_{LOAD} = 10$ nF, ENx high to Gx 20%	–	–	3	$\mu\text{s}$
Propagation Delay – Turn Off <sup>[3]</sup>	$t_{POFF}$	$C_{LOAD} = 10$ nF, ENx low to Gx 80%	–	–	2.25	$\mu\text{s}$
Turn-On Pulse Current	$I_{GXP}$		8.5	10	12	mA
Turn-On Pulse Time	$t_{GXP}$		16	–	36	$\mu\text{s}$
On Hold Current	$I_{GXH}$		–	400	–	$\mu\text{A}$
Pull-Down On Resistance	$R_{DS(on)DN}$	$T_J = 25^\circ\text{C}$ , $I_{Gx} = 10$ mA	–	5	–	$\Omega$
		$T_J = 150^\circ\text{C}$ , $I_{Gx} = 10$ mA	–	10	–	$\Omega$
Gx Output High Voltage w.r.t. $S_x$ , when $S_x \leq V_{BB}$	$V_{GH}$	$V_{BB} > 9$ V	9	10	12	V
		$6$ V $< V_{BB} \leq 9$ V	8	10	12	V
		$4.5$ V $< V_{BB} \leq 6$ V	7.5	9.5	–	V
Gate Drive Static Load Resistor	$R_{GS}$	Between Gx and $S_x$ (using $\pm 1\%$ tolerance resistor)	100	–	–	k $\Omega$
Gx Output Voltage Low	$V_{GL}$	$-10$ $\mu\text{A} < I_{Gx} < 10$ $\mu\text{A}$	–	–	$V_{SX} + 0.3$	V
Gx Passive Pull-Down	$R_{GPD}$	$V_{Gx} - V_{Sx} < 0.3$ V	–	950	–	k $\Omega$

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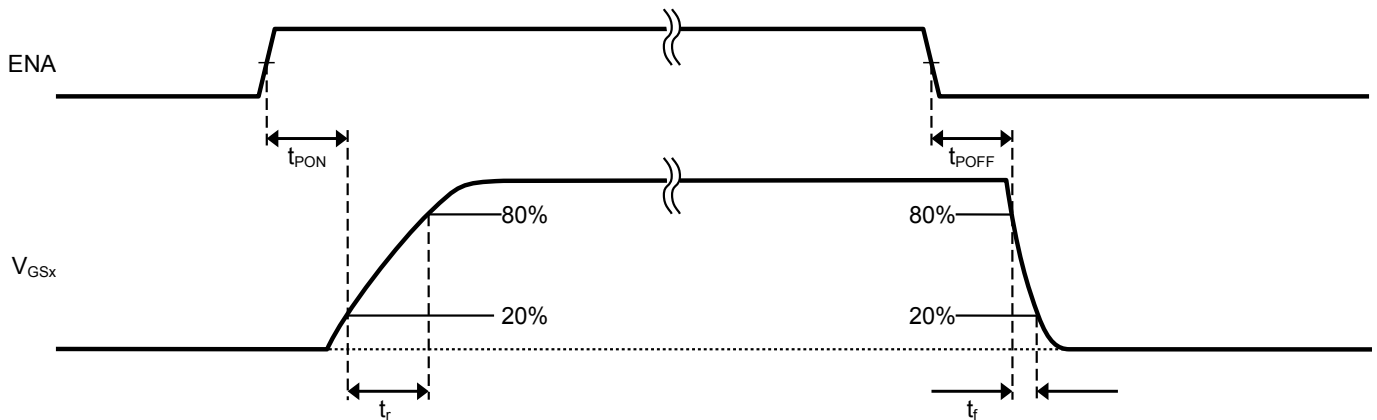
**ELECTRICAL CHARACTERISTICS (continued):** Valid at  $T_J = -40$  to  $150^\circ\text{C}$ ,  $V_{BB} = 4.5$  to  $50$  V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
<b>LOGIC INPUTS AND OUTPUTS</b>						
ENA Input Low Voltage	$V_{IL}$		–	–	0.4	V
ENA Input High Voltage	$V_{IH}$		0.7	–	–	V
ENA Input Hysteresis	$V_{Ihys}$		120	200	–	mV
ENA Input Pull-Down Resistor	$R_{PD}$		–	100	–	k $\Omega$
ENA Output Low Voltage	$V_{OLF}$	Any $V_{GS}$ or $V_{CP}$ undervoltage, $I_{OL} = -0.5$ mA [2]	1.1	1.0	0.9	V
POK, IG Input High Voltage	$V_{IH}$		2.0	–	–	V
POK, IG Input Low Voltage	$V_{IL}$		–	–	0.8	V
POK, IG Input Pull-Down Resistor	$R_{PD}$		–	100	–	k $\Omega$
<b>DIAGNOSTICS AND PROTECTION</b>						
VGS Undervoltage Threshold Rising	$V_{GSUV}$		6.0	–	7.0	V
VGS Undervoltage Threshold Hysteresis	$V_{GS hys}$		–	200	–	mV
VGS Undervoltage Filter Time	$t_{GSUV}$		3.7	–	18	$\mu\text{s}$
VCP Undervoltage Filter Time	$t_{CPUTV}$		–	12.5	–	$\mu\text{s}$
VCP Startup Blank Timer	$t_{CPON}$		–	100	–	$\mu\text{s}$
VCP Undervoltage Lockout	$V_{CPON}$	$V_{CP}$ w.r.t. $V_{BB}$ , $V_{CP}$ rising	6.5	7.0	7.5	V
	$V_{CPOFF}$	$V_{CP}$ w.r.t. $V_{BB}$ , $V_{CP}$ falling	6.25	6.75	7.25	V

[1] Function is correct but parameters are not guaranteed below the general limits (4.5 to 50 V).

[2] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.

[3] Refer to Figure 2.



**Figure 2: Enable Input to  $V_{GS}$  Timing**

## FUNCTIONAL DESCRIPTION

The A6862 is an N-channel power MOSFET driver capable of controlling MOSFETs connected as a 3-phase solid-state relay in phase-isolation applications. It has three independent floating gate drive outputs to maintain the power MOSFETs in the on-state or the off-state over the full supply range when the phase outputs are PWM switched with high phase-voltage slew rates.

The three gate drives can be controlled by a single logic-level signal on the enable input. In typical applications, the MOSFETs will be switched on within 8  $\mu$ s and will switch off within 1  $\mu$ s. The enable input can also be used as an open-drain output to indicate that the charge pump regulator is undervoltage.

A charge pump regulator provides the above-battery supply voltage necessary to maintain the power MOSFETs in the on-state continuously when the phase voltage is equal to the battery voltage. Voltage regulation is based on the difference between  $V_{BB}$  and  $V_{CP}$ .

The charge pump will maintain sufficient gate drive ( $>7.5$  V) for battery voltages down to 4.5 V. It is also able to provide the current taken by gate source resistors as low as 100 k $\Omega$ , should they be required, between the source and gate of the power MOSFETs.

The voltage generated by the charge pump can also be used to power circuitry to control the gate source voltage for a MOSFET connected to the main supply to provide reverse battery protection.

Two independent activation inputs can be used to disable the charge pump and put the A6862 into a low-power sleep mode. These two inputs can be driven by logic-level signals or connected directly to other systems supplies including the main battery supply through an external reverse protection diode.

Undervoltage monitors check that the pumped supply voltage and the gate drive outputs are high enough to ensure that the MOSFETs are maintained in a safe conducting state. If the pumped supply voltage or any gate drive output voltage is less than the undervoltage threshold, the enable input ENA will be pulled low by an open-drain output.

All logic inputs can be shorted to the main positive battery supply voltage without damage, even during a load dump up to 50 V.

## Input and Output Terminal Functions

**VBB:** Main power supply. The main power supply should be connected to VBB through a reverse voltage protection circuit.

**GND:** Main power supply return. Connect to supply ground.

**VCP:** Pumped gate drive voltage. Can be used to turn on a MOSFET connected to the main supply, to provide reverse battery protection. Connect a 1  $\mu$ F ceramic capacitor between VCP and VBB.

**CP1, CP2:** Pump capacitor connections. Connect a 330 nF ceramic capacitor between CP1 and CP2.

**CP3, CP4:** Pump capacitor connections. Connect a 330 nF ceramic capacitor between CP3 and CP4.

**ENA:** Logic-level input to control all three gate drive outputs. Pulled to VOLF by open-drain output if VCP or any VGSx is undervoltage. Battery voltage compliant terminal.

**POK:** Logic-level input to control the pump regulator activity. Both POK and IG must be high to enable the charge pump. Battery voltage compliant terminal.

**IG:** Logic-level input to control the pump regulator activity. Both POK and IG must be high to enable the charge pump. Battery voltage compliant terminal.

**GU, GV, GW:** Floating gate drive outputs for external N-channel MOSFETs.

**SU, SV, SW:** Load phase connections. These terminals are the reference connections for the floating gate drive outputs.

## Power Supplies

A single reverse polarity protected power supply voltage is required. It is recommended to decouple the supply with ceramic capacitors connected close to the supply and ground terminals.

The A6862 will operate within specified parameters with  $V_{BB}$  from 4.5 to 50 V and can maintain the external isolator MOSFETs in the off condition down to 4.0 V. The A6862 will operate without any undefined states down to 0 V to ensure deterministic operation during power-up and power-down events. As the supply voltage rises from 0 V, the gate drive outputs are maintained in the off-state until the gate voltage is sufficiently high to ensure conduction and the outputs are enabled.

This provides a very rugged solution for use in the harsh automotive environment and permits use in start-stop systems.

## Pump Regulator

The gate drivers are powered by a regulated charge pump, which provides the voltage above  $V_{BB}$  to ensure that the MOSFETs are fully enhanced with low on-resistance when the source of the MOSFET is at the same voltage as  $V_{BB}$ .

Voltage regulation is based on the difference between the  $V_{BB}$  and  $V_{CP}$  pins.

The pumped voltage,  $V_{CP}$ , is available at the  $V_{CP}$  terminal and is limited to 12 V maximum with respect to  $V_{BB}$ . This removes the need for external clamp diodes on the power MOSFETs to limit the gate source voltage.

It also allows the  $V_{CP}$  terminal to be used to power circuitry to control MOSFETs connected to the main supply to provide reverse battery protection and supply isolation.

To provide the continuous low-level current required when gate source resistors are connected to the external MOSFETs, a pump storage capacitor, typically 1  $\mu$ F, must be connected between the  $V_{CP}$  and  $V_{BB}$  terminals. Pump capacitors, typically 330 nF, must be connected between the  $CP1$  and  $CP2$  terminals and between the  $CP3$  and  $CP4$  terminals to provide sufficient charge transfer, especially at low supply voltage. If driving MOSFETs with a total charge above 400 nC, larger value capacitors (charge pump capacitors and  $C_{VCP}$ ) may be necessary.

The charge pump can be disabled by pulling either the  $POK$  or the  $IG$  terminal low. This will cause  $V_{CP}$  to reduce to zero, the outputs to switch off, and the A6862 to enter a low-power sleep mode with minimum supply current.

## Gate Drives

The A6862 is designed to drive external, low on-resistance, power N-channel MOSFETs when used in a phase isolation application. The gate drive outputs and the  $V_{CP}$  supply will turn the MOSFETs on in typically 8  $\mu$ s and will maintain the on-state during transients on the source of the MOSFETs. The gate drive outputs will turn the MOSFETs off in typically 1  $\mu$ s and will hold them in the off-state during transients on the source. An integrated hold-off circuit will ensure that the gate source

voltage of the MOSFET is held close to 0 V even with the power disconnected. This can remove the need for additional gate source resistors on the isolation MOSFETs. If gate source resistors are mandatory for the application, then the pump regulator can provide sufficient current to maintain the MOSFET in the on-state with a gate source resistor of as low as 100 k $\Omega$  using 1% tolerance resistors.

The floating gate drive outputs for external N-channel MOSFETs are provided on pins  $GU$ ,  $GV$ , and  $GW$ . The reference points for the floating drives are the load phase connections:  $SU$ ,  $SV$ , and  $SW$ . The discharge current from the floating MOSFET gate capacitance flows through these connections.

When  $ENA$  goes high, the upper-half of all of the drivers are turned on (low sides are turned off) and a current ( $I_{GXP}$ ) will be sourced to the gate, for a period of time defined between  $t_{GXP}$ . After this period, an “on hold current” ( $I_{GXH}$ ) will be sourced to the gates of the MOSFETs to keep them switched on. See Figure 3.

When  $ENA$  goes low, the lower half of the drivers are turned on (high side is turned off) and will sink current from the external MOSFET’s gates to the respective  $Sx$  terminal, turning them off. See Figure 3.

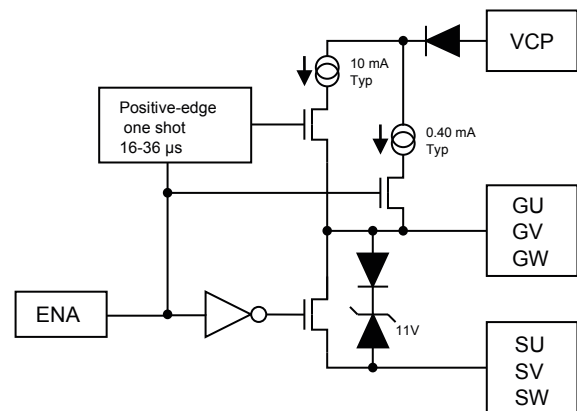


Figure 3: Operational Output Drive



**Recirculation Current Path**

In most applications, it will be necessary to provide a current recirculation path when the motor load is isolated. This will be necessary when the motor driver does not reduce the load current to zero before the isolation MOSFETs are turned off.

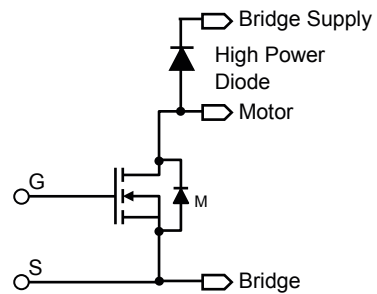
There are two ways of connecting the external MOSFETs to the motor: with the source connected to the bridge or supply (see Figure 4), and conversely with the source connected to the motor or load (see Figure 5 and Figure 6). All methods require one diode per phase.

In the case when the Bridge or supply is connected to the source (see Figure 4). When the current is flowing from bridge to the motor and the MOSFET is switch off, the motor inductance will try to force the voltage on the drain pin down. This will draw current through the body diode from the bridge. If the bridge is still on, the current will come from the positive supply, or if it is off, the current will come from the bridge low-side body diode. If the current is flowing from the motor to the bridge and the MOSFET is switched off, the motor inductance will force the voltage on the drain pin up and the high-power diode is required to clamp the voltage to the bridge  $V_{BB}$ . The high-power diodes must handle the pulse current capacity to survive all of the drive current flowing through it until it decreases to zero.

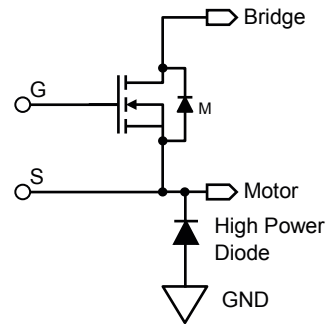
In the second case, the motor is connected to the source (see Figure 5). When the current is flowing from the bridge to the motor and the MOSFET is switch off, the motor inductance will try to force the voltage on the source pin down. This will draw current through the high-power diode from the ground. If the current is flowing from the motor to the bridge and the MOSFET is switched off, the motor inductance will force the voltage on the source pin up and the body diode will conduct. If the bridge is still on, the current will come from the ground, or if it is off, the current will come from the bridge high-side body diode. The high-power diodes must handle the pulse current capacity to survive all of the drive current flowing through it until it decreases to zero.

The third case—and the recommended method (see Figure 6)—allows the recirculation current to be dissipated in the external MOSFETs. This also has the advantage that there is no direct connection to the supply other than through the external MOSFETs and the bridge. When the current is flowing from the bridge to the motor and the MOSFET is switched off, the motor inductance will try to force the voltage on the source pin down. This will drop the voltage on the source to  $-4\text{ V}$  and the gate will be held at  $-1\text{ V}$  by

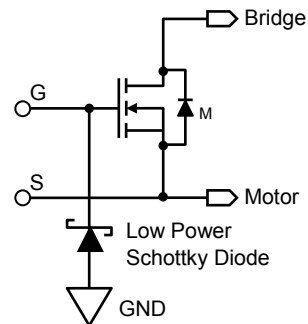
the Schottky diode. This will turn on the external MOSFET enough to draw current through the MOSFET. If the bridge is still on, current will come from the positive supply, or if it is off, the current will come from the bridge low-side body diode. If the current is flowing from the motor to the bridge and the MOSFET is switched off, the motor inductance will force the voltage on the source pin up and the body diode will conduct. If the bridge is still on, the current will come from the ground, or if it is off, the current will come from the bridge high-side body diode.



**Figure 4: Source to Bridge, Drain Diode**



**Figure 5: Source to Motor, Source Diode**



**Figure 6: Source to Motor, Gate Diode**

## Logic Control Inputs

A single digital terminal, ENA, controls all three gate drives. When ENA is high, all gate drive outputs will be on. When ENA is driven low, all gate drive outputs will be off. An internal open-drain output is connected to the ENA terminal. This will pull the ENA terminal to a regulated low voltage to indicate the status of the internal charge pump regulator. This terminal can be shorted to VBB without damage.

**Table 1: Logic Truth Table**

ENA	IG	POK	Pump	Gate Drive
0	1	1	Active	Off
1	1	1	Active	On
X	0	1	Disabled	Off
X	1	0	Disabled	Off
X	0	0	Disabled	Off

The two activation inputs, POK and IG, must both be high before the A6862 is activated with the charge pump operating. These two inputs can be driven by logic-level signals or connected directly to other systems supplies including the main battery supply through an external reverse protection diode. Typically, these would be connected to the logic supply or logic supply monitor and to the switched battery supply (ignition signal).

When either POK or IG is low, the charge pump will be disabled, and the outputs will be off. This provides additional security in the case of a supply failure. When the charge pump is disabled, the supply current drawn by the A6862 will reduce to a very low level and it will be in a low-power sleep mode.

## Charge Pump Output Monitor

The A6862 includes undervoltage detection on the charge pump output. If the voltage at the charge pump output,  $V_{CP}$ , drops below the undervoltage threshold,  $V_{CPON}$ , then a timer is started. If  $V_{CP}$  remains below  $V_{CPON}$  for the duration of the VCP undervoltage filter time,  $t_{CPUV}$ , then a VCP undervoltage condition (VCPU) will be asserted. The ENA input will be pulled to  $V_{OLF}$ , but the device stays in the on-state.

This feature also allows the controller to actively determine the delay between power-on and the time the outputs should be activated.

## Gate Drive Output Monitor

The gate-source voltage between the Gx terminal and the Sx terminal, for each phase, is monitored for an undervoltage condition. If the voltage between the gate and source of any active gate drive output,  $V_{GSx}$ , drops below the VGS undervoltage threshold,  $V_{GSUV}$ , then a timer is started. If  $V_{GSx}$  remains below  $V_{GSUV}$  for the duration of the VGS undervoltage filter time,  $t_{GSUV}$ , then the ENA input will be pulled to  $V_{OLF}$ , but all gate drive outputs will remain in the on-state. The ENA will remain at  $V_{OLF}$  until  $V_{GSx}$  rises above the undervoltage threshold  $V_{GSUV}$ .

The status of the charge pump output voltage monitor and the VGS undervoltage monitors can be checked using the ENA terminal. To use this feature, the ENA terminal should be driven with an active open-drain pull-down and a passive pull-up resistor. When no undervoltage states are present, the voltage at ENA is determined by the digital voltage on the pull-up resistor and the control signal (DIS) applied to the ENA terminal.

When any VGS undervoltage condition ( $V_{GSUX}$ ) is present, then ENA will be pulled to  $V_{OLF}$  and can be recognized as a logic low by the controller. The controller can then decide whether to hold the outputs in this state or to switch off the outputs by asserting the control signal (DIS).

A typical connection arrangement to use this feature is shown in Figure 7 and Figure 8 and a representative sequence shown in Figure 9.

The arrangement permits three specific states (see Figure 7):

ON	Gate drive commanded on. No fault indicated. Gate drive on.
FAULT	Gate drive commanded on. Fault indicated. Gate drive on.
OFF	Gate drive commanded off. No fault indication. Gate drive off.

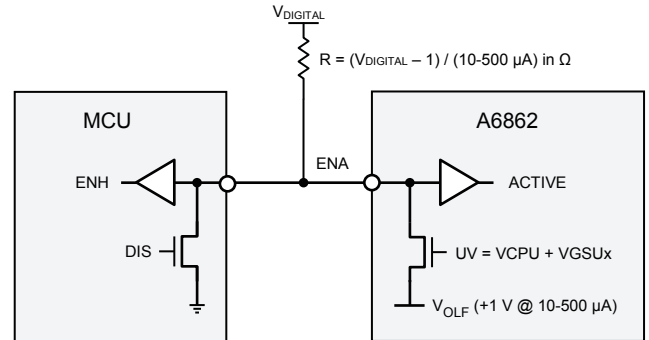
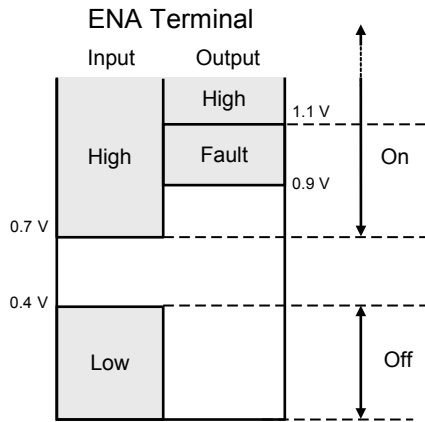


Figure 7: ENA Terminal Input and Output Levels

Figure 8: ENA Connection

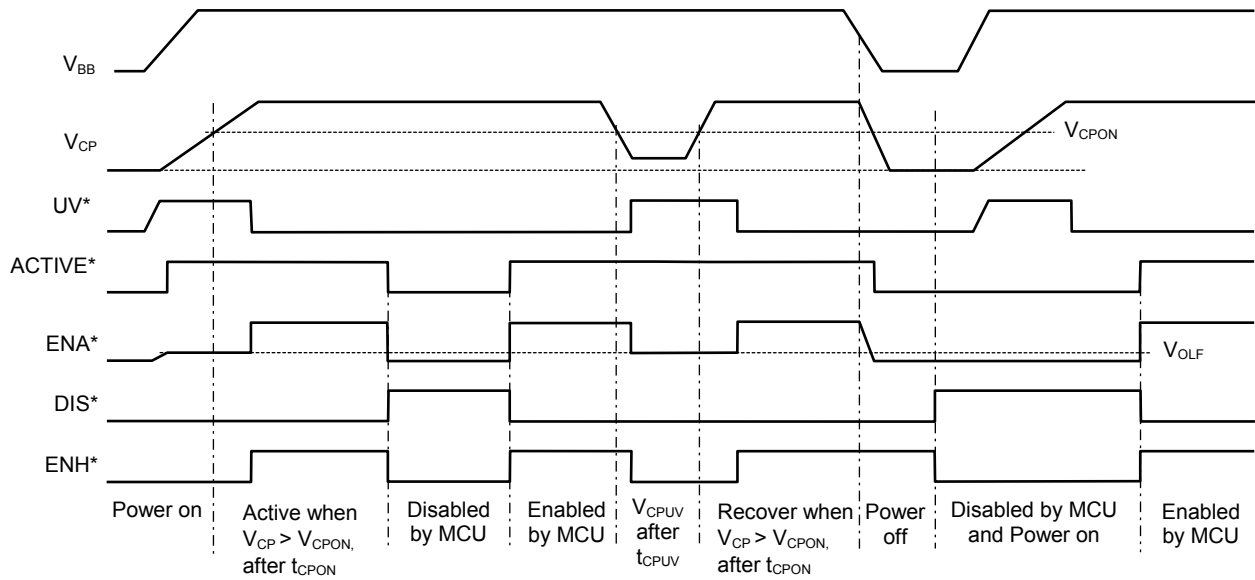
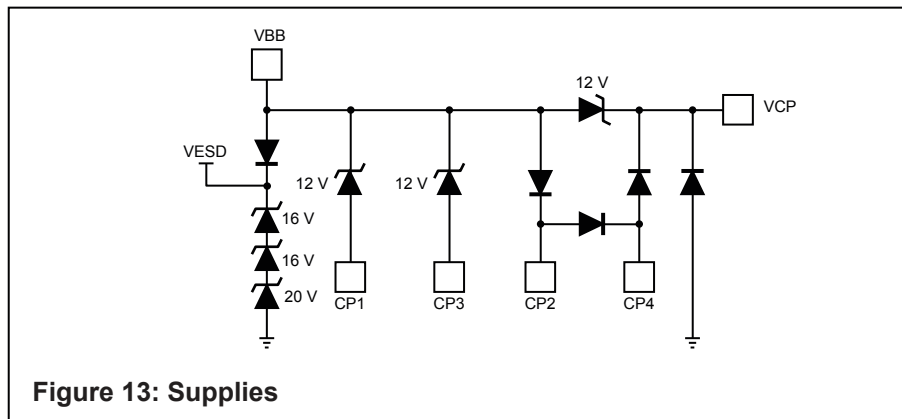
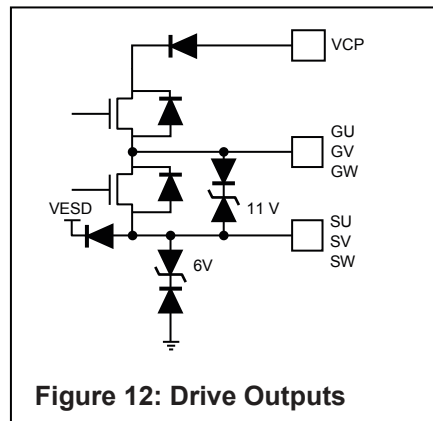
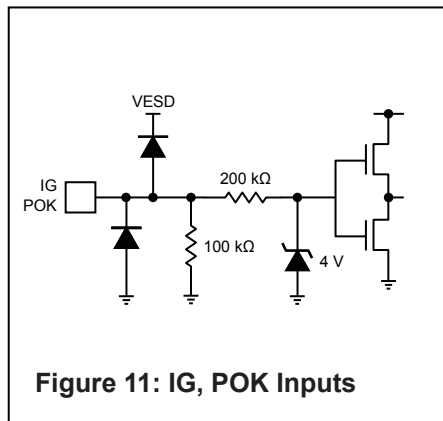
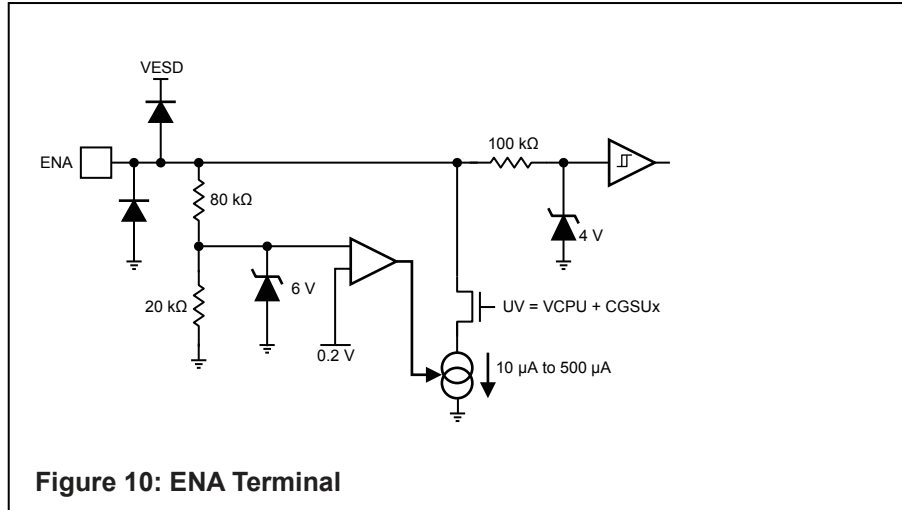


Figure 9: ENA Signal Sequence

\* For signals, see Figure 8

INPUT AND OUTPUT STRUCTURES



PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)

Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

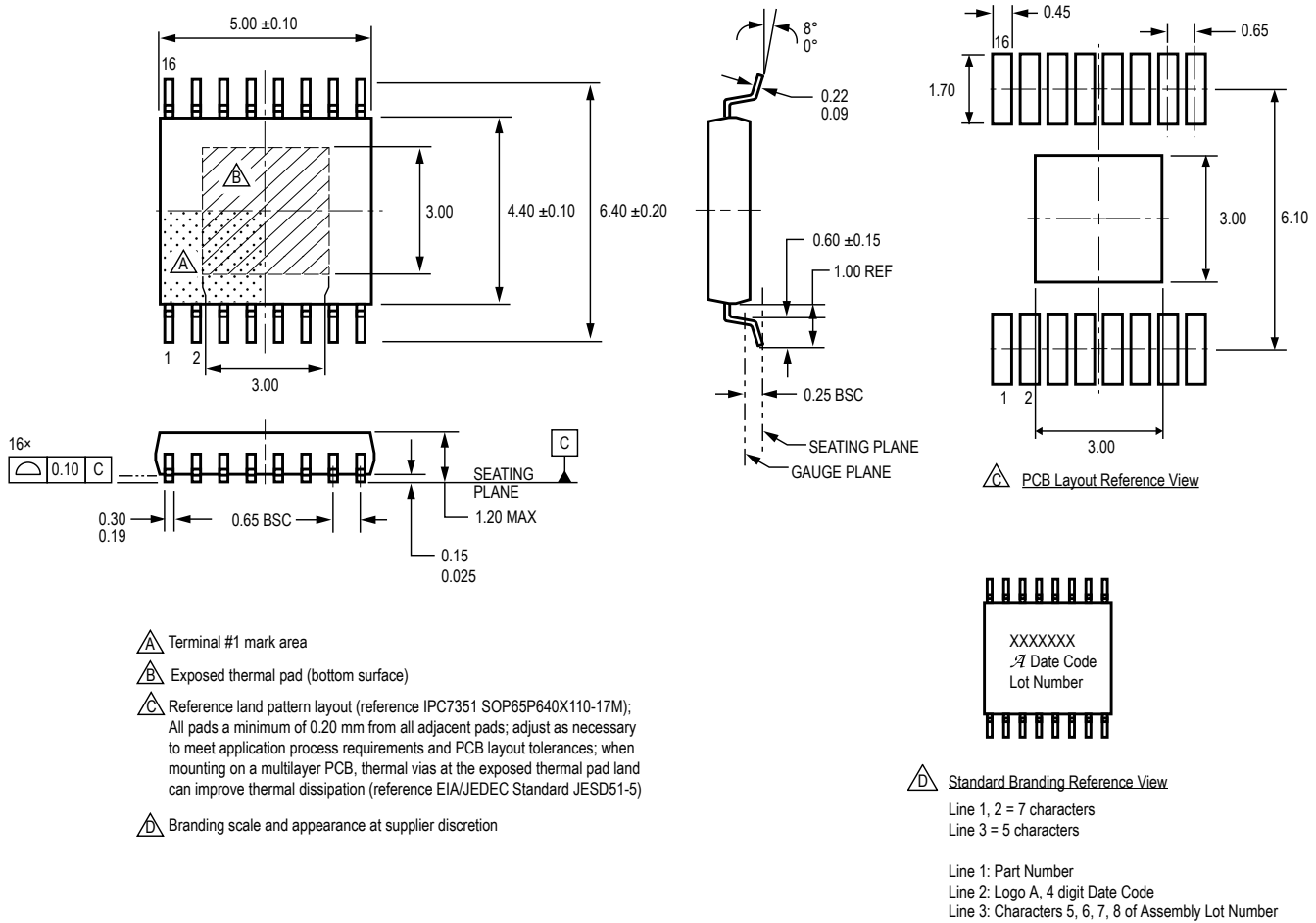


Figure 14: LP Package, 16-Lead TSSOP with Exposed Pad

**Revision History**

Number	Date	Description
–	September 23, 2016	Initial release
1	August 25, 2017	Corrected Turn-Off Time symbol (page 5), Figure 1 (page 6), and Figure 3 (page 8)
2	March 15, 2019	Updated $V_{SX}$ rating (page 2)
3	April 3, 2020	Minor editorial updates
4	April 13, 2022	Updated package drawing (page 13)

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