XN01119 (XN1119)

Silicon PNP epitaxial planar type

For switching/digital circuits

■ Features

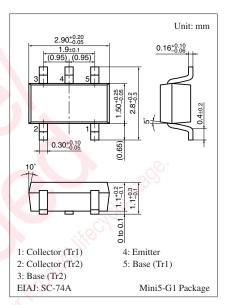
- Two elements incorporated into one package (Emitter-coupled transistors with built-in resistor)
- Reduction of the mounting area and assembly cost by one half

■ Basic Part Number

• UNR2119 (UN2119) × 2

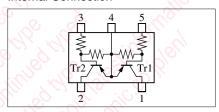
■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V_{CBO}	-50	V	
Collector-emitter voltage (Base open)	V _{CEO}	-50	V	
Collector current	I_{C}	-100	mA	
Total power dissipation	P_{T}	300	mW	
Junction temperature	T _j	150	°C	
Storage temperature	T _{stg}	-55 to +150	°C	



Marking Symbol: 7P

Internal Connection



■ Electrical Characteristics T_a = 25°C ± 3°C

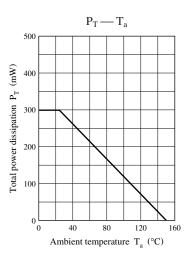
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = -10 \mu\text{A}, I_E = 0$	-50			V
Collector-emitter voltage (Base open)	V _{CEO}	$I_C = -2 \text{ mA}, I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = -50 \text{ V}, I_E = 0$			- 0.1	μΑ
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = -50 \text{ V}, I_B = 0$			- 0.5	μΑ
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = -6 \text{ V}, I_C = 0$			-1.5	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = -10 \text{ V}, I_{C} = -5 \text{ mA}$	30			_
h _{FE} Ratio *	h _{FE(Small}	$V_{CE} = -10 \text{ V}, I_{C} = -5 \text{ mA}$	0.50	0.99		_
	/Large)					
Collector-emitter saturation voltage	V _{CE(sat)}	$I_C = -10 \text{ mA}, I_B = -0.3 \text{ mA}$			- 0.25	V
Output voltage high-level	V _{OH}	$V_{CC} = -5 \text{ V}, V_B = -0.5 \text{ V}, R_L = 1 \text{ k}\Omega$	-4.9			V
Output voltage low-level	V _{OL}	$V_{CC} = -5 \text{ V}, V_B = -2.5 \text{ V}, R_L = 1 \text{ k}\Omega$			- 0.2	V
Input resistance	R ₁		-30%	1	+30%	kΩ
Resistance ratio	R ₁ / R ₂		0.08	0.10	0.12	_
Transition frequency	f_T	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}, f = 200 \text{ MHz}$		80		MHz

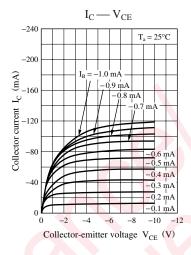
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

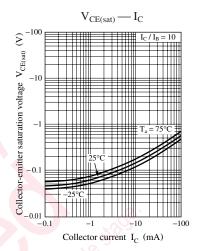
2. *: Ratio between 2 elements

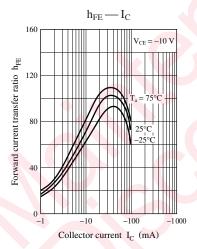
Note) The part number in the parenthesis shows conventional part number.

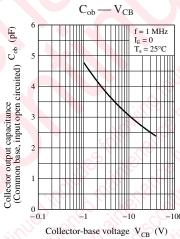
Panasonic

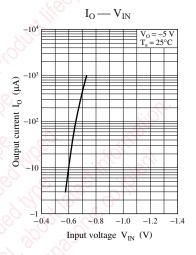


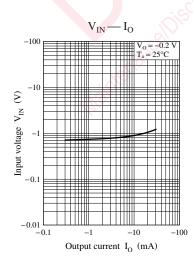












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