40V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_C = +25°C (Note 9)
40V	7.6mΩ @ V_{GS} = 10V	100A

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- Power managements
- DC-DC converters
- Motor controls

Features

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- Thermally Efficient Package – Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMTH4007SPSQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

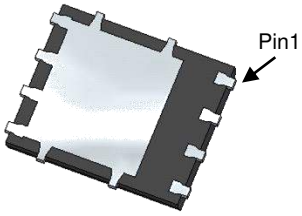
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

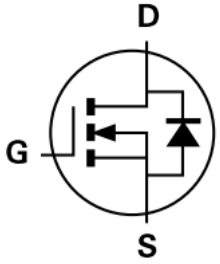
Site 1:

PowerDI5060-8

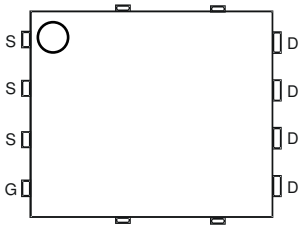
Top View



Bottom View



Internal Schematic

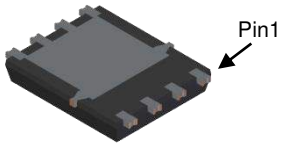


Top View
Pin Configuration

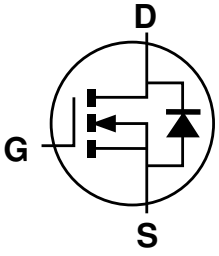
Site 2:

PowerDI5060-8/SWP (Type UX)

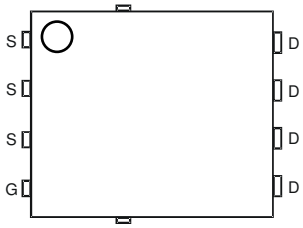
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

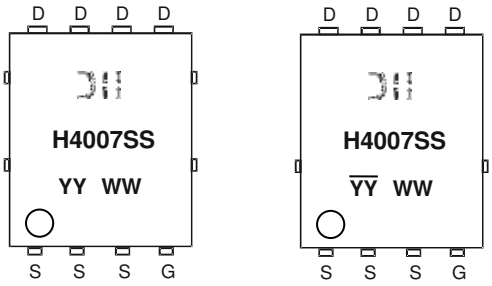
Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMTH4007SPSQ-13	PowerDI5060-8	2,500	Tape & Reel
DMTH4007SPSQ-13	PowerDI5060-8/SWP (Type UX)	2,500	Tape & Reel

Note: 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Code Marking
H4007SS = Product Type Marking Code
YYWW = Date Code Marking
YY or $\overline{YY}$ = Last Two Digits of Year (ex: 23 = 2023)
WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Note 5)	T_A = +25°C T_A = +70°C	I_D	15.7 13.1	A
Continuous Drain Current (Note 6)	T_C = +25°C (Note 9) T_C = +100°C	I_D	100 77	A
Maximum Continuous Body Diode Forward Current (Note 6)		I_S	100	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	120	A
Avalanche Current, L = 0.3mH		I_{AS}	20	A
Avalanche Energy, L = 0.3mH		E_{AS}	60	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	2.8	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	53	°C/W
Total Power Dissipation (Note 6)	T_C = +25°C	P_D	136	W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	1.1	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
6. Thermal resistance from junction to soldering point (on the exposed drain pad).
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.
9. Package limited.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage		BV_{DSS}	40	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	—	I_{DSS}	—	—	1	μA	V_{DS} = 32V, V_{GS} = 0V
	(Note 8)	I_{DSS}	—	—	100	μA	V_{DS} = 32V, V_{GS} = 0V, T_J = +125°C
Gate-Source Leakage		I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage		$V_{GS(TH)}$	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance		$R_{DS(ON)}$	—	4.9	7.6	mΩ	V_{GS} = 10V, I_D = 20A
Diode Forward Voltage		V_{SD}	—	—	1.2	V	V_{GS} = 0V, I_S = 20A
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance		C_{iss}	—	2,082	—	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz
Output Capacitance		C_{oss}	—	790	—		
Reverse Transfer Capacitance		C_{rss}	—	113	—		
Gate Resistance		R_g	0.1	0.46	1.4	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge		Q_g	—	41.9	—	nC	V_{DS} = 30V, I_D = 20A, V_{GS} = 10V
Gate-Source Charge		Q_{gs}	—	10	—		
Gate-Drain Charge		Q_{gd}	—	11.5	—		
Turn-On Delay Time		$t_{D(ON)}$	—	7	—	ns	V_{DD} = 30V, V_{GS} = 10V, I_D = 20A, R_G = 3Ω
Turn-On Rise Time		t_R	—	11.5	—		
Turn-Off Delay Time		$t_{D(OFF)}$	—	15.6	—		
Turn-Off Fall Time		t_F	—	8.8	—		
Body Diode Reverse Recovery Time		t_{RR}	—	29.9	—	ns	I_F = 20A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge		Q_{RR}	—	23	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

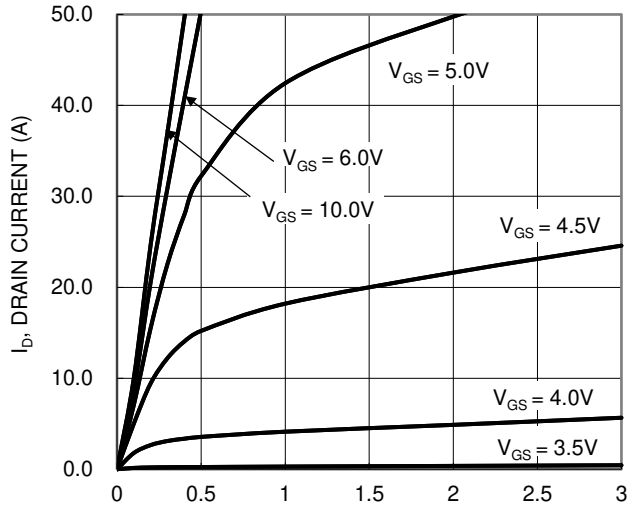


Figure 1. Typical Output Characteristic

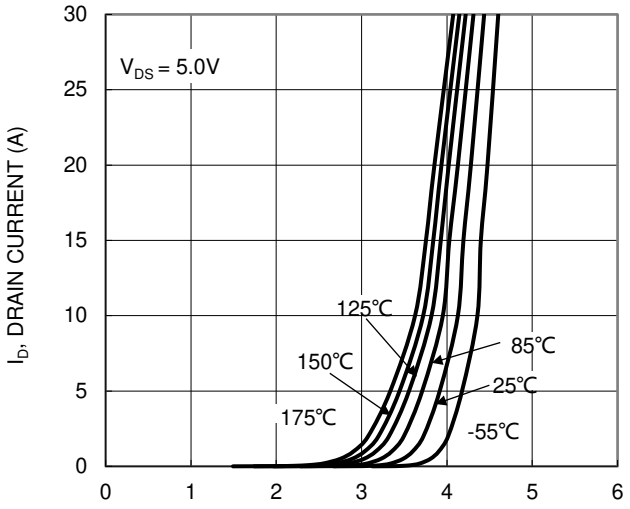


Figure 2. Typical Transfer Characteristic

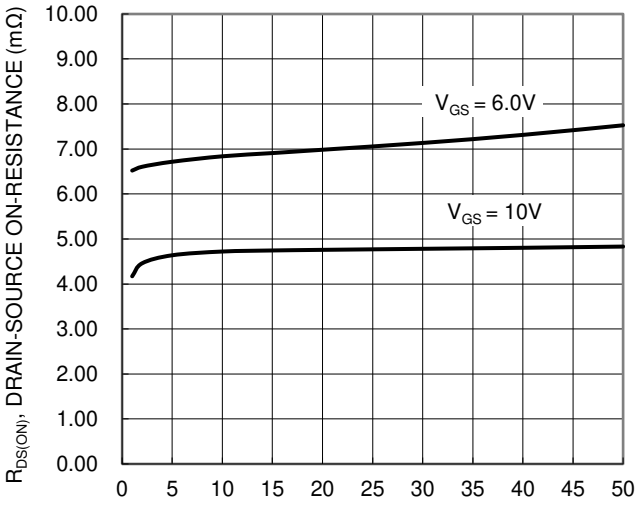


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

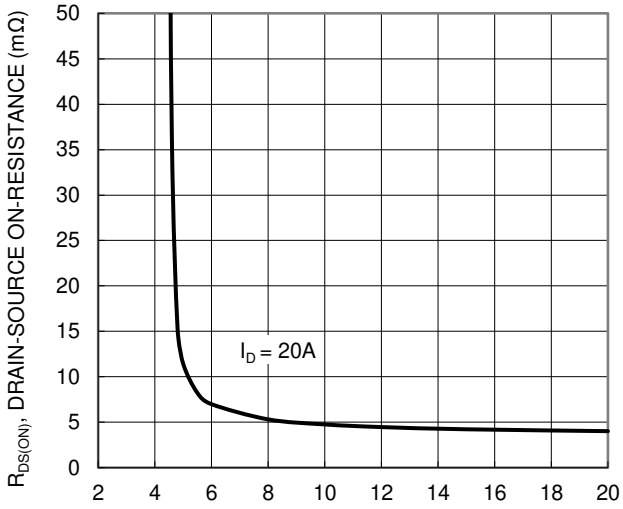


Figure 4. Typical Transfer Characteristic

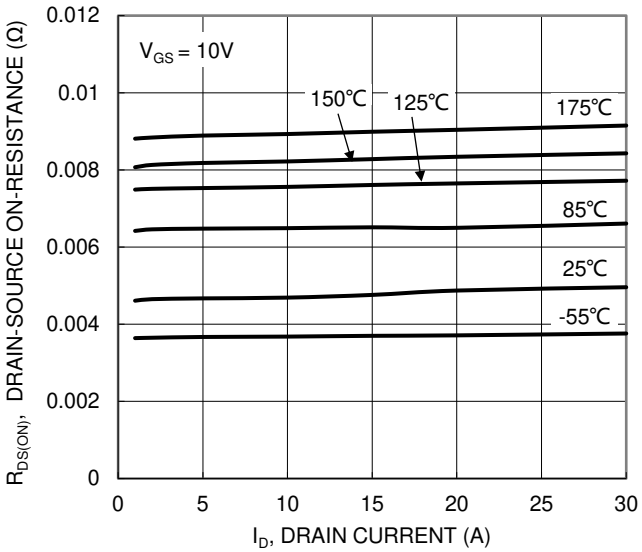


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

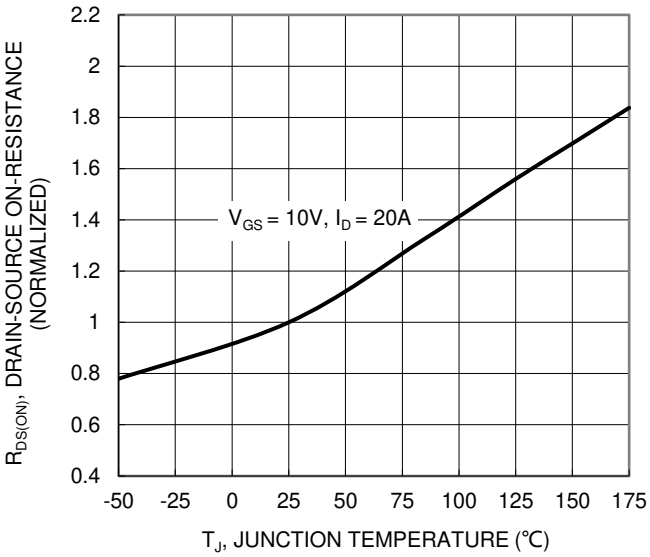


Figure 6. On-Resistance Variation with Temperature

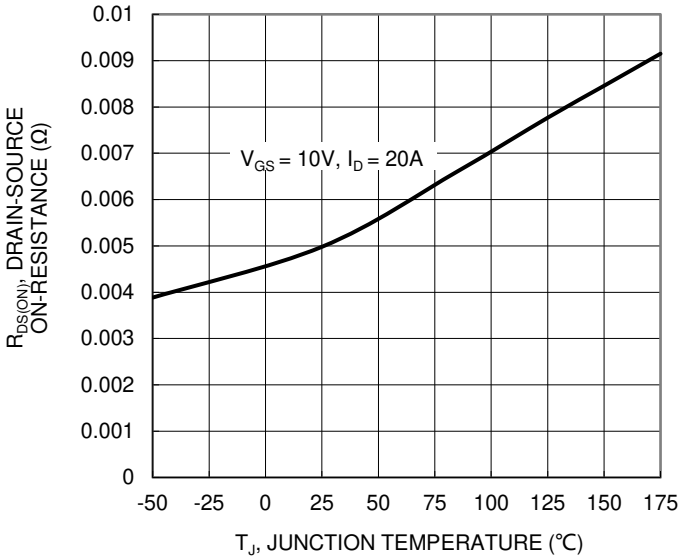


Figure 7. On-Resistance Variation with Temperature

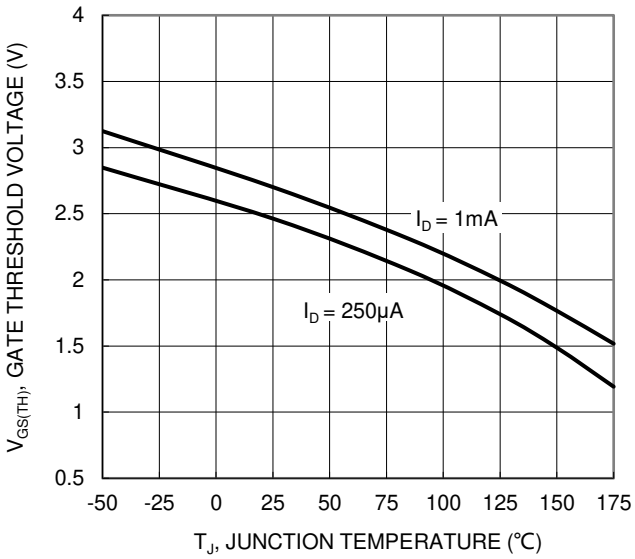


Figure 8. Gate Threshold Variation vs. Temperature

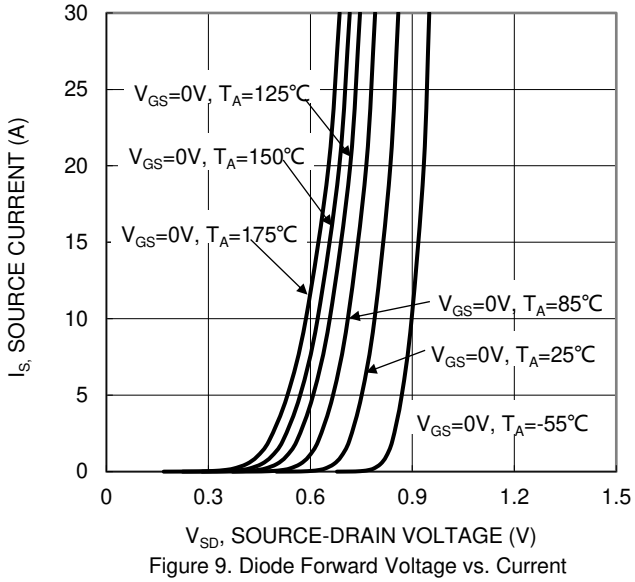


Figure 9. Diode Forward Voltage vs. Current

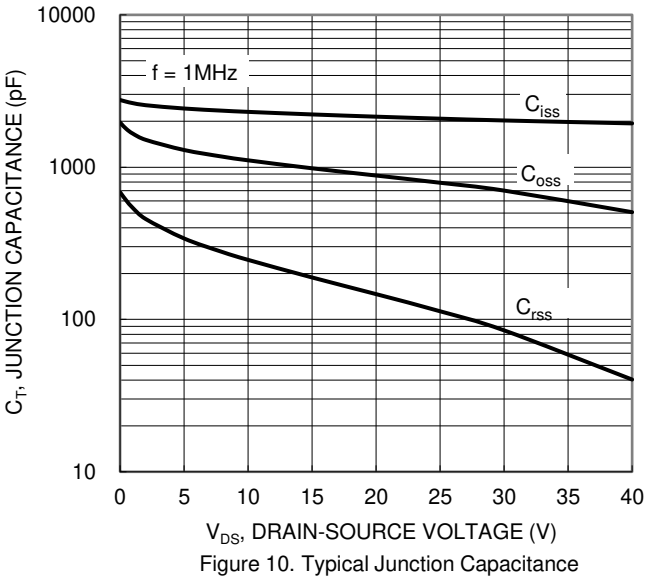


Figure 10. Typical Junction Capacitance

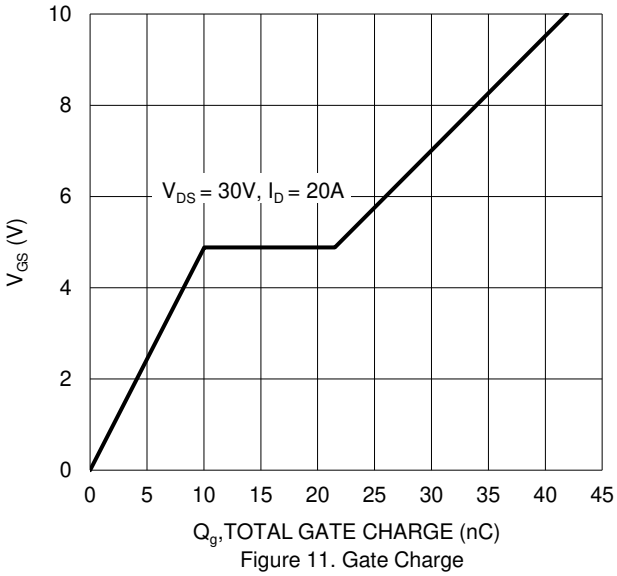


Figure 11. Gate Charge

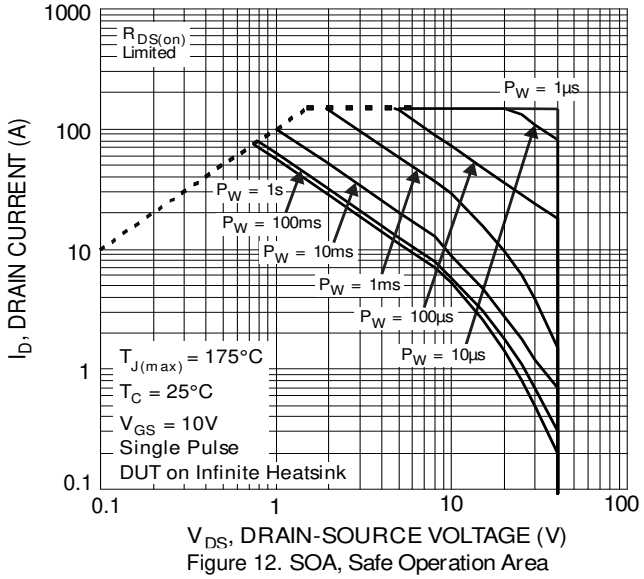


Figure 12. SOA, Safe Operation Area

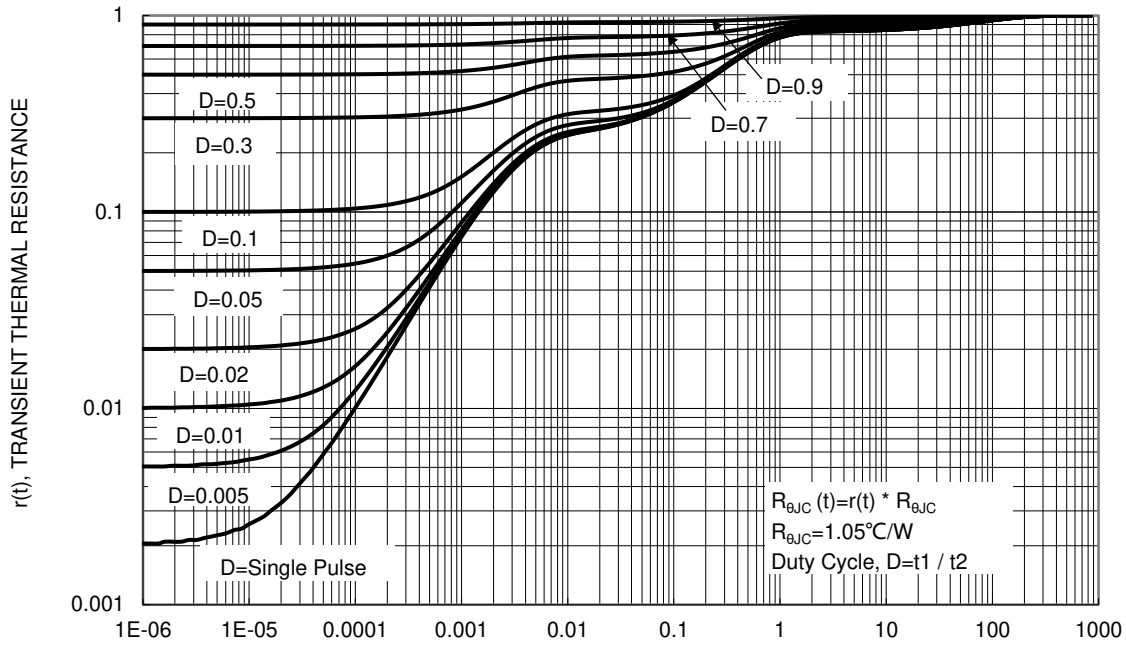


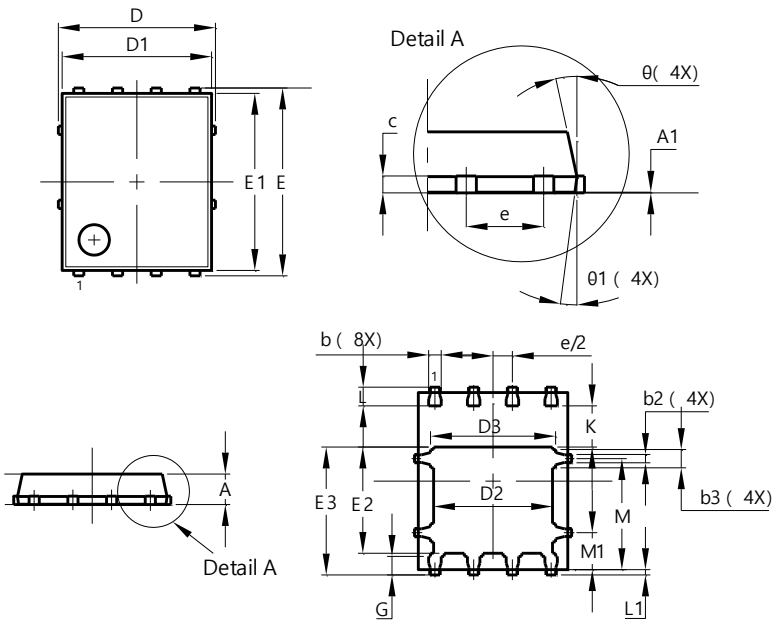
Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

Site 1:

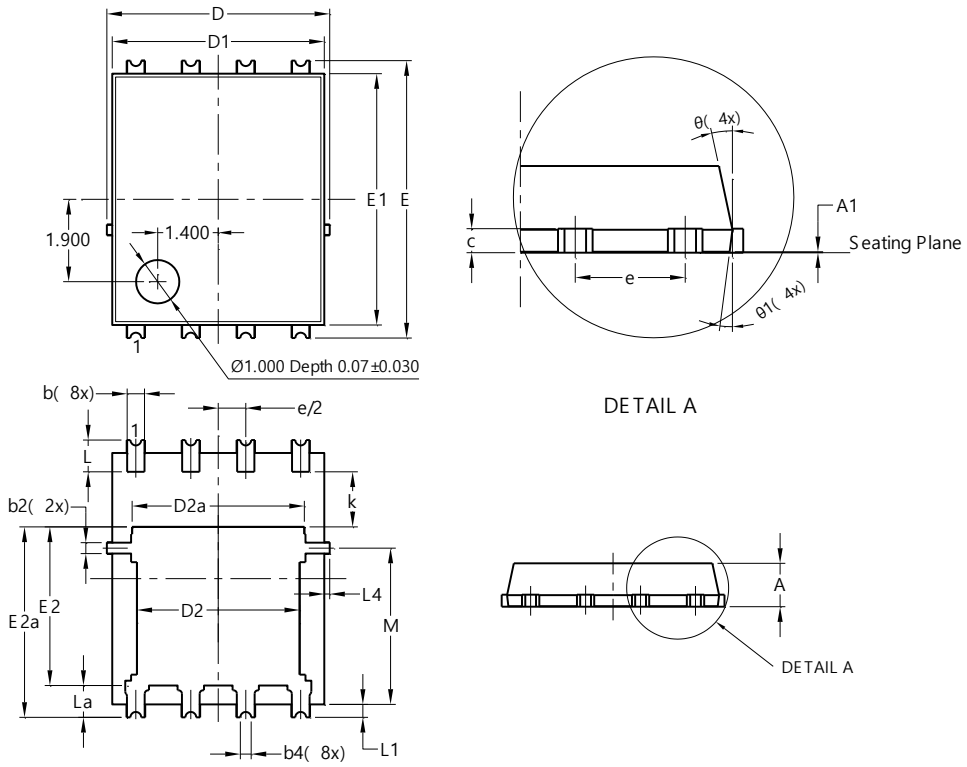
PowerDI5060-8



PowerDI5060-8			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	–
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	–	–
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Site 2:

PowerDI5060-8/SWP (Type UX)



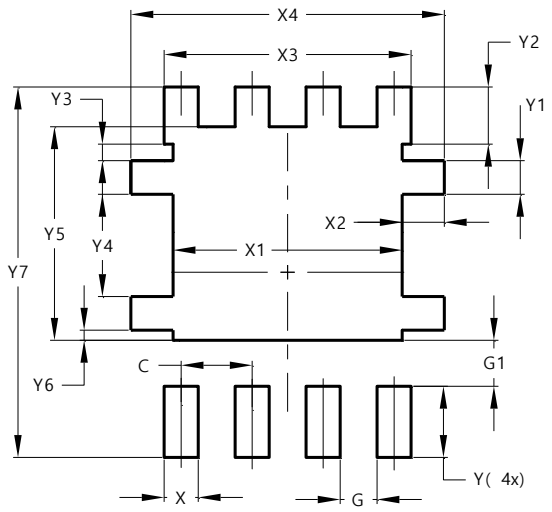
PowerDI5060-8/SWP (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

Site 1:

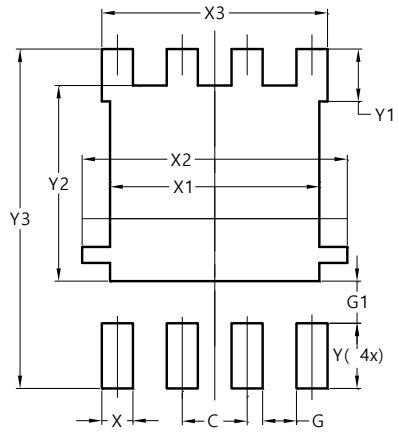
PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

Site 2:

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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