National Semiconductor

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CLC5644
Low Power, Low Cost, Quad Operational Amplifier

General Description

The CLC5644 is a quad, current feedback operational amplifier that is perfect for many cost sensitive applications that require high performance, especially when power dissipation is critical. Not only does the CLC5644 offer excellent economy in board space, but has an excellent performance vs power tradeoff which yields a 170MHz Small Signal Bandwidth while dissipating only 25mW. Applications requiring significant density of high speed devices such as video routers, matrix switches and high order active filters will benefit from the configuration of the CLC5644 and the low channel-to-channel crosstalk of 76dB at 1MHz.

The CLC5644 provides excellent performance for video applications. Differential gain and phase of 0.04% and 0.07˚ makes this device well suited for many professional composite video systems, but consumer applications will also be able to take advantage of these features due to the device's low cost. The CLC5644 offers superior dynamic performance with a small signal bandwidth of 170MHz and slew rate of 1000V/µs. These attributes are well suited for many component video applications such as driving RGB signals down significant lengths of cable. These and many other applications can also take advantage of the 0.1dB flatness to 25MHz.

Combining wide bandwidth with low cost makes the CLC5644 an attractive option for active filters. SAW filters are often used in IF filters in the 10's of MHz range, but higher order filters designed around a quad operational amplifier may offer an economical alternative to the typical SAW approach and offer greater freedom in the selection of filter parameters. National Semiconductor's Comlinear Products Group has published a wide array of literature on active filters and a list of these publications can be found on the last page of this datasheet.

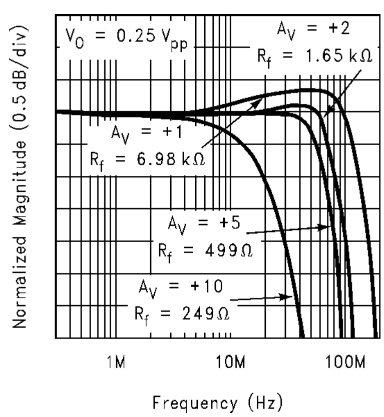
Features

- 170MHz small signal bandwidth
- 1000 V/us slew rate
- 2.5mA/channel supply current
- −72/−79dBc HD2/HD3 (5MHz)
- 0.04%, 0.07˚ differential gain, phase
- 70mA output current
- 16ns settling to 0.1%

Applications

- Portable equipment
- Video switchers & routers
- Video line driver
- Active filters
- IF amplifier
- Twisted pair driver/receiver

Non-Inverting Frequency Response



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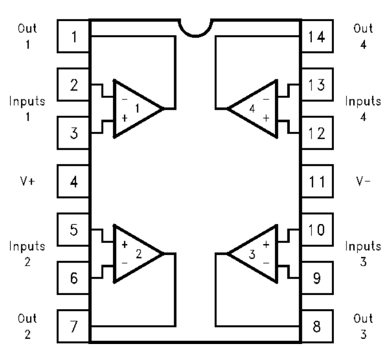
Connection Diagram



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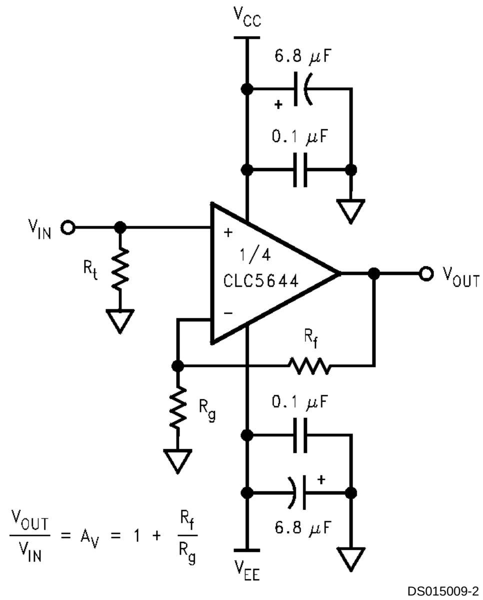
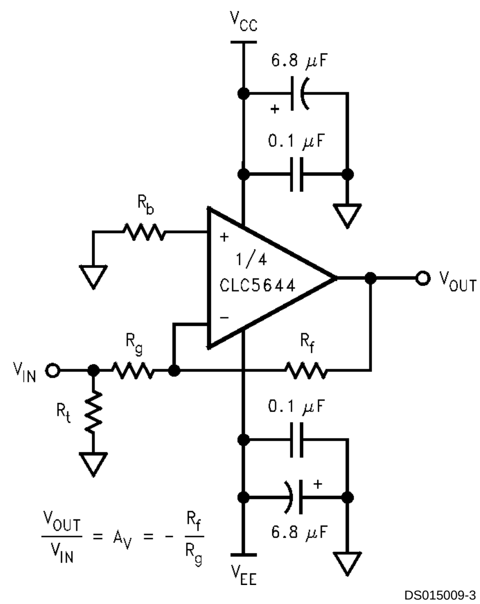
Pinout
DIP & SOIC

Typical Configurations



Non-Inverting Gain



Note: R_b provides DC bias for the non-inverting input. Select R_t to yield desired $R_{in} = R_t \parallel Rg$.

Inverting Gain

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-pin plastic DIP	−40˚C to +85˚C	CLC5644IN	CLC5644IN	N14A
14-pin plastic SOIC	−40˚C to +85˚C	CLC5644IM	CLC5644IM	M14A
		CLC5644IMX	CLC5644IM	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}-V_{EE})	+14V
Output Current	95mA
Common-Mode Input Voltage	V_{EE} to V_{CC}
Maximum Junction Temperature	+150˚C
Storage TemperatureRange	−65˚C to +150˚C
Lead Temperature (soldering 10 sec)	+300˚C

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	60˚C/W	110˚C/W
SOIC	55˚C/W	125˚C/W

Electrical Characteristics

(A_V = +2, R_f =1.65kΩ, R_L =100Ω, V_S = ±5V, unless specified)

Parameter	Conditions	Typ	Min/Max Ratings (Note 2)		Units
Ambient Temperature	CLC5644IN/IM	+25˚C	+25˚C	−40 to 85˚C	
Frequency Domain Response					
-3dB Bandwidth	A_V = 1	170	–	–	MHz
	V_O < 0.5V_{PP}	125	–	–	MHz
	V_O < 5V_{PP}	50	–	–	MHz
−0.1dB Bandwidth		25	–	–	MHz
Differential Gain	NTSC, R_L = 150Ω	0.04			dB
Differential Phase	NTSC, R_L = 150Ω	0.07			dB
Time Domain Response					
Rise and Fall Time	0.5V Step	2.7	–	–	ns
	5V Step	7	–	–	ns
Settling Time to 0.01%	1V Step	16	–	–	ns
Overshoot	0.5V Step	4	–	–	%
Slew Rate		1000	–	–	V/µs
Distortion And Noise Response					
2nd Harmonic Distortion	2V_{PP},1MHz	−72	–	–	dBc
3rd Harmonic Distortion	2V_{PP},1MHz	−79	–	–	dBc
Equivalent Input Noise					
Voltage (e_{ni})	>1MHz	4.5	–	–	nV/$\sqrt{Hz}$
Non-Inverting Current (i_{bn})	>1MHz	1.5	–	–	pA/$\sqrt{Hz}$
Inverting Current (i_{bi})	>1MHz	10	–	–	pA/$\sqrt{Hz}$
Crosstalk (Input Referred)	10MHz	76	–	–	dB
Static, DC Performance					
Input Offset Voltage (Note 3)		2.5	7	15	mV
Average Drift		25	–	90	µV/˚C
Input Bias Current (Non-Inverting)(Note 3)		2	6	10	µA
Average Drift		15	–	80	nA/˚C
Input Bias Current (Inverting)(Note 3)		2.5	7.5	22	µA
Average Drift		24	–	150	nA/˚C
Power Supply Rejection Ratio	DC	50	46	44	dB
Common Mode Rejection Ratio	DC	50	45	43	dB
Supply Current (per amplifier)(Note 3)	R_L = ∞	2.5	3	3	mA

Electrical Characteristics (Continued)

(A_V = +2, R_f =1.65kΩ, R_L =100Ω, V_S = ±5V, unless specified)

	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)		Units
Miscellaneous Performance						
	Input Resistance (Non-Inverting)		2	1	0.5	MΩ
	Input Capacitance (Non-Inverting)		1	2	2	pF
	Common-Mode Input Range		±2.2	±2.0	±1.4	V
	Output Voltage Range	R_L = 150Ω	±2.8	±2.6	±2.5	V
	Output Current		70	50	30	mA
	Output Resistance, Closed Loop	DC	0.2	0.3	0.6	mΩ

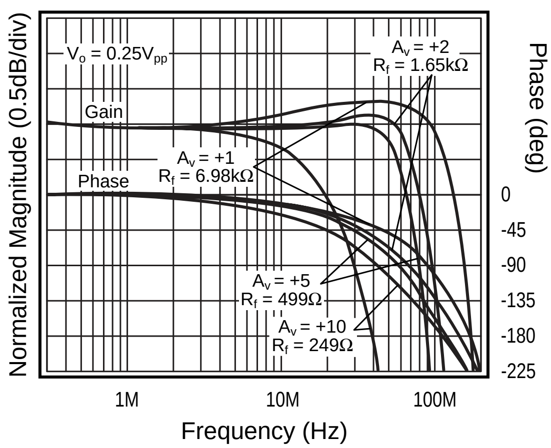
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25˚C.

Typical Performance Characteristics (A_V = +2, R_f = 1.65kΩ, R_L = 100Ω, V_S = +5V)

Non-Inverting Frequency Response



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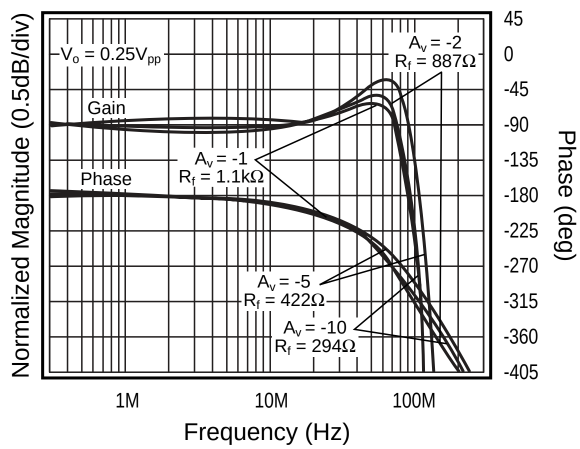
Inverting Frequency Response



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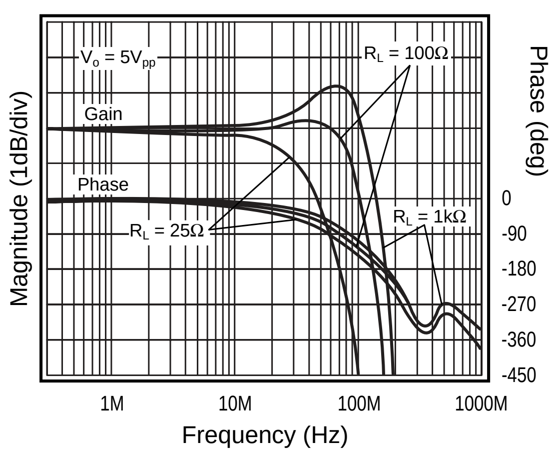
Frequency Response vs. R_L



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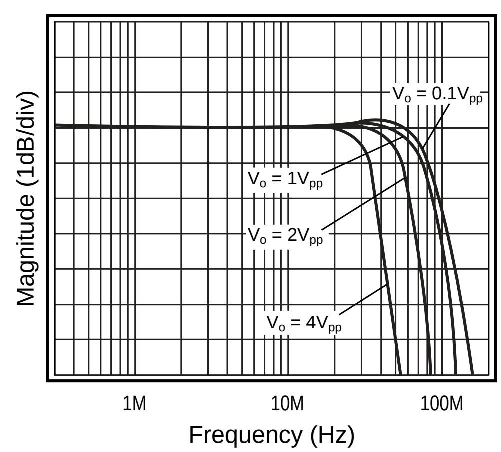
Frequency Response vs. V_O



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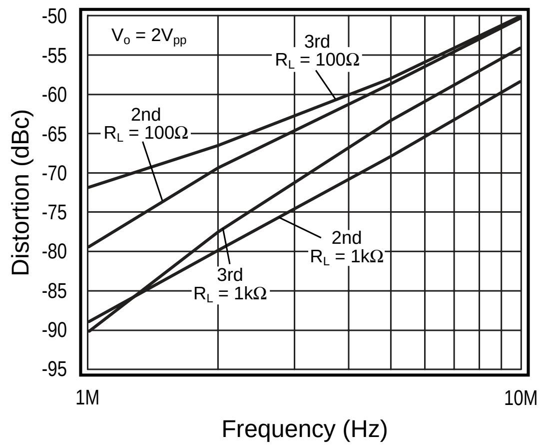
Typical Performance Characteristics (A_V = +2, R_f = 1.65kΩ, R_L = 100Ω, V_S = +5V) (Continued)

2nd & 3rd Harmonic Distortion



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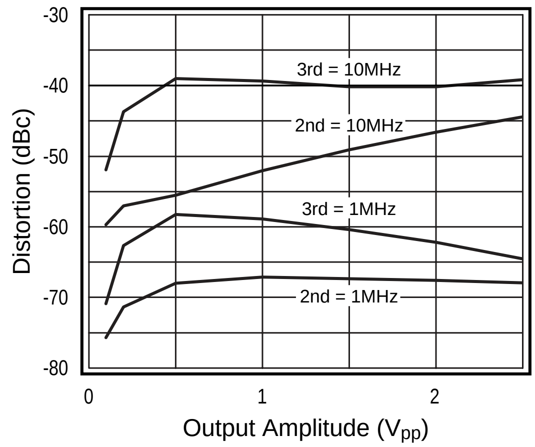
2nd & 3rd Harmonic Distortion, R_L = 25Ω



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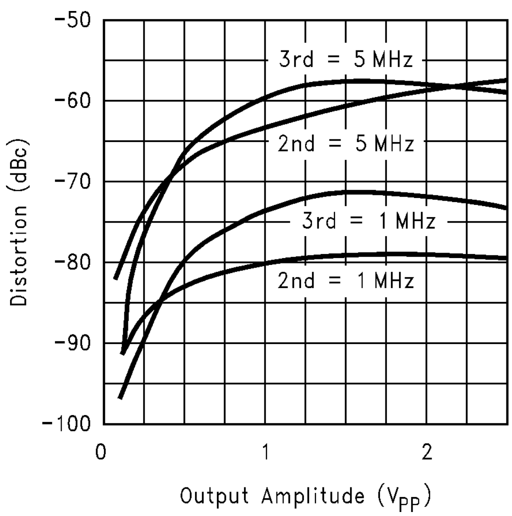
2nd & 3rd Harmonic Distortion, R_L = 100Ω



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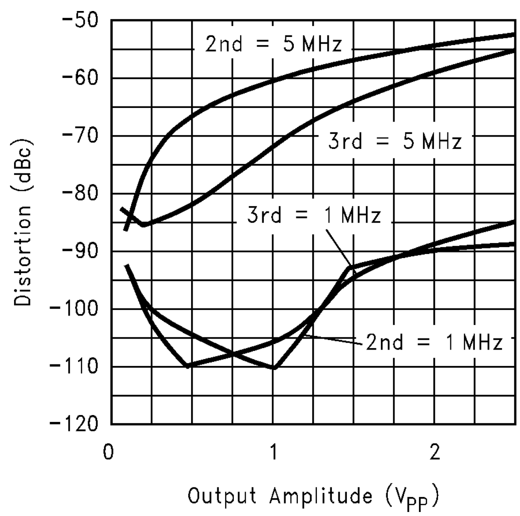
2nd & 3rd Harmonic Distortion, R_L = 1kΩ



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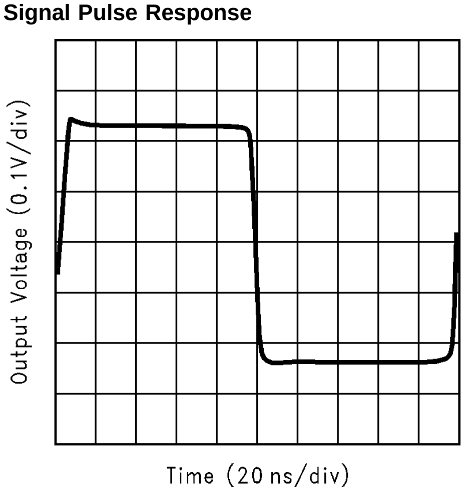
Small Signal Pulse Response



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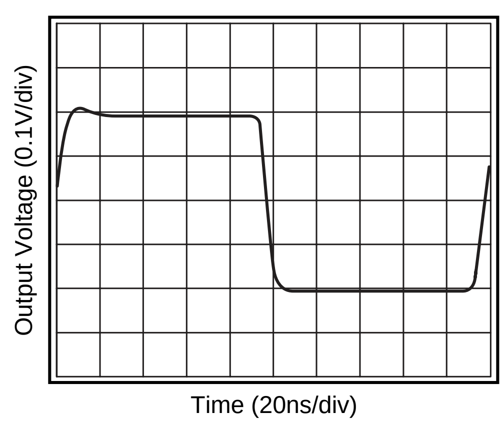
Large Signal Pulse Response



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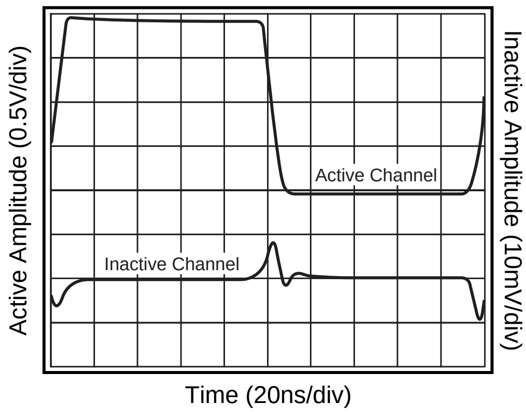
Typical Performance Characteristics (A_V = +2, R_f = 1.65kΩ, R_L = 100Ω, V_S = +5V) (Continued)

Most Susceptible Channel Pulse Coupling



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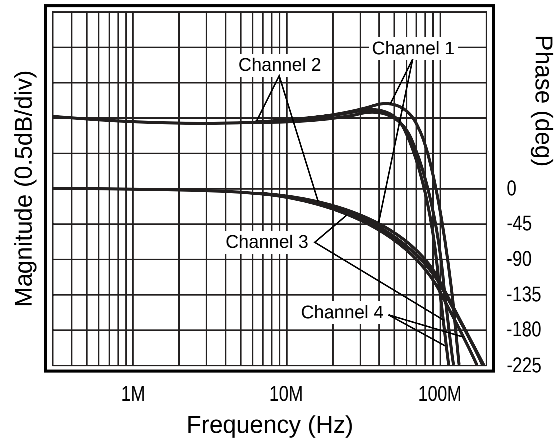
Channel to Channel Gain Matching



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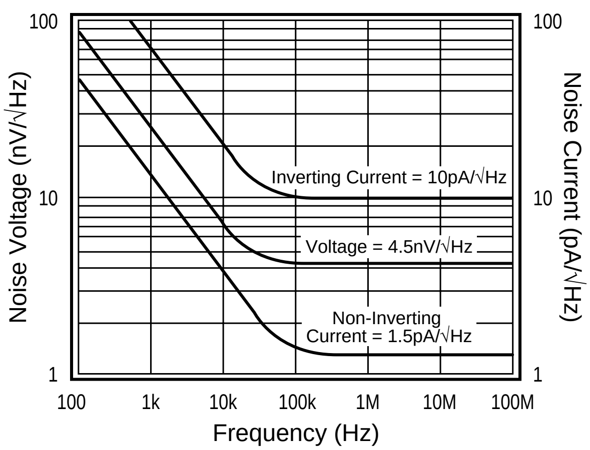
Equivalent Input Noise



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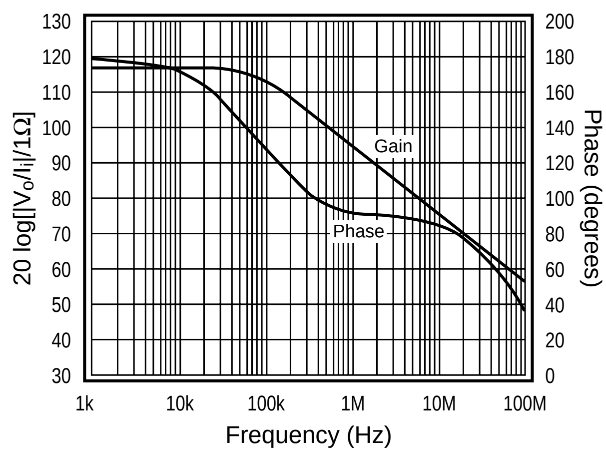
Open-Loop Transimpedance Gain, Z(s)



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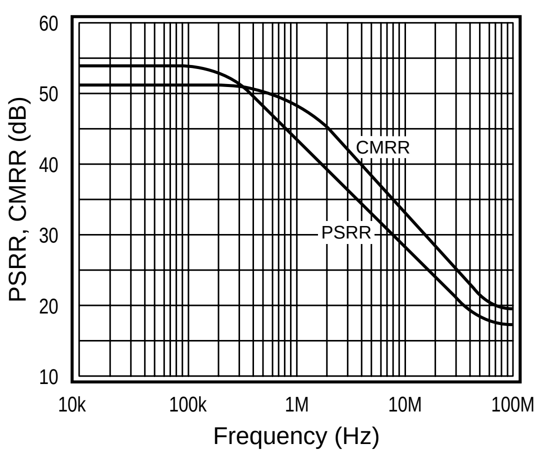
PSRR and CMRR



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Application Division

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with R_f
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_i} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \tag{1}$$

where:

A_v is the closed loop DC voltage gain

R_f is the feedback resistor

$Z(j\omega)$ is the open loop transimpedance gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the −3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC5644 (CLC730024-DIP, CLC730031-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization. General layout and supply bypassing play major roles in high frequency performance. Follow these steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prorotyping, never use high profile DIP sockets.

Active Filter Application Notes

OA-21 Simplified Component Pre-Distortion for High Speed Active Filters

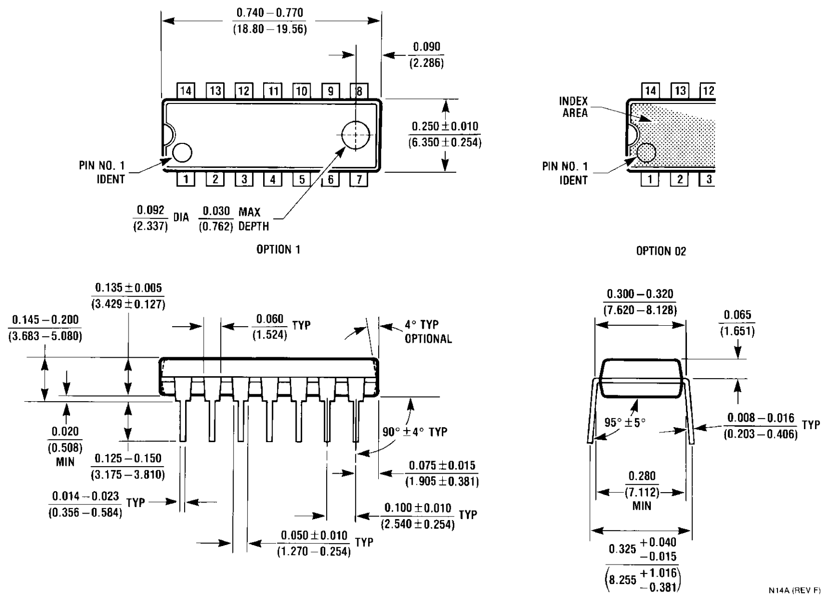
OA-26 Designing High-Speed Active Filters

OA-27 Low-Sensitivity, Lowpass Filter Design

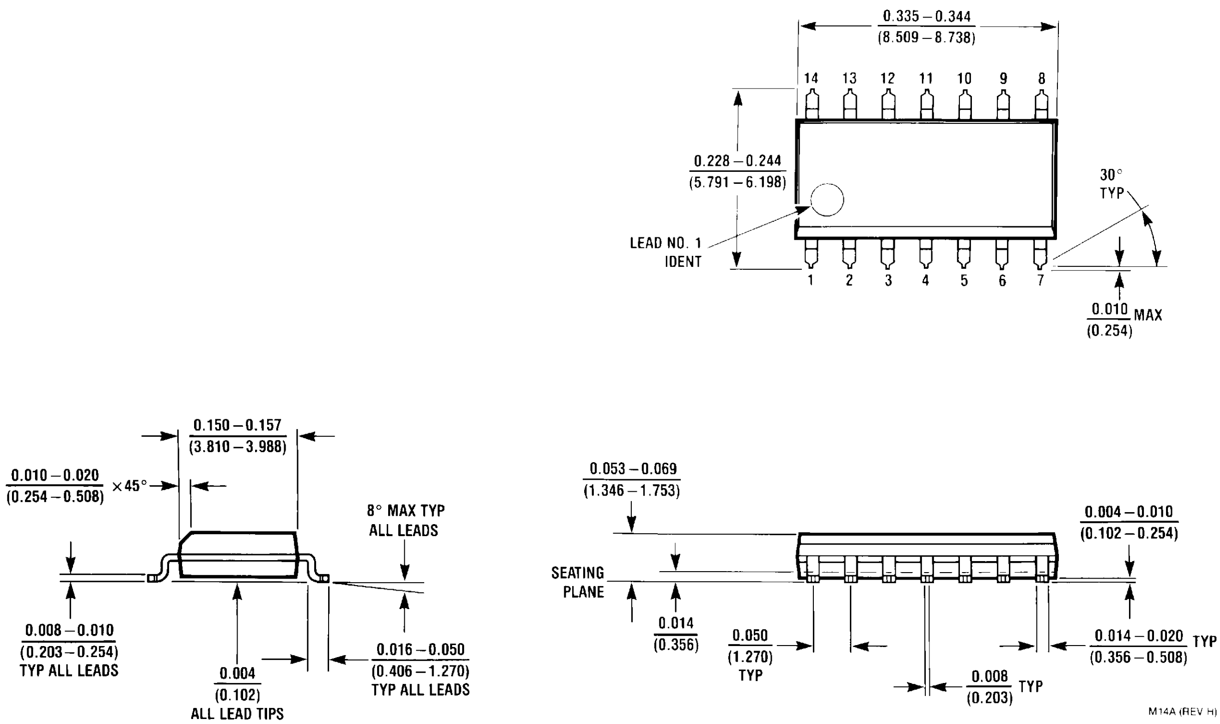
OA-28 Low-Sensitivity, Bandpass Filter Design with Tuning Method

OA-29 Low-Sensitivity, Highpass Filter Design with Parasitic Compensation

Physical Dimensions inches (millimeters) unless otherwise noted



14-Pin MDIP
NS Package Number N14A



14-Pin SOIC
NS Package Number M14A

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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