Wireless Power Receiver Compliant with WPC

General Description

The RT1650 is a wireless power receiver compliant with WPC V1.1 standard. The RT1650 integrates a synchronous full-bridge rectifier, a low dropout regulator, and a Micro Controller Unit (MCU) for control and communication. The device receives AC power from a WPC compatible wireless transmitter and provides output power up to 7.5W, which could be used as a power supply for a charger of mobile or consumer devices.

The MCU-based controller can support bi-direction channel communication including Frequency Shift Keying (FSK) demodulation for power signal from the transmitter and Amplitude Shift Keying (ASK) modulation for power signal to the transmitter. The RT1650 provides Foreign Object Detection (FOD) function to meet the requirement after WPC V1.1. It communicates with the transmitter for the received power to determine if a foreign object is present within the magnetic interface. This provides a higher level of safety.

The RT1650 provides a programmable dynamic rectifier voltage control function to improve power efficiency, a programmable power management control for maximum power delivery, a programmable current limit for suitable load setting, a programmable temperature setting with external NTC for thermoregulation, and proper protection functions such as UVLO, OVP, and OTP.

Features

- **Single-Chip WPC V1.1 Compliant Receiver**
- **Integrated Synchronous Rectifier Switch**
  - **Support Output Power up to 7.5W**
  - **High Rectifier Efficiency up to 96%**
  - **High System Efficiency up to 80%**
  - **Programmable Loading for Synchronous Rectifier Operation**
- **Programmable Dynamic Rectifier Voltage Control for Optimized Transient Response and Power Efficiency**
- **High Accurate Received Power Calculation for FOD Function**
  - **10-bit ADC for Voltage/Current Measurement**
  - **Coil Power Loss Modeling for Optimized Compensation**
  - **Adaptive Power Offset Compensation**
- **Low Quiescent Embedded 32-bit ARM Cortex-M0 MCU**
  - **32KB ROM/OTP, 1KB SRAM and 272B MTP**
  - **Easy Tuning for Communication and Control Parameters**
- **Support Bi-direction Channel Communication**
  - **FSK Demodulation for Power Signal from Wireless Power Transmitter**
  - **ASK Modulation for Power Signal to Wireless Power Transmitter**
- **Programmable Temperature Control**
- **Programmable Charge Status Packet**
- **Support Alignment with Transmitter**
- **Support Enable, Charge Complete and Fault Control Inputs**
- **Receiver Controlled EPT Packet**
- **Over Current Limit**
- **Over Voltage Protection**
- **Thermal Shutdown**
- **CSP 3.0mm x 3.4mm 48B (Pitch = 0.4mm)**
- **Low Profile (0.5mm Max.)**

Applications

- WPC Compliant Receivers
- Cell Phones & Smart Phones
- Digital Cameras
- Power Banks
- Wireless Power Embedded Batteries
- Headsets
- Portable Media Players
- Hand-held Devices

Ordering Information

RT1650 □
Package Type
WSC : WL-CSP-48B 3x3.4 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT1650
WSC
YMDNN
●

RT1650WSC : Product Number
YMDNN : Date Code

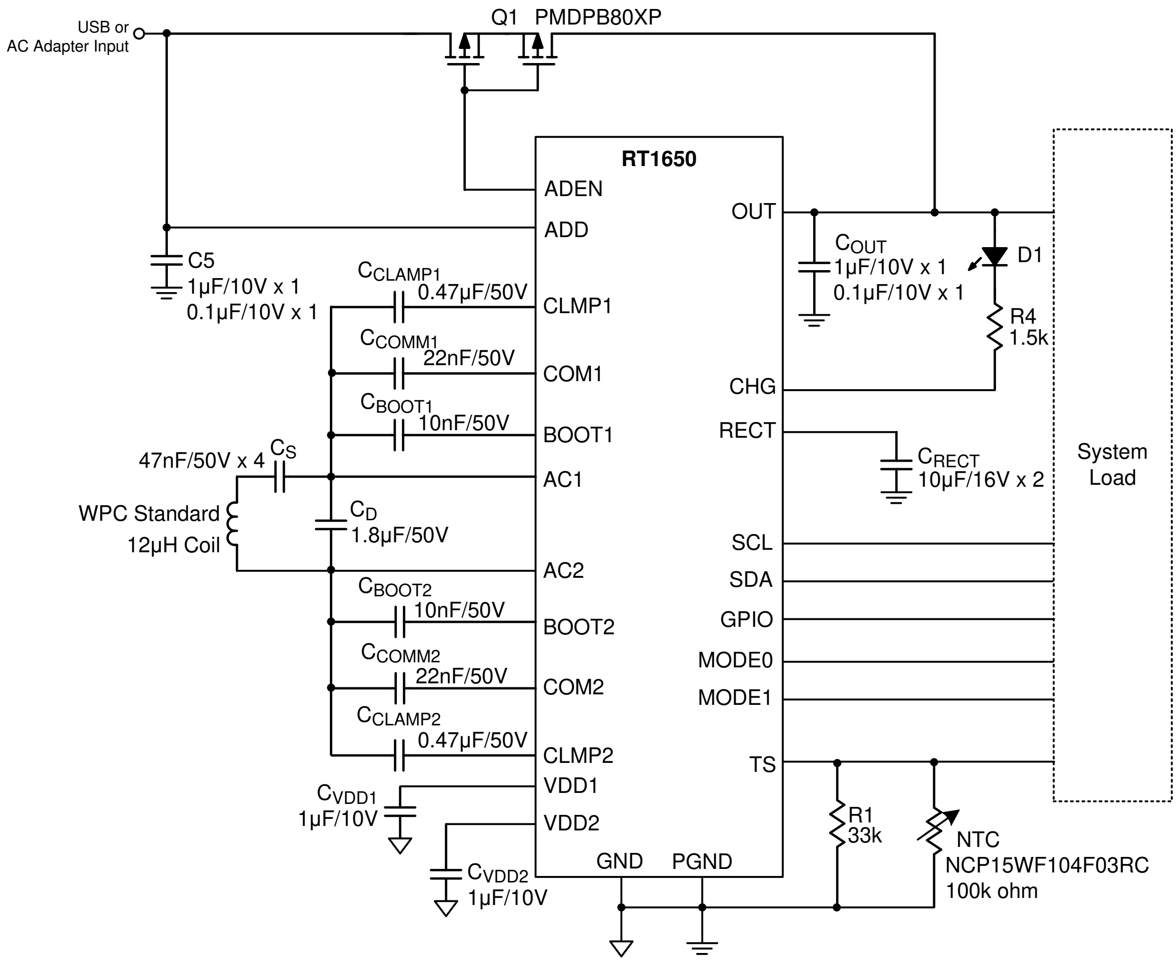
Pin Configurations

(TOP VIEW)

A1 BOOT2	A2 PGND	A3 PGND	A4 PGND	A5 PGND	A6 BOOT1
B1 AC2	B2 AC2	B3 AC2	B4 AC1	B5 AC1	B6 AC1
C1 RECT	C2 RECT	C3 RECT	C4 RECT	C5 RECT	C6 COM1
D1 OUT	D2 OUT	D3 OUT	D4 OUT	D5 OUT	D6 CLMP1
E1 GND	E2 NC	E3 NC	E4 VDD1	E5 VDD2	E6 COM2
F1 SCL	F2 SDA	F3 GPIO	F4 VDD1	F5 VDD2	F6 CLMP2
G1 TS	G2 MODE0	G3 MODE1	G4 NC	G5 NC	G6 PGND
H1 CHG	H2 ADEN	H3 ADD	H4 GND	H5 GND	H6 PGND

WL-CSP-48B 3x3.4 (BSC)

Typical Application Circuit



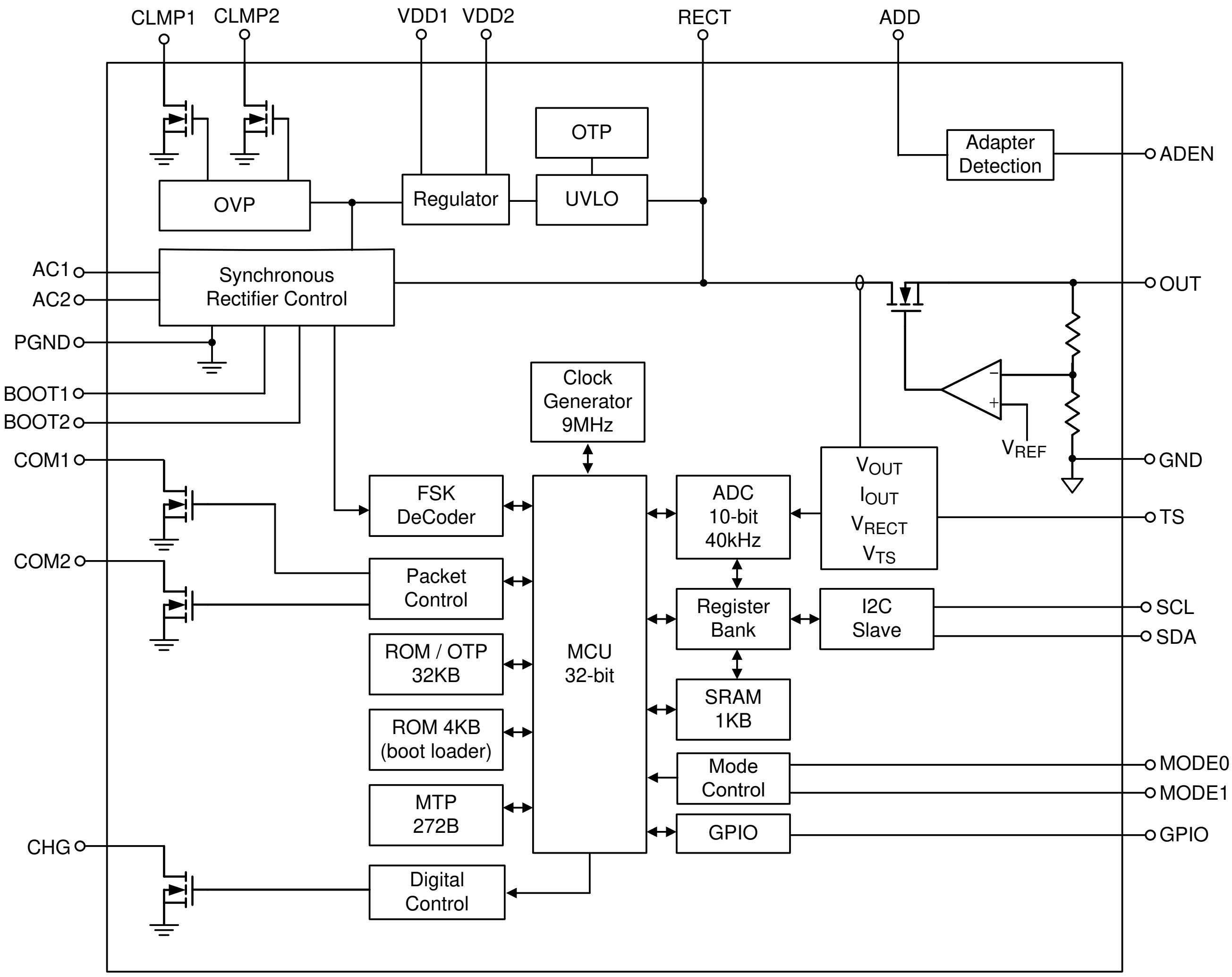
Note : The component value and the maximum voltage rating is based on the WPC standard transmitter and 5V adapter application. The customer should modify it depend on the different design and application.

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1	BOOT2	O	Bootstrap Supply for Driving the High-side FETs of Synchronous Rectifier. Connect a 10nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2.
A6	BOOT1	O	
A2 to A5 G6, H6	PGND		Power Ground.
B1 to B3	AC2	I	AC Power Input from Receiver Coil.
B4 to B6	AC1	I	
C1 to C5	RECT	O	Output of Synchronous Rectifier. Connect a ceramic capacitor (10μF to 22μF) between this pin to PGND.
C6	COM1	O	Open-Drain Output for Communication with Transmitter. Connect through a capacitor to AC1/AC2 for capacitive load modulation.
E6	COM2	O	
D1 to D5	OUT	O	Power Output of Regulator.

Pin No.	Pin Name	I/O	Pin Function
D6	CLMP1	O	Open Drain Output for Over-voltage Clamp Protection. Connect a 0.47μF ceramic capacitor between this pin to AC1/AC2. When the RECT voltage exceeds 11.5V, both switches will be turned on and the capacitors will act as a low impedance to protect the IC from damage.
F6	CLMP2	O	
E1, H4, H5	GND		Analog Ground.
E2, E3 G4, G5	NC		No Connection. Keep this pin as floating. Do not connect this pin to power input or ground.
E4, F4	VDD1	O	Voltage Supply for Internal Circuit. Connect a 1μF ceramic capacitor between this pin and GND.
E5, F5	VDD2	O	Voltage Supply for Internal Circuit. Connect a 1μF ceramic capacitor between this pin and GND.
F1	SCL	I	I^2C Compatible Series-Clock Input for internal register/MTP access.
F2	SDA	I/O	I^2C Compatible Series-Data Input/Output for internal register/MTP access.
F3	GPIO	I/O	General Purpose Input/Output.
H1	CHG	O	Open-Drain Indicator Output. When the output regulator is enabled, this pin is pulled to low.
H2	ADEN	O	Enable Control Output for External P-FET connecting ADD and OUT. This pin is pulled to the higher of OUT and ADD when turning off the external FET. This voltage tracks approximately 4V below ADD when voltage is present at ADD.
H3	ADD	I	Adapter Power Detection Input. Connect this pin to the adapter input. When a voltage is applied to this pin, wireless power is disabled and ADEN is pulled low. If not used, this pin should be connected to ground.
G1	TS	I	Temperature Sense Input. Connect a NTC between this pin and GND for temperature sensing. If the temperature sensing function is not desired, connect a 24kΩ resistor to GND. Host side can control this pin to send end power transfer (EPT) to the transmitter: pull-low for EPT fault; pull-up for EPT termination.
G2	MODE0	I	Operation Mode Control Input. These two pins are used to set power source operation mode. [MODE0, MODE1] = [0, 0]. Auto mode. Adapter power prior. [MODE0, MODE1] = [0, 1]. Wireless power mode. [MODE0, MODE1] = [1, 0]. Adapter power mode and OTG mode [MODE0, MODE1] = [1, 1]. Disable both adapter and wireless powers.
G3	MODE1	I	

Function Block Diagram



Operation

MCU Based Digital Circuit

RT1650 is a SoC (System on Chip) produce, which contains system level feature to control the communication with power transmitter, power calculation and GPIO. The firmware can be programmed into OTP (One Time Programmable) memory, so that user can discuss the features with RICHTEK, and custom some functions and GPIO behavior. To flexibly control whole functions, this chip embedded a MTP (Multiple Time Programmable) memory to save various setting and parameters. The external host can real-time read some power information via I^2C interface.

OVP (Over Voltage Protection)

The OVP function using to protect the abnormal power signal to let the RT1650 damaged. Once the VRECT exceeds 11.5V, this block will drive the CLAMP MOS to avoid the over voltage damage.

OTP (Over Temperature Protection)

The OTP function shuts down the linear regulator operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by around 20°C, the receiver will automatically resume operating.

Synchronous Rectifier Control

This block detect the zero-cross of the AC1 and AC2 voltage then control the high-side and low-side MOS of the rectifier. RT1650 provide the Asynchronous, Half-synchronous and Full-synchronous control to optimize the rectifier efficiency.

Mode Control

Mode control is using for the default mode, wireless mode, adapter mode and disable mode selection.

Adapter Detection

In the default mode and adapter mode, adapter detection block control the ADEN pin to follow the VADD-5V to avoid the PMOS damaged.

FSK Decoder

This block analysis the frequency from the AC1 and AC2. This information can use for the FSK (Frequency Shift Key) decode to the WPC medium power standard. This information also can use for the power loss calculation of the resonant tank.

Packet Control

This block build up the WPC standard 2kHz bi-phase encoding scheme with the asynchronous serial format and the packet structure. This block control the open-drain MOS to achieve the ASK (Amplitude Shift Key) communication.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, AC1, AC2, RECT, COM1, COM2, OUT, CHG, CLMP1, CLMP2 ------------- –0.3V to 20V
- Supply Input Voltage, ADD, ADEN --- –0.3V to 30V
- Supply Input Voltage, BOOT1, BOOT2 -- –0.3V to 26V
- Supply Input Voltage, VDD1, VDD2, SDA, SCL, GPIO, TS ----------------------------- –0.3V to 6V
- Input Current, AC1, AC2 --- 2A(rms)
- Output Current, OUT --- 2A
- Output Sink Current, CHG --- 15mA
- Output Sink Current, COM1, COM2 --- 1A
- Power Dissipation, P_D @ T_A = 25°C
- WL-CSP-48B 3x3.4 --- 3.67W
- Package Thermal Resistance (Note 2)
- WL-CSP-48B 3x3.4, θ_{JA} --- 27.2°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range --- –65°C to 150°C
- ESD Susceptibility (Note 3)
- HBM (Human Body Model) --- 2kV
- MM (Machine Model) --- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage Range, RECT --- 5V to 10V
- Input Current, RECT --- 1.5A
- Output Current, OUT --- 1.5A
- Sink Current, ADEN --- 1mA
- Sink Current, COM -- 500mA
- Ambient Temperature Range --- –40°C to 85°C
- Junction Temperature Range -- –40°C to 125°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
RECT Under-voltage Lockout Threshold	V_{RECT_UVLO}	V_{RECT} Rising : 0V → 3V	2.6	2.7	2.8	V
RECT UVLO Hysteresis		V_{RECT} Falling : 3V → 0V	--	250	--	mV
RECT Over-Voltage Threshold	V_{RECT_OVP}	V_{RECT} Rising : 7V → 13V	11	11.5	12	V
RECT Over-Voltage Hysteresis		V_{RECT} Falling : 13V → 7V	--	150	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dynamic V_{RECT} Setting-1	V_{RECT_SET1}	(Note 5)	--	7	--	V
Dynamic V_{RECT} Setting-2	V_{RECT_SET2}	(Note 5)	--	6.3	--	
Dynamic V_{RECT} Setting-3	V_{RECT_SET3}	(Note 5)	--	5.8	--	
Dynamic V_{RECT} Setting-4	V_{RECT_SET4}	(Note 5)	--	5.3	--	V
I_{OUT} Hysteresis for Dynamic V_{RECT} Settings	$I_{OUT\_TH\_HYS}$	(Note 5)	--	5	--	%
RECT Quiescent Current	I_Q		--	8	--	mA
Regulator Output						
OUT Regulation Voltage	V_{OUT_REG}	I_{OUT} = 1mA	4.95	5	5.05	V
		I_{OUT} = 1A	4.94	4.99	5.04	
		I_{OUT} = 1.5A	4.90	4.96	5.02	
Regulator Drop-out Voltage	V_{DROP}	V_{RECT} –V_{OUT}, I_{OUT} = 1A	--	100	200	mV
Output Current Limit Tolerance	I_{OUT_LIMIT}	I_{OUT} =1.5A	–10	-	10	%
OUT Leakage Current	I_{OUT_LKG}	Disabled, V_{OUT} = 5V	--	40	--	μA
Synchronous Rectifier						
Programmable I_{OUT} Threshold Range to Enable Half-Synchronous Rectifier	I_{SR_TH}	I_{OUT} Rising (Note 5)	50	--	500	mA
Programmable I_{OUT} Threshold Range to Enable Full-Synchronous Rectifier		I_{OUT} Rising (Note 5)	150	--	750	
Programmable I_{OUT} Hysteresis Range		I_{OUT} Falling (Note 5)	25	--	100	
Rectifier Diode Voltage in Asynchronous Mode	V_{DIODE}	$I_{AC-VRECT}$ = 250mA	--	0.65	--	V
TS Sense/Control Input						
TS Thermoregulation Threshold	V_{TS_REG}	V_{TS} Falling (Note 5)	--	786	--	mV
Too-Hot Protection Threshold	V_{TS_HOT}	V_{TS} Falling (Note 5)	--	278	--	mV
Too-Cold Protection Threshold	V_{TS_COLD}	V_{TS} Rising (Note 5)	--	1.82	--	V
TS Output Current	I_{TS}		--	60	--	μA
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_J	(Note 5)	--	150	--	°C
Over-Temperature Protection Hysteresis		(Note 5)	--	20	--	
CHG Indicator Output						
CHG Low-Level Output Voltage	V_{CHG_L}	I_{SINK} = 5mA	--	--	100	mV
CHG Leakage Current when disabled	I_{CHG_LKG}	V_{CHG} = 20V	--	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
COM Outputs						
COM1, COM2 N-FET On-Resistance	R_{ON_COM}	V_{RECT} = 2.6V	--	0.7	--	Ω
COM1, COM2 Signaling Frequency	f_{COM}		--	2	--	kHz
COM1, COM2 Leakage Current	I_{COM_LKG}	V_{COM1} = V_{COM2} = 20V	--	--	1	μA
CLAMP Outputs						
CLMP1, CLMP2 N-FET On-Resistance	R_{ON_CLM}		--	0.5	--	Ω
Adapter Power Enable Control						
ADD Detection Voltage Threshold	V_{ADD}	V_{ADD} Rising : 0V → 5V	3	3.6	4	V
ADD Detection Voltage Hysteresis		V_{ADD} Falling : 5V → 0V	--	400	--	mV
ADD Input Leakage Current	I_{ADD_LKG}	V_{ADD} = 5V , V_{RECT} = 0V	--	--	60	μA
Pull-up Resistance from ADEN to OUT pin when Adapter mode is disabled	R_{ADD}	V_{ADD} = 0V, V_{OUT} = 5V	--	275	350	Ω
ADD to ADEN Voltage when Adapter Mode is Enabled	V_{AD_EN}	V_{ADD} = 5V, V_{ADD} – V_{ADEN}	3	4.25	5	V
GPIO Input/Output						
GPIO Input Voltage (Logic-Low)	V_{IL}		0	--	0.8	V
GPIO Input Voltage (Logic-High)	V_{IH}		2	--	5	V
GPIO Output Voltage (Logic-Low)	V_{OL}		--	--	0.4	V
GPIO Output Voltage (Logic-High)	V_{OH}		2.6	3.3	3.6	V
Received Power (WPC Related Measurements)						
Received Power Accuracy	P_{RX_AC}	I_{OUT} = 0A to 1A (Note 5)	--	--	0.25	W
I^2C Compatible Interface (Note 5)						
Logic Input (SDA, SCL) Low Level	V_{SCL_L}		--	--	0.6	V
Logic Input (SDA, SCL) High Level	V_{SCL_H}		1.2	--	--	V
SCL Clock Frequency	f_{CLK}		10	--	400	kHz
Output Fall Time	$t_{FL2COUT}$		--	--	250	ns
Bus Free Time Between Stop/Start	t_{BUF}		1.3	--	--	μs
Hold Time Start Condition	t_{HD_STA}		0.6	--	--	μs
Setup Time for Start Condition	t_{SU_STA}		0.6	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Low Time	t_{LOW}		1.3	--	--	μs
SCL High Time	t_{HIGH}		0.6	--	--	μs
Data Setup Time	t_{SU_DAT}		100	--	--	ns
Data Hold Time	t_{HD_DAT}		0	--	900	ns
Setup Time for Stop Condition	t_{SU_STO}		0.6	--	--	μs
Mode Control						
Logic Input (MODE0, MODE1) Low Level	V_{MODE_L}		--	--	0.6	V
Logic Input (MODE0, MODE1) High Level	V_{MODE_H}		1.2	--	--	V
Communication Interface						
FSK Modulation Frequency Change	f_{FSK}	f_{OP} = 175kHz (Note 5)	3	5	7	kHz

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

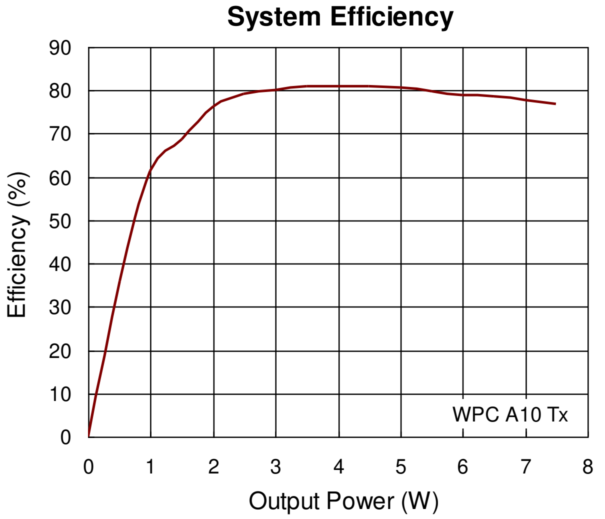
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

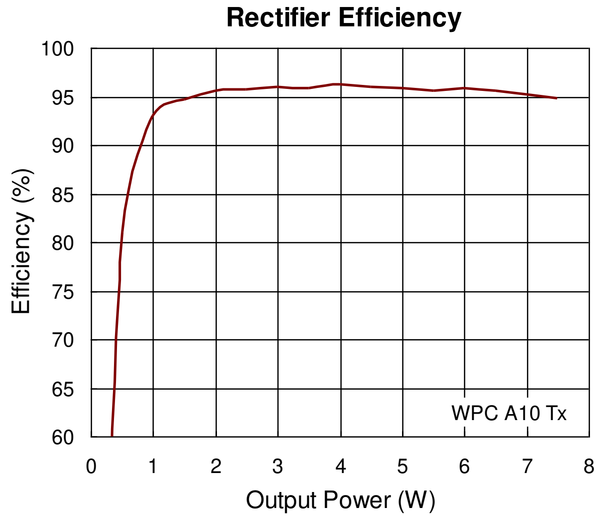
Note 3. Devices are ESD sensitive. Handling precaution recommended.

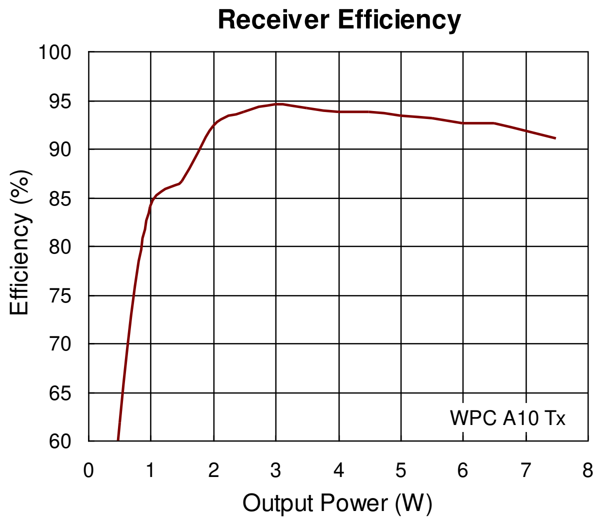
Note 4. The device is not guaranteed to function outside its operating conditions.

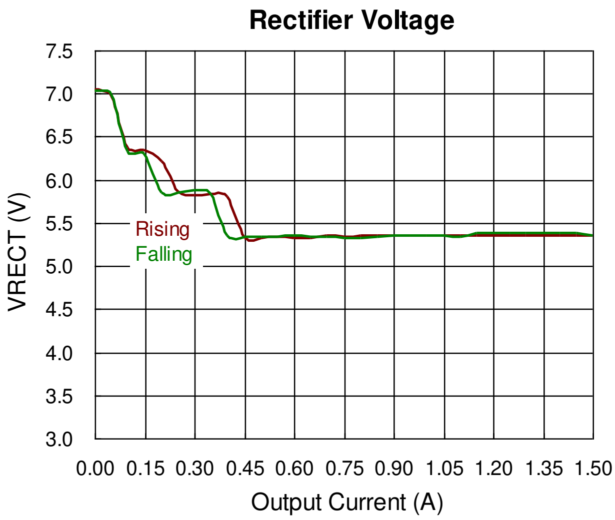
Note 5. Specification is guaranteed by design and/or correlation with statistical process control.

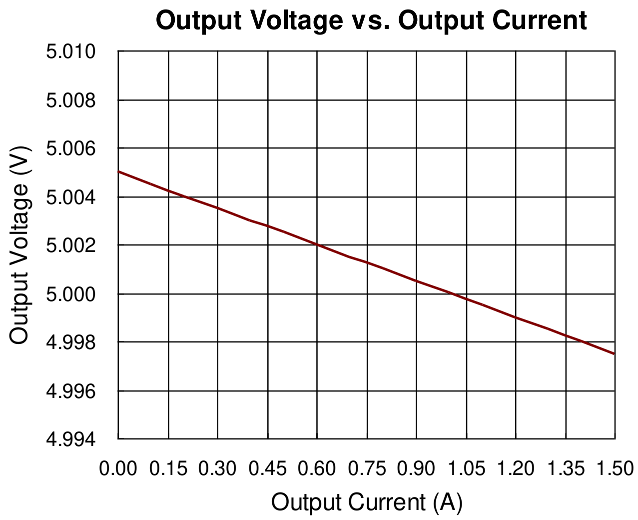
Typical Operating Characteristics

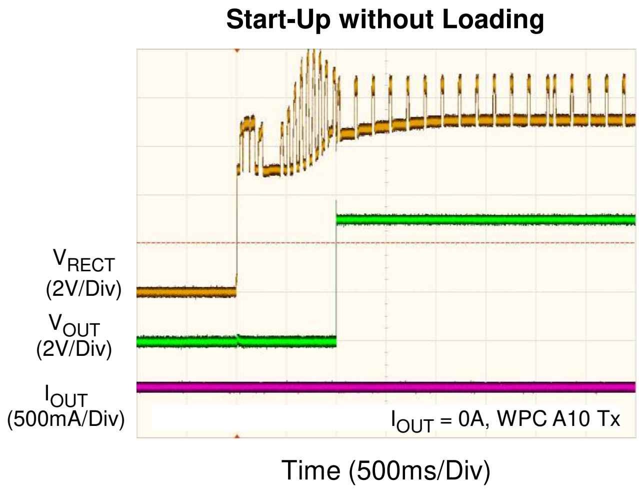




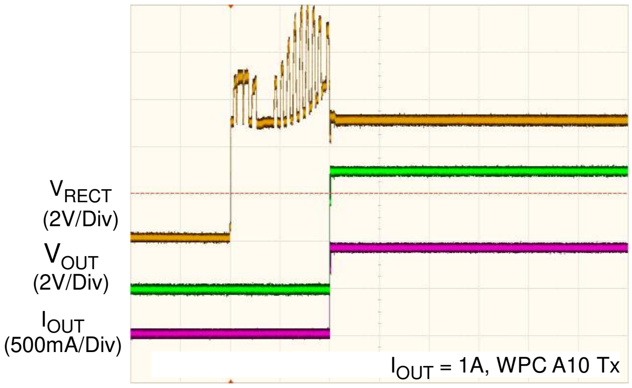






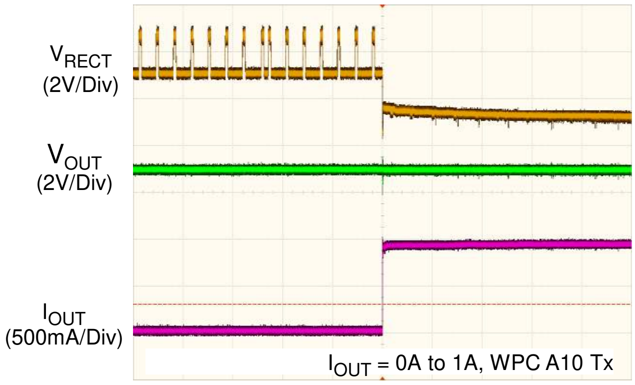


Start-Up with Loading



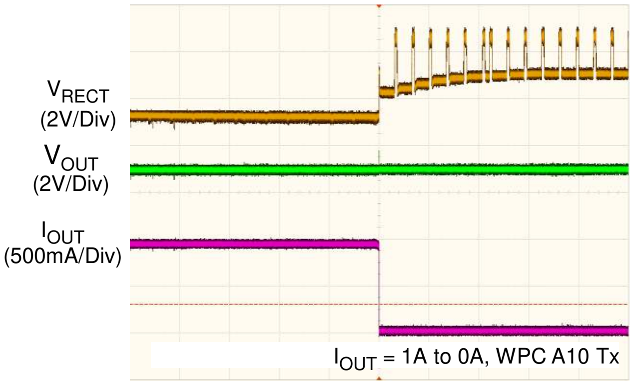
Time (500ms/Div)

Load Transient Response



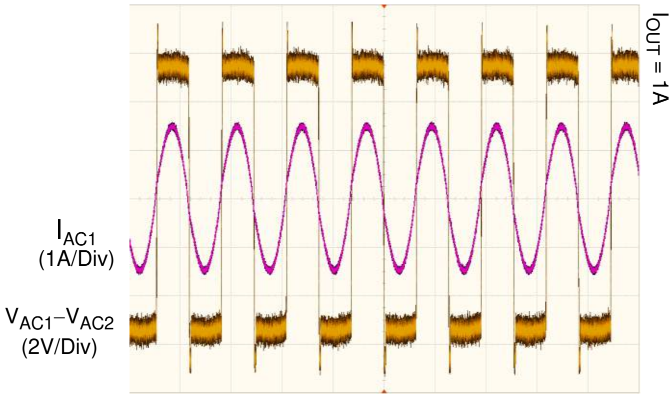
Time (500ms/Div)

Load Transient Response



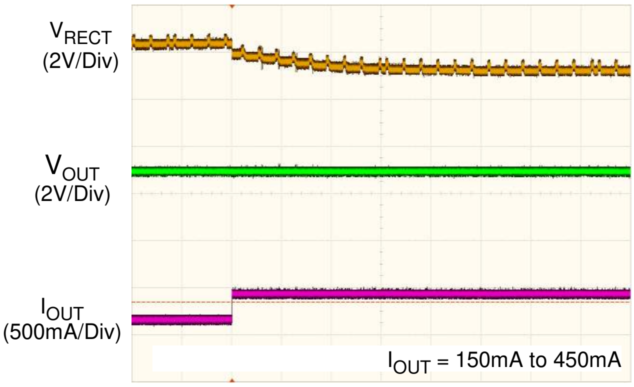
Time (500ms/Div)

Synchronous Rectifier



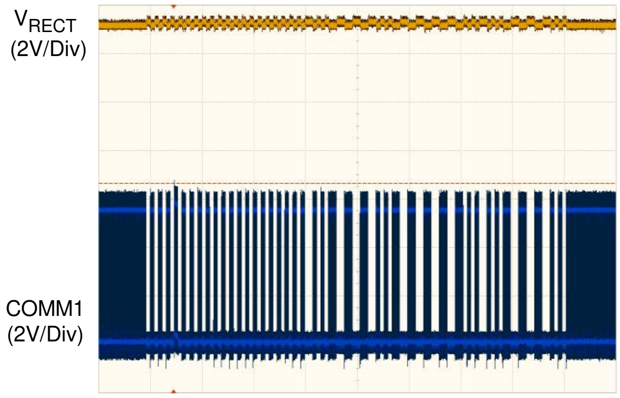
Time (5μs/Div)

Dynamic Rectifier Voltage



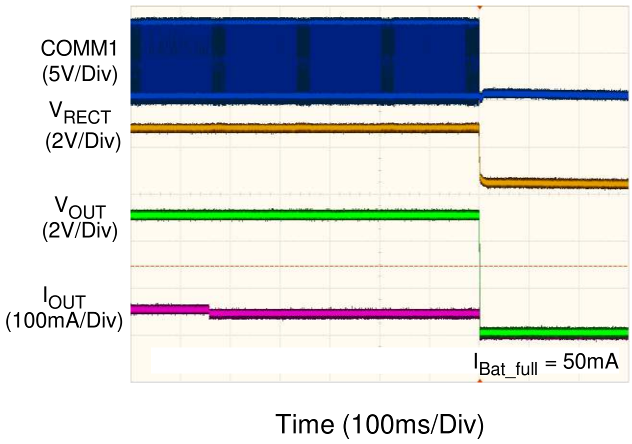
Time (500ms/Div)

Communication

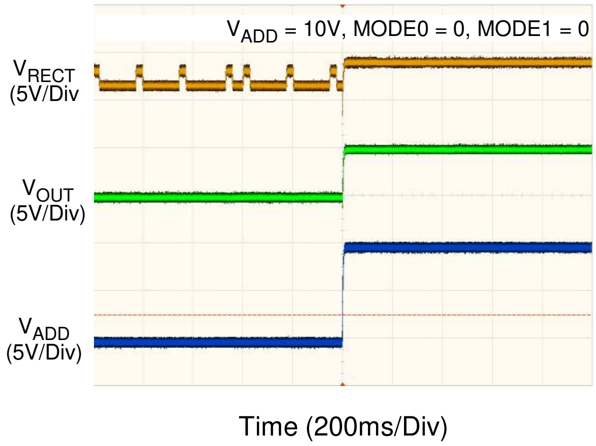


Time (3.29ms/Div)

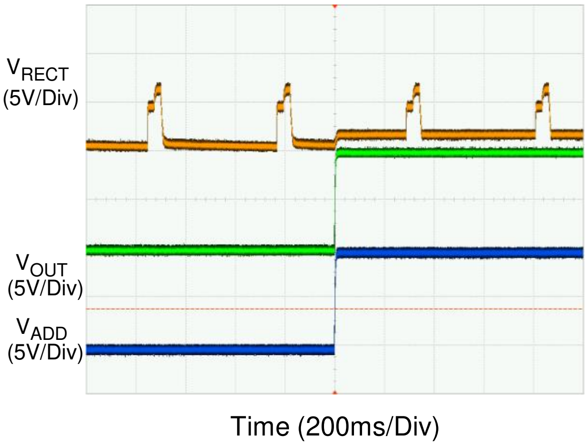
Battery Full Detection



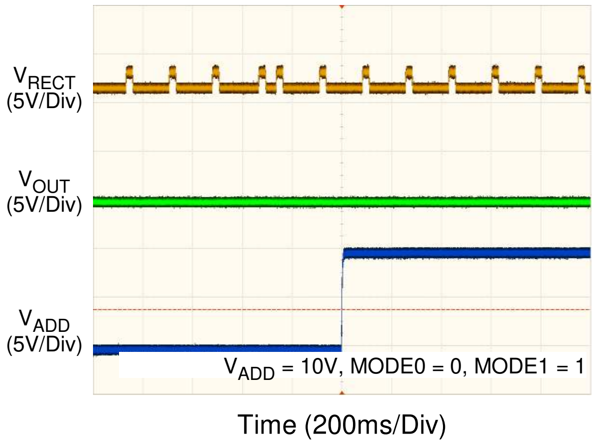
Default Mode



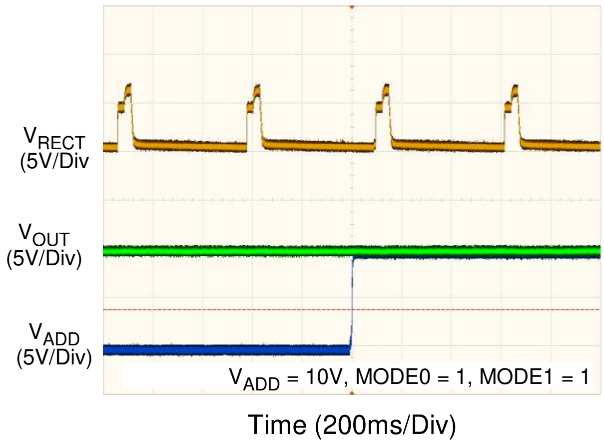
Adapter Mode



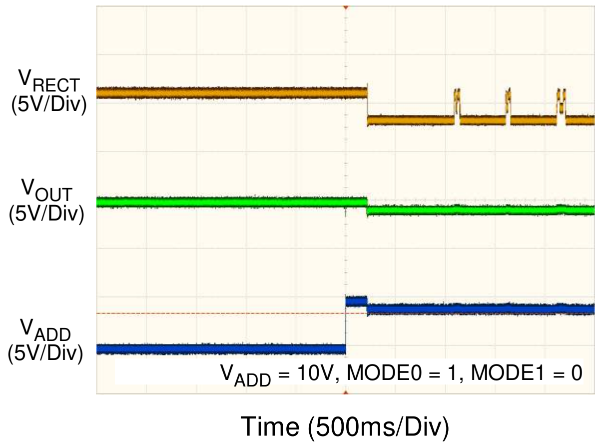
Wireless Mode



Disable Mode



OTG Mode



Functional Description

Description of the Wireless Power System

A wireless power system is composed by a power transmitter with one or more primary coils and a power receiver in a mobile system. Power transmitter will transfer power via a DC-to-AC inverter to drive a strong-coupled inductor to power receiver in a mobile device.

The power transferred to power receiver is controlled by itself. The power receiver sends communication packets with control error voltage information to the power transmitter for power tracking. The bit rate of the communication link from receiver to transmitter is 2kbps.

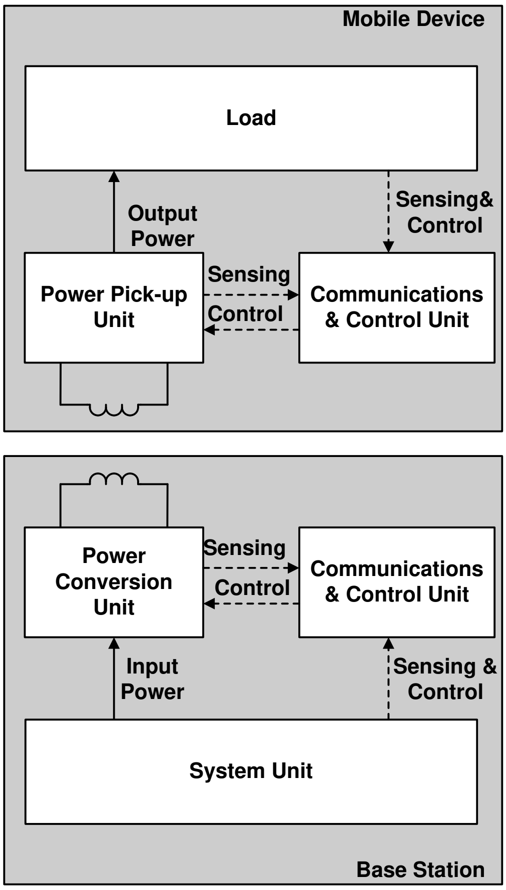


Figure 1. Wireless Power System

Start-up

When the receiver is placed on the power pad, the receiver coil is inductively coupled to the magnetic flux generated by the coil in the power pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor. The RT1650 communicates to the transmitter by switching on and off the COM FETs.

Power Transfer phases

There are 4 power transfer phases for the WPC V1.1.

- Selection : As soon as the Power Transmitter applies a Power Signal, the Power Receiver shall enter the selection phase.
- Ping : The power Receiver should send the Digital Ping Packet to power Transmitter then into next phase. If not, the system shall revert to the Selection phase. The power Receiver also can send the End Power transfer Packet to stop the power Transmitter.

- Identification & Configuration : In this phase, the Power Receiver identifies the revision of the System Description Wireless Power Transfer the Power Receiver complies and configuration information such as the maximum power that the Power Receiver intends to provide at its output. The Power Transmitter uses this information to create a Power Transfer Contract.

- Power Transfer : In this phase, the Power Transmitter continues to provide power to the Power Receiver. The power Receiver sends the Control Error Packet for adjusting the Primary Cell current. The Power Transmitter stops to provide power when the Received Power Packet is too low to trigger the FOD function or End Power Transfer Packet is sent from power Receiver.

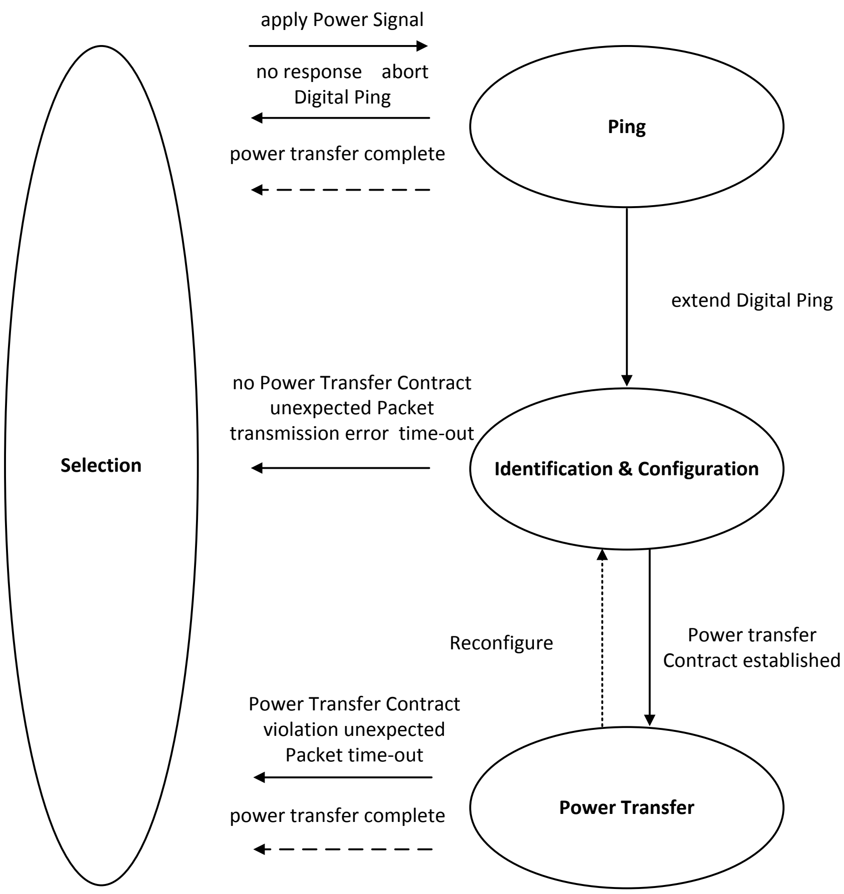


Figure 2. WPC V1.1 Low Power Transfer Phases

Micro Controller Unit

Memory Map

The memory mapping of MCU can be divided into 3 blocks, Code, SRAM and Peripheral. Each region has its recommend usage, and the memory access behavior could depend on which memory region you are accessing to.

Code

The size of the code region is 32KB. It is primarily used to store program code, including the exception vector table, which is a part of the program image. In OTP version of chip, the programmable user firmware will be stored in this area.

SRAM

The SRAM region starts from 0x2000_0000 and the total access size is 1KB. It's primarily used to store data, including stack.

Peripheral

There are 2 peripheral blocks in RT1650, MTP and peripheral registers. MTP (Multiple Time Programmable

Memory) is primarily used to save non-volatile user setting data and part of MTP store internal factory setting. User firmware can control some of chip hardware behavior via peripheral registers. It also could be an interface to communicate with external I^2C via the registers.

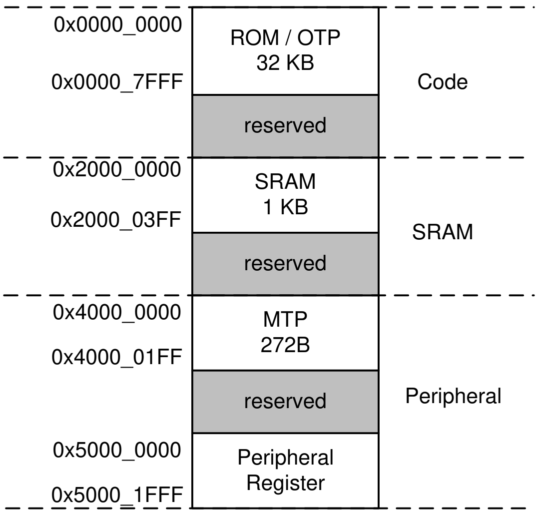


Figure 3. Memory Map

Programmable Dynamic Rectifier Voltage Control

The RT1650 provides a programmable Dynamic Rectifier Voltage Control function to optimize the transient response and power efficiency for applications. Table 1 and Figure 4 show an example to summarize how the rectifier behavior is dynamically adjusted based the registers V_{RECT_SETx}[7:0] (x = 1 to 4), which are available to be programmed by users.

Table 1. Dynamic Rectifier Voltage Setting

Output Current, I_{OUT}	Rectifier Voltage Target
< I_{OUT_TH1}	V_{RECT_SET1}
I_{OUT_TH1} to I_{OUT_TH2}	V_{RECT_SET2}
I_{OUT_TH2} to I_{OUT_TH3}	V_{RECT_SET3}
> I_{OUT_TH3}	V_{RECT_SET4}

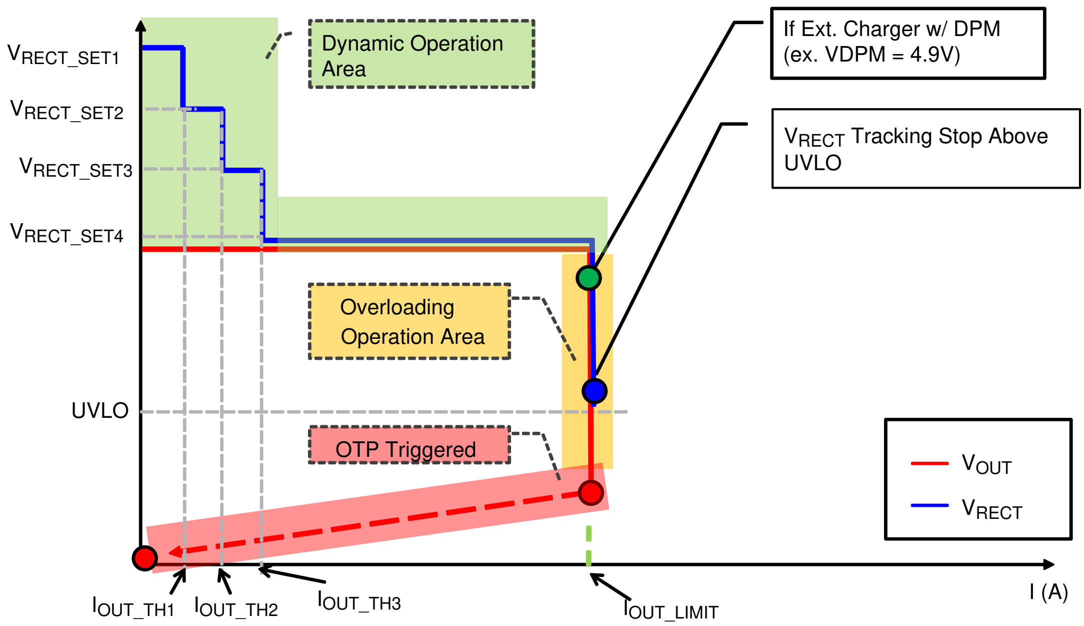


Figure 4. Dynamic Rectifier Voltage vs. Output Current

Thermal Management

The RT1650 provides an external device thermal management function with an external NTC thermistor and a resistor connected between TS pin and GND pin shown as Figure 5. User can use this function to control the temperature of the coil, battery or other device. An internal current source (60μA) is provided to the external NTC thermistor and generates a voltage at the TS pin. The TS voltage is detected and sent to the ADC converter for external device thermal manage control.

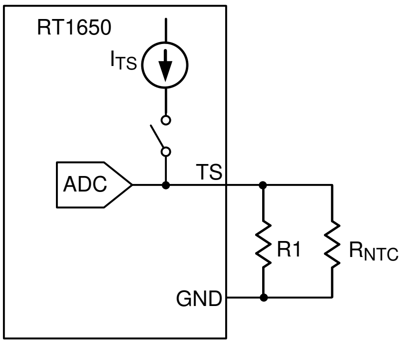


Figure 5. NTC Circuit for Device Temperature Detection and Thermoregulation

The thermal management function is shown as Figure 6. If the temperature is higher than Hot_temp or lower than Cold_temp threshold, the RT1650 will send the EPT to disable the power transfer. When the detected temperature increases and reaches the desired Regulation_temp, RT1650 will decrease the current limit to reduce the output current to regulate the temperature. When the detected temperature is lower than the Regulation_temp, the current limit will increase to the default value. This function is shown as Figure 7.

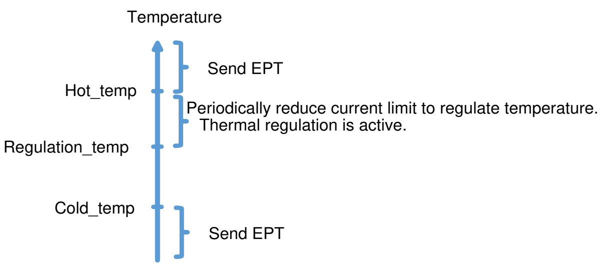


Figure 6. Thermal Management Function

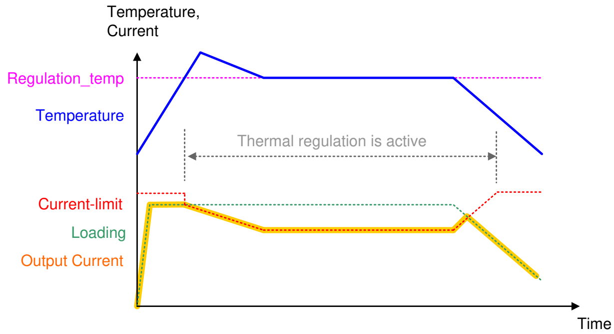


Figure 7. Thermoregulation Control

The NTC thermistor should be placed as close as possible to the device such as battery or mobile device. The recommended NTC thermistor is NCP15WF104F03RC (tolerance ±1%, β = 4250k). The typical resistance of the NTC is 100kΩ at 25°C. The recommended resistance for R_1 is 33kΩ (±1%).The value of the NTC thermistor at the desired temperature can be estimated by the following equation.

$$R_{NTC\_Reg} = R_O e^{\beta\left(\frac{1}{T_{Reg}} - \frac{1}{T_0}\right)}$$

$$R_{eq} = \frac{R_1 \times R_{NTC\_Reg}}{R_1 + R_{NTC\_Reg}}$$

where T_{Reg} is the desired regulation temperature in degree Kelvin. R_O is the nominal resistance at temperature T_0 and β is the temperature coefficient of the NTC thermistor. Req is the equivalent resistor of NTC thermistor in parallel with R_1.

Figure 8 shows the equivalent resistance of the thermistor in parallel with R_1 resistor varies with operating temperature. Figure 9 shows the VTS voltage with operating temperature. Customer can select the desire temperature and calculate the mapping data by the following equation.

Data = (VTS/2 x 1024)

If the thermal management function is not used (R_{NTC} = open), the resistor R1 = 24kΩ must be connected between the TS and GND pins

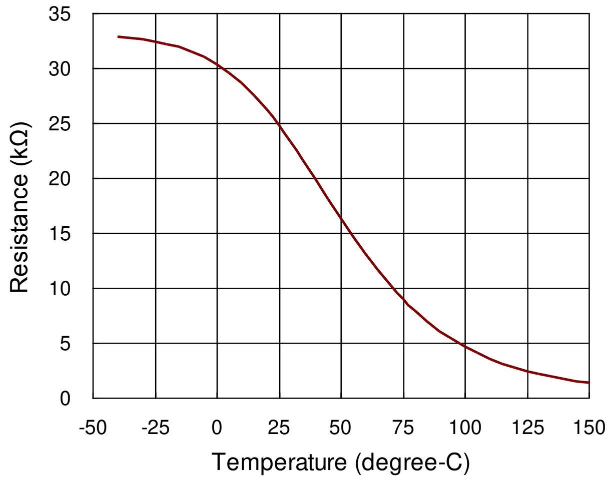


Figure 8. Equivalent Resistance for Temperature Sensing

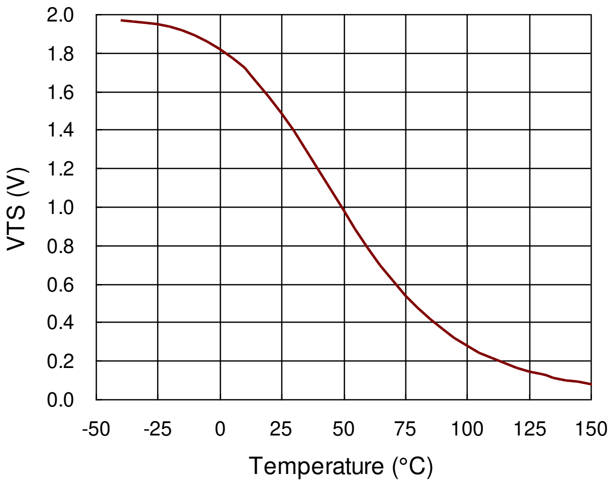


Figure 9. Thermal Sensing Voltage

Communication

The RT1650 supports two communication modulations, Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), to communicate with the power transmitter. For ASK modulation, the RT1650 provides two integrated communication N-FETs which are connected to the COM1 and COM2 pins. These N-FETs are used for modulating the secondary load current which allows the RT1650 to communicate Control Error and configuration information to the transmitter. Figure 10 shows the RT1650 operating with capacitive load modulation. When the N-FETs are turned-on, there is effectively a capacitor connected between AC1 and AC2. The impedance seen by the coil will be reflected in the primary as a change in current.

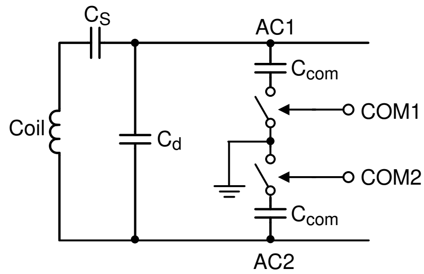


Figure 10. Capacitive Load Modulation

The RT1650 supports FSK demodulation to receive the power signal from the transmitter shown as Figure 11. The change in frequency between high and low states is dependent on the operating frequency. The power transmitter should modulate the power signal at specific times during the Negotiation phase to avoid interrupting communication packets from the receiver. The FSK modulation scheme should be compliant with WPC Volume II V0.9.

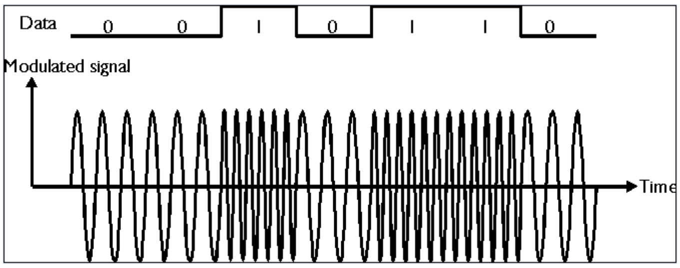


Figure 11. FSK Modulation Power Signal

Bit Encoding Scheme

According to WPC protocol, the RT1650 uses a differential bi-phase encoding scheme to modulate data bits onto the Power Signal. The internal clock signal has a frequency 2kHz. The Receiver shall encode a ONE bit using two transitions in the Power Signal, such that the first transition coincides with the rising edge of the clock signal, and the second transition coincides with the falling edge of the clock signal. The Receiver shall encode a ZERO bit using a single transition in the Power Signal, which coincides with the rising edge of the clock signal. Figure 12 shows an example of the differential bi-phase encoding.

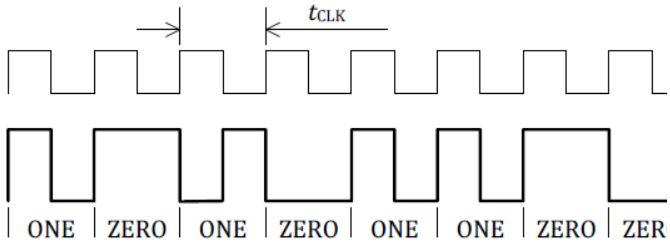


Figure 12. Example of the Differential Bi-phase Encoding

End Power Transfer Packet (WPC Header 0x02)

The End Power Transfer (EPT) packet is a special command for the RT1650 to request the transmitter to terminate power transfer. Table 2 specifies the reasons coulomb and their responding data field value. The condition column corresponds to the values sent by the RT1650 for a given reason.

Table 2. End Power Transfer (EPT) packet

Reason	Value	Condition
Unknown	0x00	V_{ADD} > 3.6V
Charge Complete	0x01	From I^{2}C, MODE0 = High or V_{TS} = High
Internal Fault	0x02	T_J > 150°C
Over Temperature	0x03	V_{TS} < V_{TS_HOT}, V_{TS} > V_{TS_COLD} or V_{TS} = Low
Over Voltage	0x04	Not Sent
Over Current	0x05	Not Sent
Battery Failure	0x06	From I^{2}C
Reconfigure	0x07	Not Sent
No Response	0x08	V_{RECT} target doesn't converge

Operation Mode Control

The RT1650 provides 2 input pins for operating mode control. Table 4 shows an example of operating mode control for wireless power and external adapter power. In default mode, both MODE0 and MODE1 are low, the wireless power is enabled and the adapter power has a higher priority. The wireless power is the normally operation. Once the adapter power is detected, the wireless power will be turned off and the ADEN will be pulled low to turn on the external switch for connecting the adapter power to system load. When the MODE1 is pulled to high, the adapter power will be turned off by the external switch and enters wireless mode to allow wireless power operation only In adapter mode, the wireless power is turned off always and ADEN is pulled low to turn on external switch for adapter power In this mode, it allows an external charger operating in USB OTG mode to connect the OUT pin to power the USB at ADD pin. If both MODE0 and MODE1 pins are pulled to high, the wireless power and adapter power are disabled.

Table 4. Operation Mode Control

Mode	MODE0	MODE1	Wireless Power	Adapter Power	OTG
Default	0	0	ON	ON(*)	OFF
Wireless	0	1	ON	OFF	OFF
Adapter	1	0	OFF	ON	Allowed
Disable	1	1	OFF	OFF	OFF

(*)Note: If both adapter power and wireless power are present, adapter power is given higher priority.

I^2C Interface

The RT1650 provides I^2C interface to communicate with external host device. Besides OTP firmware programming and MTP setting programming can be approached through the I^2C interface, the external host can also communicate with the RT1650 to achieve more flexible applications. For example, the host can read the ADC information via the I^2C Interface. In addition, the I^2C is used to read the internal status and the power source is from the VRECT. If the wireless function disable or in the adapter mode, the I^2C can't be accessed. Table 3 shows the register definition. It's not fixed, the registers definition can be costumed by firmware. If user need to read other information via I^2C, please discuss with RICHTEK firmware engineer.

I^2C Slave

0100010X (in binary format)

0x44 / 0x45 (hex format, include R/W bit)

MSB							LSB
0	1	0	0	0	1	0	R/W

Table 3. RT1650 Register Definition

Address	MSB	LSB	Name	Description
0x64	7	0	Vrect	Vrect (4V to 8V), unit = 15.68mV
0x66	7	0	Vout	Vout (3V to 6V), unit = 11.76mV
0x67	7	0	Iout	Iout (0A to 2A), unit = 7.84mA
0x78	7	0	last CE packet	last CE packet
0x79	7	0	last RP packet	last RP packet
0x7A	7	0	Received Power [7:0] (mW)	low byte of Received Power (mW)
0x7B	6	0	Received Power [14:8] (mW)	high byte of Received Power (mW)
0x7B	7	7	Received Power updating flag	0: Received Power is valid 1: Received Power is updating, not valid
0x10	7	7	Vout enable	0: Vout is disable 1: Vout is enable
0x02	7	0	freq_cnt[7:0]	Frequency = 1000 / ((freq_cnt[13:0] * 0.11) /128) KHz
0x03	5	0	freq_cnt[13:8]	
0x7C	3	0	WPC phase status	WPC status 0:booting 1: ping phase 2: ID_CF phase 3: Negotiation phase 4: power transfer phase

GPIO Interface

The RT1650 provides a programmable General Purpose Input/Output (GPIO) pin. The GPIO can be used as an input or used as a status indicator for different application. Before use this GPIO, user should discuss its functions with RICHTEK and then RICHTEK code its function into firmware.

GPIO can be programmed as an output port, be a status indicator. For example,

- To control LED flashing when Rx position search
- To indicate thermal regulation is active
- To indicate battery is full or charging is complete

GPIO can be programmed as input port, to connect external signal and inform MCU. For example,

- Enable/Disable the output
- Enable the End Power Packet

Option for GPIO

- Internal pull-up option (pull-up to 3.3V)
- Internal pull-low option
- GPIO can be push-pull or open-drain architecture when GPIO programmed as an output.

Table 5. RT1650 GPIO Specification

Symbol	Description	Min	Typ	Max
Vil	input logic low voltage			0.8V
Vih	input logic high voltage	2V		5V
Vol	output low voltage			0.4V
Voh	output high voltage when push-pull architecture	2.6V	3.3V	
Voh	output high voltage when open-drain architecture		Hi-Z	

Indicator Output

An open-drain output pin, CHG, is provided to indicate the status of wireless power receiver. The CHG pin can be connected to a LED for charge status indicator. When the output of the RT1650 is enabled, the open-drain N-FET at CHG pin will be pulled to low level.

Input Over-Voltage Protection

When the input voltage increases suddenly, the RT1650 adjusts voltage-control loop to maintain regulator output voltage and sends control error packets to the transmitter every 30ms until the input voltage comes back to the V_{RECT} target level (refer to Dynamic Rectifier Voltage Control Section). Once the V_{RECT} voltage exceeds its over-voltage threshold (11.5V typ.), the RT1650 turns on the N-FETs at CLMP1 and CLMP2 pins to shunt the input current through external capacitors. By the way the CLAMP function may affect the communication signal to let the Tx re-start up.

Over-Temperature Protection

The RT1650 provides an Over Temperature Protection (OTP) feature to prevent excessive power dissipation from overheating the device. The OTP function shuts down the linear regulator operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by around 20°C, the receiver will automatically resume operating.

Foreign Object Detection

The RT1650 is a WPC 1.1.1 compatible device. In order to enable a power transmitter to monitor the power loss across the interface as one of the possible methods to limit the temperature rise of foreign objects, the RT1650 reports its received power to the power transmitter. The received power equals the power that is available from the output of the power receiver plus any power that is lost in producing that output power (the power loss in the secondary coil and series resonant capacitor, the power loss in the shielding of the power receiver, the power loss in the rectifier). In WPC1.1.1 specification, Foreign Object Detection (FOD) is enforced. This means the RT1650 will send received power information with known accuracy to the transmitter. The received power is sensed as the Figure 13.

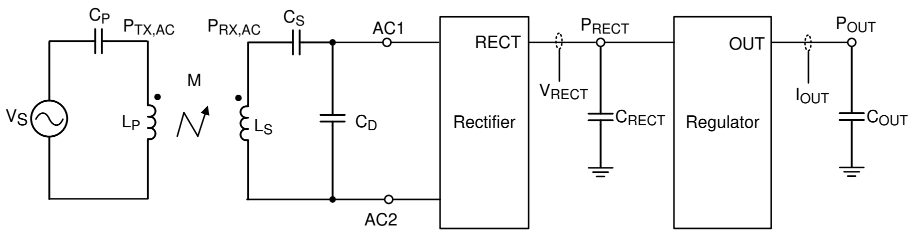


Figure 13. Received Power Sensed

Battery Charge Complete Detection

The RT1650 supports battery charge complete detection function. A programmable charge complete current threshold and a programmable charge complete delay time are provided. This function can be used to send the Charge Status packet (0x05) to the transmitter for indicating a full charged status 100%. Note that this packet does not turn off the transmitter.

The charge complete current threshold is adjustable from 0mA to 510mA and the default value is 50mA. The charge complete time is also adjustable from 0 seconds to 3825 seconds and the default value is 180 seconds.

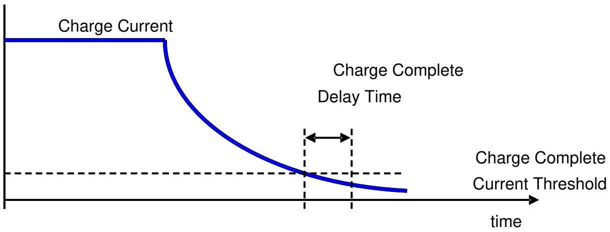


Figure 14. Battery Charge Complete Detection

There are 3 operation modes when the charge complete status is detected. The first mode is to send a CS packet (0x05) to transmitter only. The CS packet does not turn off the transmitter. In the second mode, the RT1650 will send a CS packet (0x05) and an EPT packet to transmitter. In the third mode, the RT1650 will send a CS packet (0x05) and stop communication with the transmitter.

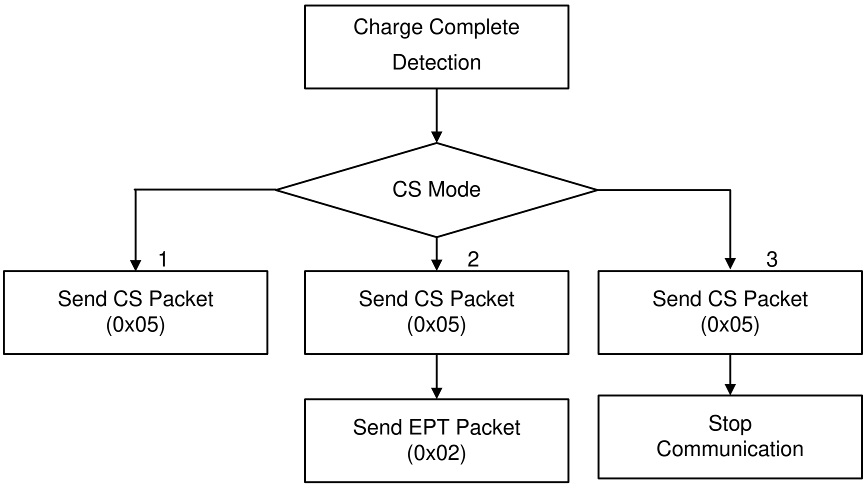


Figure 15. Operation Modes of Charge Complete Detection

Receiver Coil and Resonant Capacitors

According to WPC specification, the dual resonant circuit of the power receiver comprises the receiver coil and capacitors C1 and C2. The receiver coil design is related to system design. Coil shape, material, inductance and shielding need to be considered. Shielding provides protection from interference between wireless power system and mobile electronic device. The recommended coil self-inductance is between 8μH to 13μH. The capacitance of the resonant capacitors can be calculated by the following equations.

$$C1 = \frac{1}{L'_S \times (2\pi f_S)^2}$$

$$C2 = \frac{1}{L_S \times (2\pi f_d)^2 - \frac{1}{C1}}$$

In these equations, fs is resonant frequency with typical value 100kHz; and fd is another resonant frequency with typical value 1000kHz. L's is coil self-inductance when placed on the interface surface of a transmitter; and Ls is the self-inductance when placed away from the transmitter.

Firmware Setting

Please refer to another document for detailed description of firmware setting.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-48B 3x3.4 package, the thermal resistance, θ_{JA}, is 27.2°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (27.2°C/W) = 3.67W for WL-CSP-48B 3x3.4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 16 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

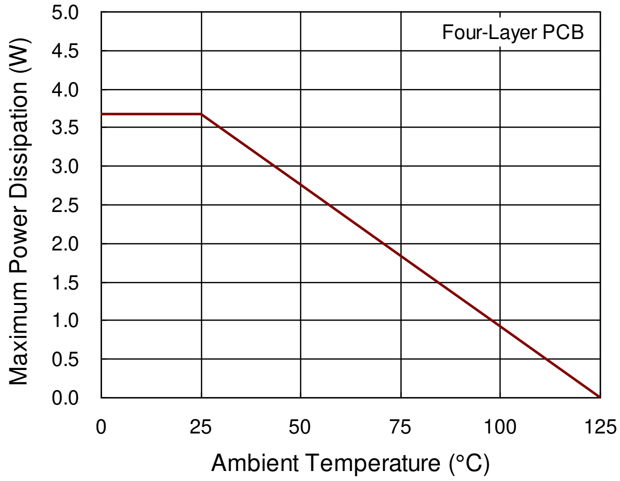


Figure 16. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the IC.

- Keep the traces of main current paths as short and wide as possible.
- Place the capacitors as close as possible to the IC.
- Power ground should be as large as possible and connected to a power plane for thermal dissipation.

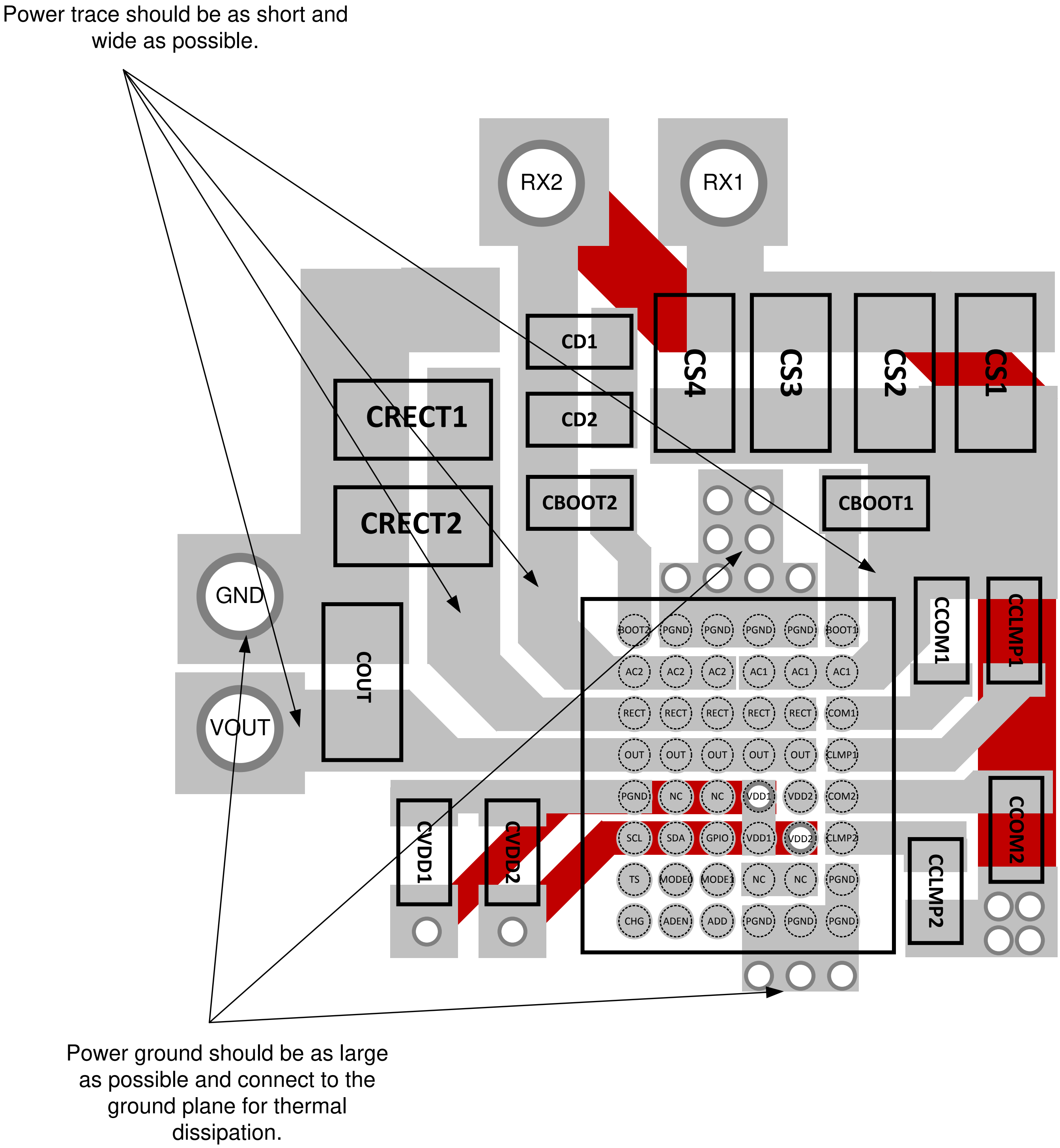
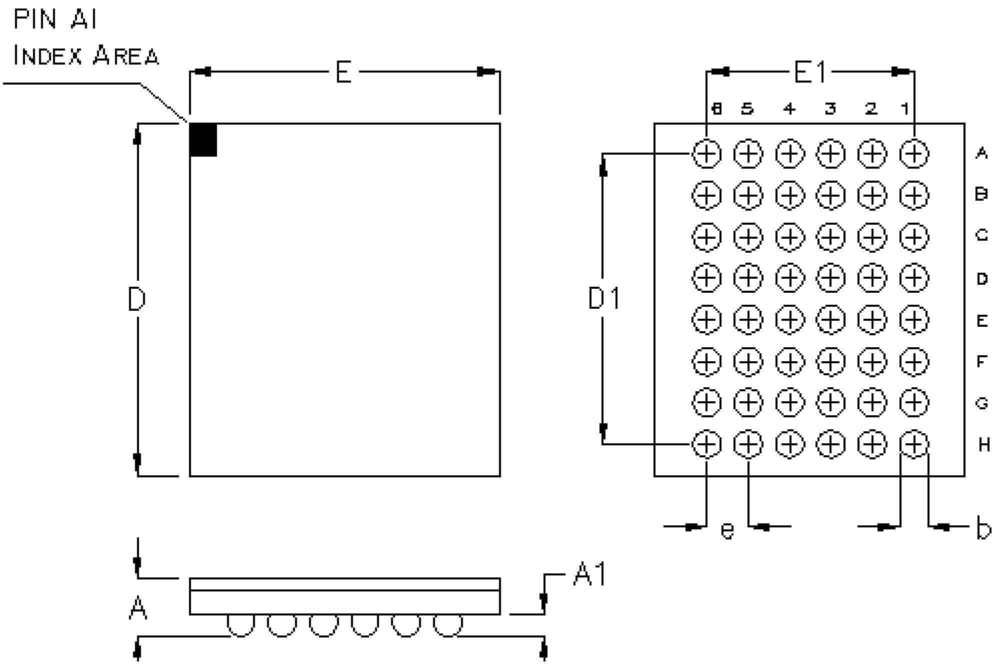


Figure 17. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.500	0.018	0.020
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	3.350	3.450	0.132	0.136
D1	2.800		0.110	
E	2.950	3.050	0.116	0.120
E1	2.000		0.079	
e	0.400		0.016	

48B WL-CSP 3x3.4 Package (BSC)

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