# EVM User's Guide: DS320-SLIMSAS-EVM DS320-SLIMSAS-EVM User's Guide



## ABSTRACT

The DS320-SLIMSAS-EVM together with the DS320PR810-RSC-EVM, or other Texas Instrument's riser-card style PCI-Express<sup>™</sup> 5.0 redriver evaluation module, provides a complete high-bandwidth platform for evaluating the signal conditioning features of the Texas Instruments PCI-Express 5.0 linear redrivers. These evaluation boards can be used for performance evaluation and initial system prototyping.



Figure 1-1. DS320-SLIMSAS-EVM – Top Side View

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# Trademarks

PCI-Express<sup>™</sup> is a trademark of PCI SIG.

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# 1 Introduction

DS320-SLIMSAS-EVM is a PCI-Express 5.0 x16 to two x8 SlimSAS (SFF-8654) adapter, which enables DS320PR810-RSC-EVM and other Texas Instruments PCI-Express 5.0 redriver riser card evaluation modules to interface with up to four U.2 solid state drives (SSDs) using commercially available SlimSAS (SFF-8654) to U.2 (SFF-8639) cable assemblies (not included). Interface to M.2 SSDs is also possible using commercially available U.2 to M.2 adapter cards (not included).

DS320-SLIMSAS-EVM features Texas instruments LMK00334 PCI-Express clock buffer for distributing the PCI-Express 100 MHz reference clock to downstream SSDs. It also allows flexible assignment of the PCI-Express side band signals using jumpers.

## 1.1 Features

- PCIe-Express CEM 5.0 compliant Goldfinger connector
- Two x8 SlimSAS (SFF-8654) connectors
- LMK00334 PCI-Express clock buffer
- Flexible assignment of PCI-Express side band signals
- Supports PCI-Express 1 x4, 2 x4, and 4 x4 bifurcation ٠

## 1.2 Applications

- PCI Express Gen-1, 2, 3, 4 and 5
- Enterprise storage

## **1.3 Description**

## **1.3.1 Connectors and Access Points**

Table 1-1 shows DS320-SLIMSAS-EVM main connectors and access points.

COMPONENT	NAME	FUNCTION / DESCRIPTION
P2	PCIe 4.0 x8 SlimSAS Connector 1	Access points to PCIe lanes 0 - 7. Use a SlimSAS (SFF-8654) to U.2 (SFF-8639) cable assembly (not included) to interface to SSDs with U.2 form factor.
P3	PCIe 4.0 x8 SlimSAS Connector 1	Access points to PCIe lanes 8 - 15. Use a SlimSAS (SFF-8654) to U.2 (SFF-8639) cable assembly (not included) to interface to SSDs with U.2 form factor.
P1	PCIe CEM 5.0 x16 Goldfinger Connector	Access points to PCIe lanes 0 - 15. Plug into a PCIe x16 CEM slot.
J7	3x1 Header	I2C bus access point.
J1	2x1 Header	Access point to WAKE and CLKREQ pins on the CEM connector.

# Table 4.4. Main Commontons and Assass Dainte

Table 1-2 shows PCIe side band signal controls and access points.

Table 1-2.	PCIe Side	Band Signal	Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J8	3x1 Header	Provision for connecting PERST# signal from the CEM connector to B11 or B12 pin of SlimSAS connector P2. Shunt installed across pins 1-2: PERST# signal routed to B11 pin of SlimSAS connector P2. Shunt installed across pins 2-3: PERST# signal routed to B12 pin of SlimSAS connector P2 (default).
J10	3x1 Header	Provision for connecting PERST# signal from the CEM connector to B29 or B30 pin of SlimSAS connector P2. Shunt installed across pins 1-2: PERST# signal routed to B29 pin of SlimSAS connector P2. Shunt installed across pins 2-3: PERST# signal routed to B30 pin of SlimSAS connector P2 (default).

COMPONENT	NAME	FUNCTION / DESCRIPTION
J9	3x1 Header	<ul> <li>Provision for connecting PERST# signal from the CEM connector to B11 or B12 pin of SlimSAS connector P3.</li> <li>Shunt installed across pins 1-2: PERST# signal routed to B11 pin of SlimSAS connector P3.</li> <li>Shunt installed across pins 2-3: PERST# signal routed to B12 pin of SlimSAS connector P3 (default).</li> </ul>
J11	3x1 Header	<ul> <li>Provision for connecting PERST# signal from the CEM connector to B29 or B30 pin of SlimSAS connector P3.</li> <li>Shunt installed across pins 1-2: PERST# signal routed to B29 pin of SlimSAS connector P3.</li> <li>Shunt installed across pins 2-3: PERST# signal routed to B30 pin of SlimSAS connector P3 (default).</li> </ul>
J16	4x2 Header	<ul> <li>Provision for connecting PRSNT1 signal to PRSNT2_1, PRSNT2_2, PRSNT2_3 and PRSNT2_4 pins on the CEM connector.</li> <li>Shunt installed across pins 1-2: PRSNT1 signal routed to PRSNT2_1 pin on the CEM connector (default).</li> <li>Shunt installed across pins 3-4: PRSNT1 signal routed to PRSNT2_2 pin on the CEM connector (default).</li> <li>Shunt installed across pins 5-6: PRSNT1 signal routed to PRSNT2_3 pin on the CEM connector (default).</li> <li>Shunt installed across pins 5-6: PRSNT1 signal routed to PRSNT2_3 pin on the CEM connector (default).</li> <li>Shunt installed across pins 7-8: PRSNT1 signal routed to PRSNT2_4 pin on the CEM connector (default).</li> </ul>
J5	4x1 Header	Access point to the pins A8, A9, A26, and A27 of SlimSAS connector P2.
J6	4x1 Header	Access point to the pins A8, A9, A26, and A27 of SlimSAS connector P3.
J12	3x1 Header	Provision for connecting PRSNT2_2 pin on the CEM connector to B11 or B12 pin of SlimSAS connector P2.
J14	3x1 Header	Provision for connecting PRSNT2_1 pin on the CEM connector to B29 or B30 pin of SlimSAS connector P2.
J13	3x1 Header	Provision for connecting PRSNT2_4 pin on the CEM connector to B11 or B12 pin of SlimSAS connector P3.
J15	3x1 Header	Provision for connecting PRSNT2_3 pin on the CEM connector to B29 or B30 pin of SlimSAS connector P3.

Table 1-2 shows PCIe reference clock controls and access points.

## Table 1-3. PCIe Reference Clock Controls and Access Points

COMPONENT	NAME	FUNCTION / DESCRIPTION
JMP2	3x1 Header	Clock distributor (LMK00334) output enable Shunt installed across pins 1-2: outputs disabled. Shunt installed across pins 2-3: outputs enabled (default).
JMP1	3x1 Header	Clock distributor (LMK00334) input select Shunt installed across pins 1-2: CLKIN1 (An external clock source coming from the SMP connectors) selected. Shunt installed across pins 2-3: CLKIN0 (PCIe system clock coming from the CEM connector) selected (default).
J2 - J3	SMP Connectors	Provision for connecting an external clock source to the LMK00334 CLK1 input Plug into a PCIe x16 CEM slot.
JMP3	3x1 Header	Clock distributor (LMK00334) LVCMOS reference output enable Shunt installed across pins 1-2: reference output enabled. Shunt installed across pins 2-3: reference output disabled (default).
J4	SMP Connector	Access point to the LMK00334 reference output.

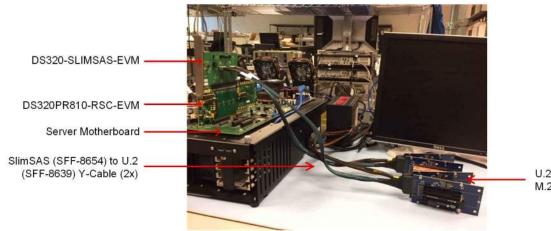


# 1.4 Quick-Start Guide

- 1. Check that the shunts are at the following default positions as shown in Figure 1-1.
  - J8: Shunt installed across pins 2-3: PERST# signal routed to B12 pin of SlimSAS connector P2.
  - J10: Shunt installed across pins 2-3: PERST# signal routed to B30 pin of SlimSAS connector P2.
  - J9: Shunt installed across pins 2-3: PERST# signal routed to B12 pin of SlimSAS connector P3.
  - J11: Shunt installed across pins 2-3: PERST# signal routed to B30 pin of SlimSAS connector P3.
  - J16: Shunts installed across pins 1-2, 3-4, 5-6, and 7-8: PRSNT1 signal routed to PRSNT2\_1, PRSNT2\_2, PRSNT2\_3, and PRSNT2\_4 pins on the CEM connector.
  - JMP2: Shunt installed across pins 2-3: LMK00334 outputs enabled.
  - JMP1: Shunt installed across pins 2-3: PCIe system clock selected as an input to the LMK00334.
  - JMP3: Shunt installed across pins 2-3: LMK00334 reference output disabled.
- 2. Plug DS320PR810-RSC-EVM, or other riser card style TI evaluation board into a PCIe x16 CEM slot on a motherboard. Ensure that the motherboard is powered down prior to installing the riser card.
- 3. Install DS320-SLIMSAS-EVM into the straddle connector on the riser card selected in the prior step.
- Connect a SlimSAS (SFF-8654) to U.2 (SFF-8639) cable assembly (not included) into the SlimSAS connector P2 of the DS320-SLIMSAS-EVM. Alternatively, connect the second cable assembly into the SlimSAS connector P3 of the DS320-SLIMSAS-EVM.
- 5. Attached an endpoint or endpoints on the other side of the cable. Ensure that the power is also provided to one or more of the endpoints prior to powering up the motherboard.
- 6. Power-up the motherboard.
- 7. Observe a successful linkup of one or more of the endpoints using system BIOS or other available system utility.

# 2 Typical Test Setup

Figure 2-1 shows a typical system test setup with the DS3200PR810-RSC-EVM and DS320-SLIMSAS-EVM placed between a CPU on a server motherboard and PCIe 5.0 endpoints. The endpoints are SSDs with M.2 form factor mounted on U.2 to M.2 adapters.



U.2 to M.2 Adapters with M.2 SSDs (4x)

Figure 2-1. Example Test Setup

The test setup features the following items not included in the DS320-SLIMSAS-EVM:

- SlimSAS x8 (SFF-8654) to 2x PCIe Drive Receptacle (SFF-8639) Cable (for U.2, 1×4 only), Part #: SLSP-8X-39X2F4-0.5M. More information about this item is available here.
- PCIe 4.0 U.2 to M.2 Adapter, Part #: PCI-AD-U2M2-04-G4. More information about this item is available here.



# **3 Board Layout**

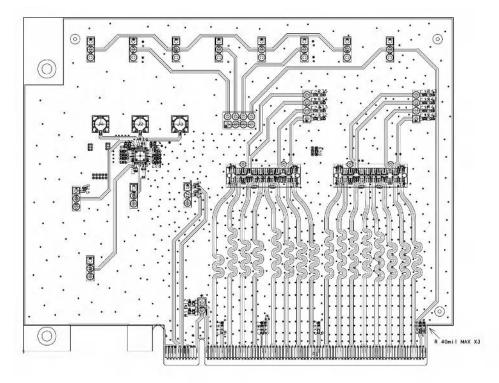


Figure 3-1. Top Layer

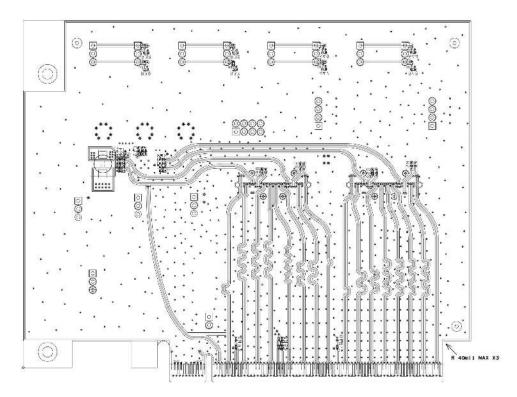


Figure 3-2. Bottom Layer



# **4** Schematic

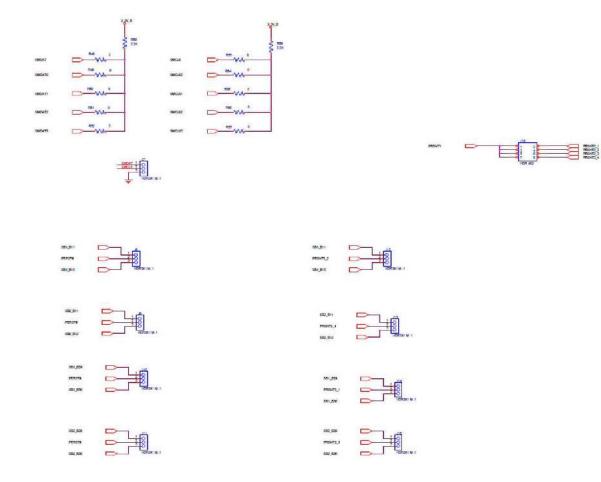


Figure 4-1. Controls Schematic Page

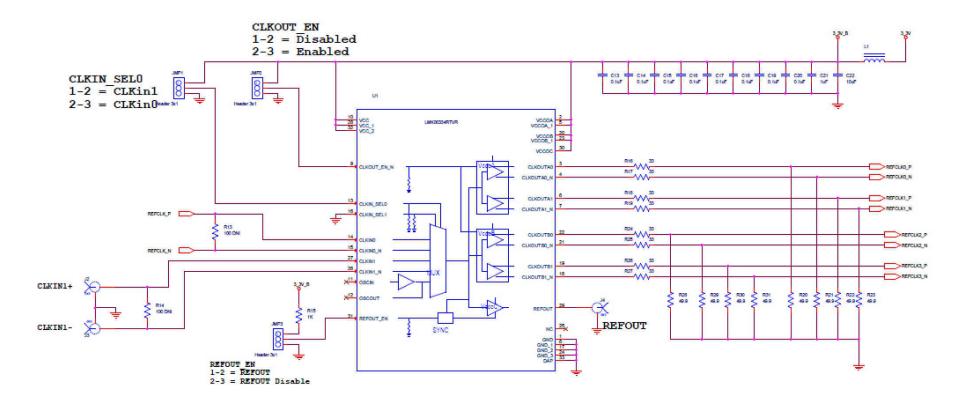


Figure 4-2. Clock Distribution Schematic Page

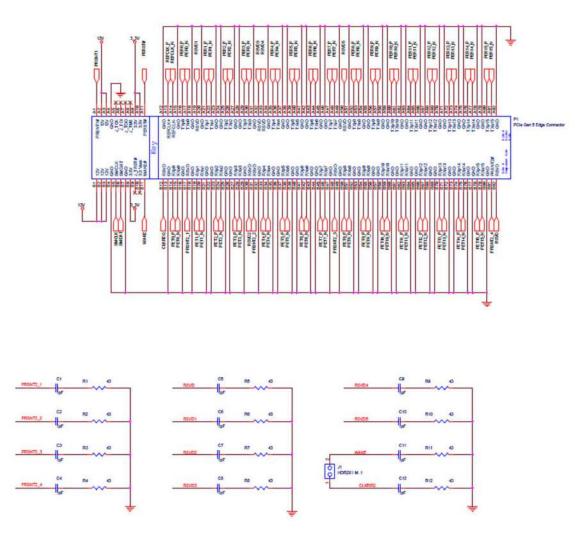
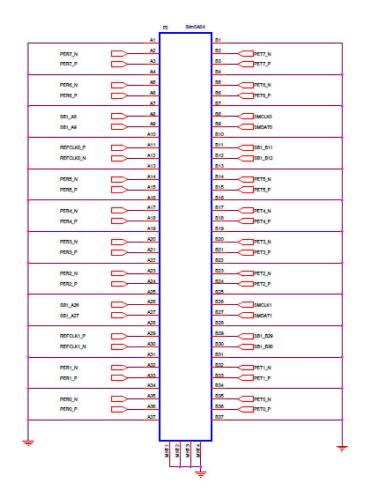
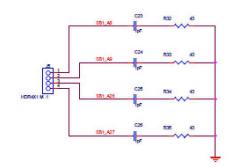


Figure 4-3. Goldfinger Connector Schematic Page







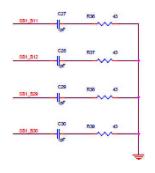
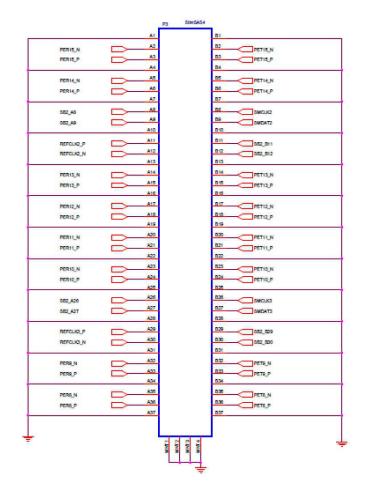
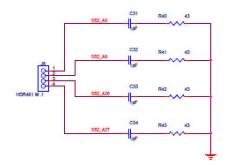


Figure 4-4. SlimSAS Connector 1 Schematic Page







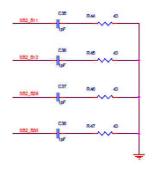


Figure 4-5. SlimSAS Connector 2 Schematic Page

# 5 Bill of Materials

## Table 5-1. Bill of Materials

Reference	Quantity	Value	Manufacturer	Manufacturer Part Number	PCB Footprint
C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C23,C2 4,C25,C26,C27,C28,C29,C30,C31,C32,C33,C34,C35, C36,C37,C38	28	1 pF	Murata Electronics	GRM1555C1H1R0CA01D	CAP_0402
C13,C14,C15,C16,C17,C18,C19,C20	8	0.1 µF	Murata Electronics	GRM155R71A104KA01J	CAP_0402
C21	1	1 µF	Yageo	CC0402KRX5R6BB105	CAP_0402
C22	1	10 µF	Murata Electronics	GRM188R60J106ME47D	CAP_0603
JMP1,JMP2,JMP3	3	Header 3x1	AMP		hdr_thvt_1x3_254_871
J1	1	HDR2X1 M .1	AMP	103321-2	hdr_thvt_1x2_254_871
J2,J3,J4	3	SMP	Rosenberger		CON_SMVT_19S101-40ML5_ R04350
J5,J6	2	HDR4X1 M .1	AMP	103321-4	hdr_thvt_1x4_254_871
J7,J8,J9,J10,J11,J12,J13,J14,J15	9	HDR3X1 M .1	AMP	103321-3	hdr_thvt_1x3_254_871
J16	1	HDR 4X2			HDR_THVT_2X4_254_871
LB1	1	THD-47-478-10	Brady		rectangle
L1	1	6.8 µH	Eaton		IND_SM_DRA73
PCB1	1	HSDC096A	Any		n/a
P1	1	PCIe Gen 5 Edge Connector			CON_EDGE_164_100_Gen5
P2,P3	2	SlimSAS4	Amphenol ICC		CON_SMVT_U10BH74
R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12,R32,R3 3,R34,R35,R36,R37,R38,R39,R40,R41,R42,R43,R44, R45,R46,R47	28	43	Panasonic		RES_0402
R13,R14	2	100 DNI	Panasonic Electronic Components	ERA-2AED101X	RES_0402
R15	1	1К	Panasonic Electronic Components	ERJ-2GEJ102X	RES_0402
R16,R17,R18,R19,R24,R25,R26,R27	8	33	Panasonic Electronic Components	ERA-2AKD330X	RES_0402
R20,R21,R22,R23,R28,R29,R30,R31	8	49.9	Panasonic Electronic Components	ERJ-2RKF49R9X	RES_0402



### Schematic

## Table 5-1. Bill of Materials (continued)

Reference	Quantity	Value	Manufacturer	Manufacturer Part Number	PCB Footprint
R48	1	0	Panasonic Electronic Components	ERJ-2GE0R00X	RES_0402
R49,R50,R51,R52,R53,R54,R55,R56,R57	9	0	Panasonic Electronic Components	ERJ-2GE0R00X	RES_0402
R58,R59	2	2.2 K	Panasonic Electronic Components	ERJ-2GEJ222X	RES_0402
SHNT1,SHNT2,SHNT3	3	QPC02SXGN-RC	Sullins Connector Solutions		0.1
U1	1	LMK00334RTVR	Texas Instruments	LMK00334RTVR	RTV0032BA_310x310

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User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

#### CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

#### FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

#### Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### **Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

- 3.3 Japan
  - 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti\_ja/general/eStore/notice\_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti\_ja/general/eStore/notice\_01.page
  - 3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti\_ja/general/eStore/notice\_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti\_ja/general/eStore/notice\_02.page
- 3.4 European Union
  - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

#### 4 EVM Use Restrictions and Warnings:

- 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
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