The following document contains information on Cypress products. Although the document is marked with the name “Broadcom”, the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

CONTINUITY OF SPECIFICATIONS

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

CONTINUITY OF ORDERING PART NUMBERS

Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

FOR MORE INFORMATION

Please visit our website at www.cypress.com or contact your local sales office for additional information about Cypress products and services.

OUR CUSTOMERS

Cypress is for true innovators – in companies both large and small.

Our customers are smart, aggressive, out-of-the-box thinkers who design and develop game-changing products that revolutionize their industries or create new industries with products and solutions that nobody ever thought of before.

ABOUT CYPRESS

Founded in 1982, Cypress is the leader in advanced embedded system solutions for the world’s most innovative automotive, industrial, home automation and appliances, consumer electronics and medical products. Cypress’s programmable systems-on-chip, general-purpose microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first.

Cypress is committed to providing customers with the best support and engineering resources on the planet enabling innovators and out-of-the-box thinkers to disrupt markets and create new product categories in record time. To learn more, go to www.cypress.com.

Single-Chip IEEE 802.11 a/b/g/n 2x2 MAC/ Baseband/Radio with Integrated Bluetooth 4.0 + HS

GENERAL DESCRIPTION

The Broadcom® BCM43242 is a single-chip device for wireless media systems. It integrates the MAC, baseband, and radio of IEEE 802.11 a/b/g and 2×2 IEEE 802.11n with Bluetooth 4.0 + HS.

The BCM43242 takes advantage of the high throughput and extended range of the Broadcom second-generation MIMO solution. With MIMO, the information is sent and received over two or more antennas, simultaneously using the same frequency band, thus providing greater range and higher throughput, while maintaining compatibility with legacy IEEE 802.11a/b/g devices. This is accomplished through a combination of enhanced MAC and PHY implementations including spatial multiplexing modes in the transmitter and receiver, and advanced digital signal processing techniques to improve receive sensitivity. The BCM43242 architecture, with its fully integrated dual-band radio transceiver, supports 2 × 2 antennas. It also supports 20 and 40 MHz channels, allowing for PHY Layer throughput up to 300 Mbps.

Using advanced design techniques and process technology to reduce active and idle power, the BCM43242 is designed to address the needs of media-embedded applications that require minimal power consumption and compact size.

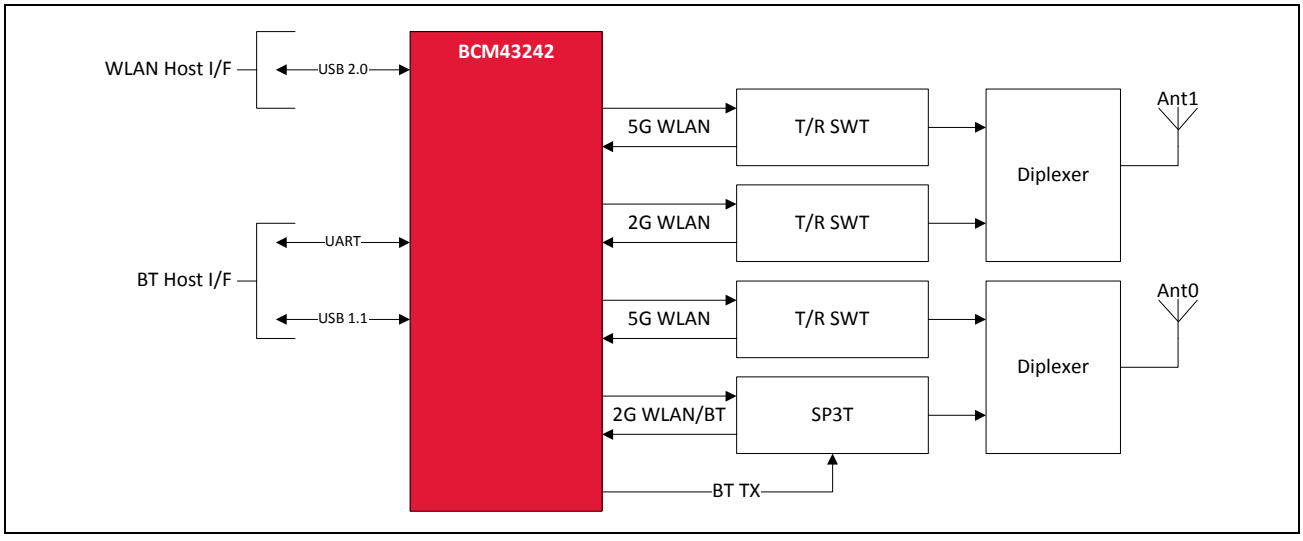
FEATURES

It includes a power management unit that simplifies the system power topology and allows for operation directly from a 3.3V or 5V supply, which provides flexibility. The BCM43242 includes power saving schemes such as single-core listen (OCL), single-core demodulation of SISO/STBC packets, and dynamic maximum likelihood (ML) demapping (which is based on channel conditions).

The BCM43242 implements the highly sophisticated Enhanced Collaborative Coexistence radio coexistence algorithms and hardware mechanisms. As a result, enhanced overall quality for simultaneous audio, video, and data transmission for home entertainment devices is achieved.

The WLAN host interface is USB 2.0. The Bluetooth host interface options include full-speed USB 1.1 and a high-speed UART.

Figure 1: Functional Block Diagram



5300 California Avenue • Irvine, CA 92617 • Phone: 949-926-5000 • Fax: 949-926-5203

Revision History

Revision	*Date*	*Change Description*
002-14920 *D	09/21/16	Parts in this datasheets are not recommended for new designs
43242-DS103-R	05/18/15	**Updated:** • "Power Supply Topology" on page 16 • "BCM43242 PMU Features" on page 16 • Figure 3: "Typical Power Topology," on page 17 • Table 15: "FCFBGA Signal Descriptions," on page 75 • Table 19: "Absolute Maximum Ratings," on page 84 • Table 21: "ESD Specifications," on page 85 • Table 22: "Recommended Operating Conditions and DC Characteristics," on page 86 • Section 16: "WLAN RF Specifications, "Introduction" on page 94 • Table 33: "Core Buck Switching Regulator (CBUCK) Specifications," on page 104 • Table 34: "CLDO Specifications," on page 106 • Table 36: "LNLDO1 Specifications," on page 108 • "WLAN Current Consumption" on page 109 (added) • Figure 28: "WLAN = ON, Bluetooth = ON," on page 114 • Figure 29: "WLAN = OFF, Bluetooth = OFF," on page 114
43242-DS102-R	10/29/13	**Updated:** • By changing this from a preliminary data sheet to a data sheet.

Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

Revision	*Date*	*Change Description*
43242-DS101-R	10/25/13	**Updated:** • The Features section just prior to the “Revision History” on page 4. • “BCM43242 PMU Features” on page 17. • “WLAN Power Management” on page 19. • “GPIO Interface” on page 51. • Section 10: “USB Interfaces,” on page 52. • “PHY Features” on page 58. • Table 13: “Pin List By Pin Number,” on page 66. • Table 15: “FCFBGA Signal Descriptions,” on page 74. • “Environmental Ratings” on page 84. • Table 28: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 94. • Table 29: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 98. • Table 31: “WLAN 5 GHz Transmitter Performance Specifications,” on page 102. • Table 33: “Core Buck Switching Regulator (CBUCK) Specifications,” on page 104. • “Package Thermal Characteristics” on page 114. • Section 23: “Ordering Information,” on page 116.
43242-DS100-R	04/12/12	Initial release

Table of Contents

List of Figures

List of Tables

About This Document

Purpose and Audience

This data sheet provides details about the functional, operational, and electrical characteristics of the Broadcom BCM43242. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK**, press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads and Support site (http://www.broadcom.com/support/).

Section 1: Overview

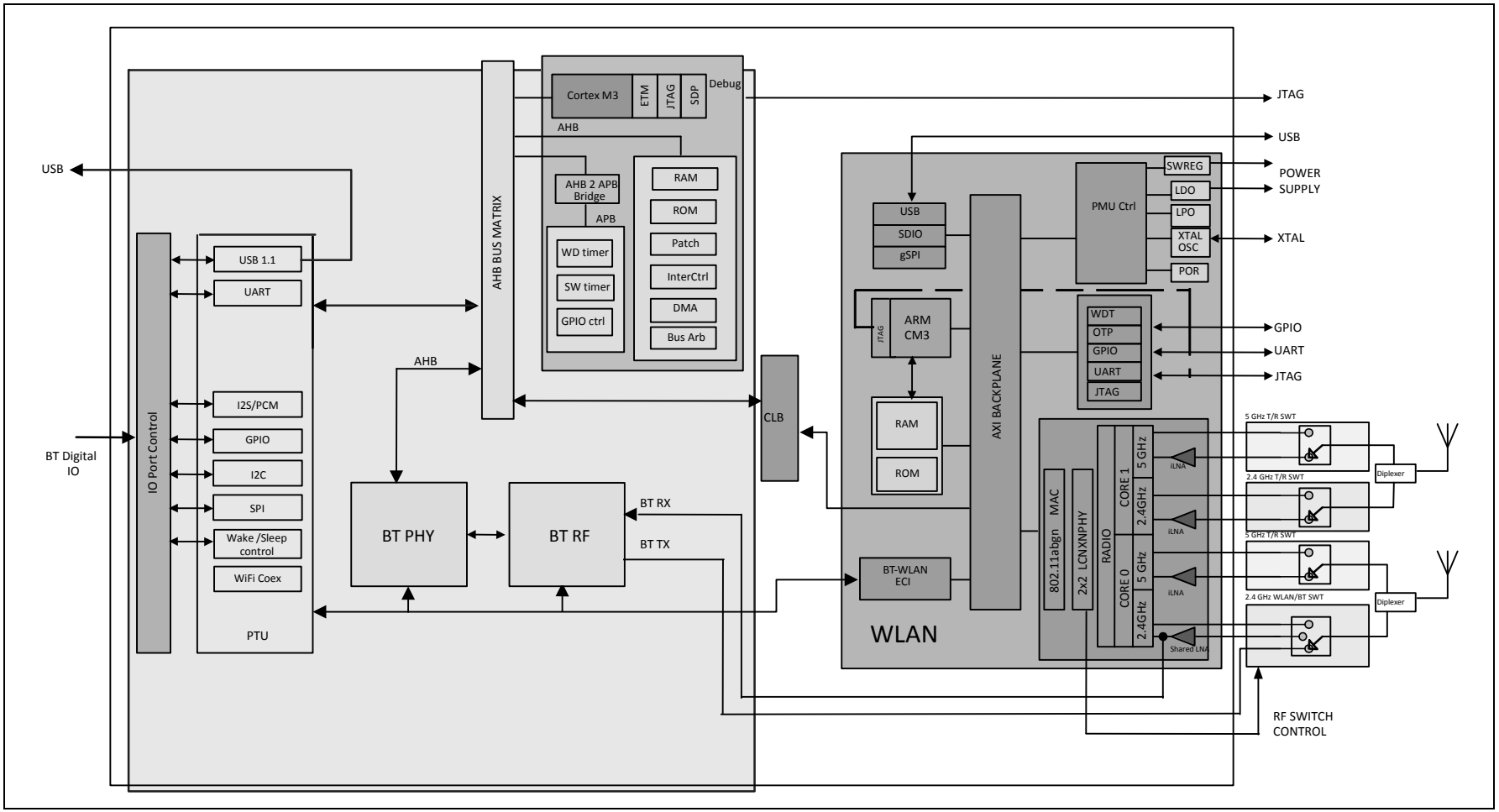
Overview

The Broadcom BCM43242 is a single-ch1ip device for wireless media systems. It integrates the MAC, baseband, and radio of IEEE 802.11 a/b/g and 2 × 2 IEEE 802.11n with Bluetooth 4.0 + HS. BCM43242-based designs require few external components; provide size, form, and function design flexibility; and can be produced in mass volumes at minimal cost.

Comprehensive power management circuitry and software ensure the system can meet the needs of media devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the BCM43242 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2: BCM43242 Block Diagram



Features

The BCM43242 supports the following features:

- IEEE 802.11a/b/g/n dual-band radio—virtual simultaneous dual-band operation
- Bluetooth v4.0 + HS with integrated Class 1 PA
- Concurrent Bluetooth and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single- and dual-antenna support
  - Single antenna with shared LNA
  - Simultaneous BT/WLAN receive with single antenna
- WLAN high-speed USB 2.0 host interface
- BT host digital interface (can be used concurrently with above interfaces):
  - UART (up to 4 Mbps)
  - Full-speed USB 1.1
- ECI—enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- I^2S/PCM for Bluetooth audio
- HCI high-speed UART (H4 and H5) transport support
- Wideband speech support (16 bits linear data, MSB first, left justified at 16K samples/s for transparent air coding, both through I^2S and PCM interfaces)
- Bluetooth low-power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth wideband speech (WBS)
- Multiple simultaneous A2DP audio stream
- MP3 and SBC on-chip decoders for low-power music playback
- Support for encoding SBC streams with input from I^2S and output over A2DP

Standards Compliance

The BCM43242 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0 + HS
- Bluetooth 4.0 (Bluetooth Low Energy)
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11a, IEEE 802.11b, and IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The BCM43242 supports the following future drafts/standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11k—Resource Management
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11r Fast Roaming Support
  - IEEE 802.11k Radio Resource Measurement
- Security:
  - WLAN authentication and privacy infrastructure (WAPI)
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (Hardware Accelerator)
  - TKIP (HW Accelerator)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2, CCXv3, CCXv4, and CCXv5
  - WFAEC
- IEEE 802.15.2 Coexistence Compliance—on silicon solution compliant with IEEE 3 wire requirements

Section 2: Power Supplies and Power Management

Power Supply Topology

One buck regulator, multiple LDO regulators, and a Power Management Unit (PMU) are integrated into the BCM43242. All regulators are programmable via the PMU. These blocks simplify power supply design for WLAN and Bluetooth functions in embedded designs. Regulator inputs and outputs are brought out to pins on the BCM43242. This allows maximum flexibility for the system designer to choose which of the BCM43242 integrated regulators to use.

A 3.3V regulated supply can be used, with all additional voltages being provided by the regulators in the BCM43242.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK, CLDO, and LNLDOs power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDOs may be turned off/on based on the dynamic demands of the digital baseband.

The BCM43242 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNDLO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VDDIO supply) provide the BCM43242 with all the voltages it requires, further reducing leakage currents.

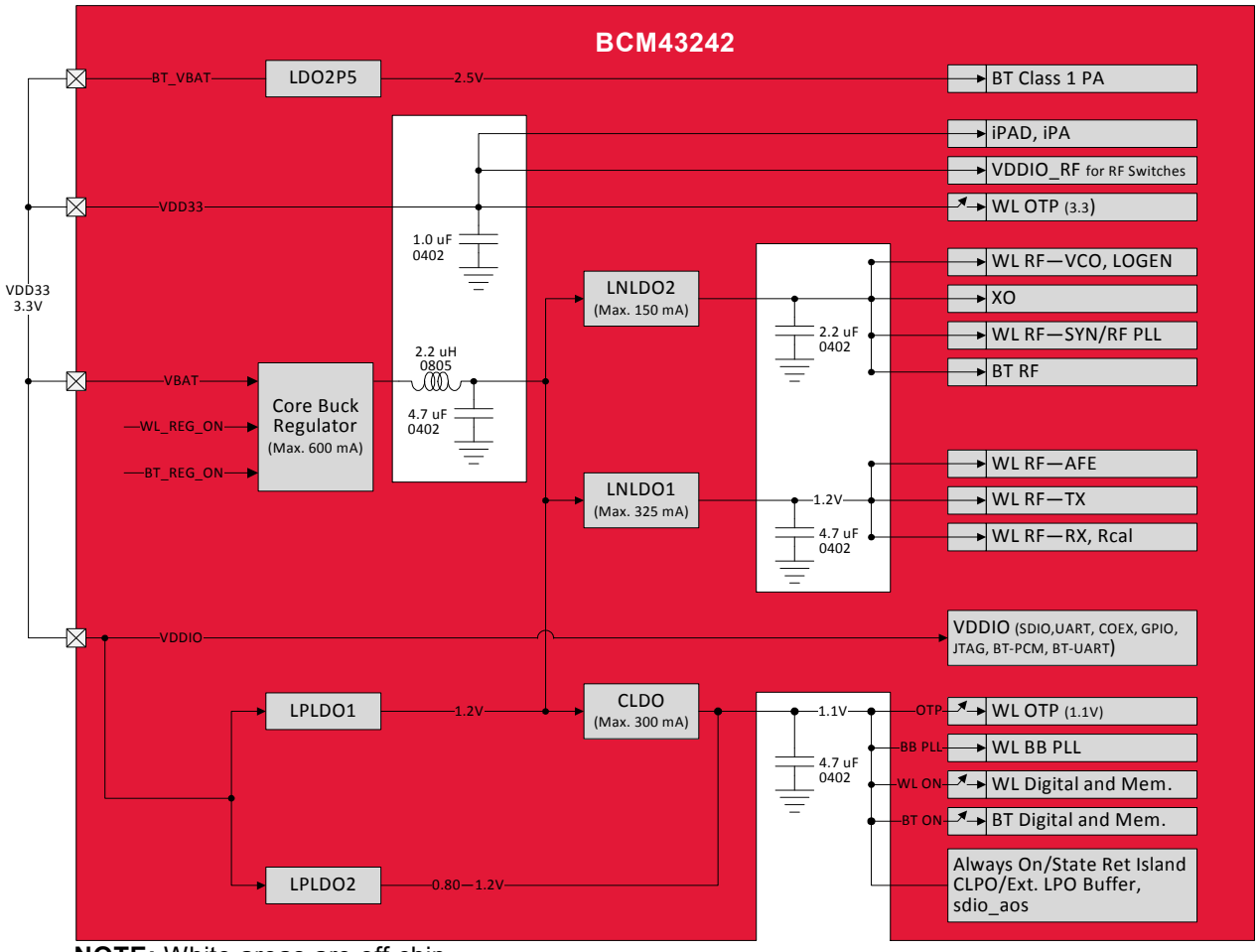
BCM43242 PMU Features

The BCM43242 PMU supplies the following voltages:

- 3.0V to 5.25V (VBAT) down to 1.35 × Vout
- 1.35V to 1.2 × Vout (150 mA and 325 mA maximum) LNLDOs
- 1.35V to 1.2 × Vout (300 mA maximum) CLDO
- Additional internal LDOs (not externally accessible)

Figure 3 on page 17 shows the regulators and a typical power topology: VDD33 is an external regulated supply at 3.3V ±10%. Input to the core buck regulator (VBAT) can be tied to VDD33. The same applies to the input (BT_VBAT) to the BT PA LDO (LDO2P5). VDDIO can also be provided by VDD33.

Figure 3: Typical Power Topology



NOTE: White areas are off-chip.

WLAN Power Management

All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43242 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the BCM43242 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43242 into various power management states appropriate to the current environment and activities that are being performed.

The BCM43242 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the BCM43242 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Power-down mode—The BCM43242 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic, reenabling the internal regulators.

PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Power-Up/Power-Down/Reset Circuits

The BCM43242 has two signals (see Table 1) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 20: “Power-Up Sequence and Timing,” on page 111.

Table 1: Power-Up/Power-Down/Reset Control Signals

Signal	*Description*
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM43242 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal BCM43242 regulators. When this pin is high, the regulators are enabled and the BT section is out of reset. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Section 3: Frequency References

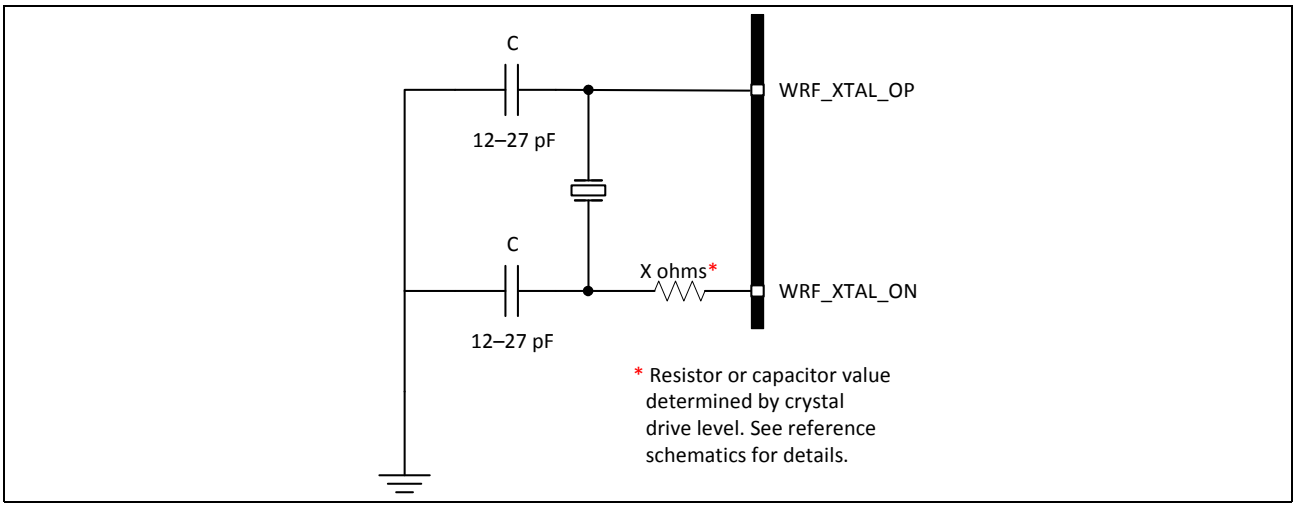
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Note: The crystal and TCXO implementations have different power supplies (WRF_XTAL_VDD1P2 for crystal, WRF_TCXO_VDD for TCXO).

Crystal Interface and Clock Generation

The BCM43242 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 4. Consult the reference schematics for the latest configuration.

Figure 4: Recommended Oscillator Configuration



A fractional-N synthesizer in the BCM43242 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The default frequency reference is a 37.4 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in Table 2 on page 22.

Note: The fractional-N synthesizer can support alternative reference frequencies. Frequencies other than the default, however, require support to be added in the driver plus additional extensive system testing. Contact Broadcom for further details.

TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the Phase Noise requirements listed in Table 2. When the clock is provided by an external TCXO, there are two possible connection methods, shown in Figure 5 and Figure 6:

1. If the TCXO is dedicated to driving the BCM43242, it should be connected to the WRF_XTAL_OP pin through an external 1000 pF coupling capacitor, as shown in Figure 5. The internal clock buffer connected to this pin will be turned OFF when the BCM43242 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P2 pin.
2. For 2.4 GHz operation only, an alternative is to DC-couple the TCXO to the WRF_TCXO_CK pin, as shown in Figure 6. Use this method when the same TCXO is shared with other devices and a change in the input impedance is not acceptable because it may cause a frequency shift that cannot be tolerated by the other device sharing the TCXO. This pin is connected to a clock buffer powered from WRF_TCXO_VDD. If the power supply to this buffer is always on (even in sleep mode), the clock buffer is always on, thereby ensuring a constant input impedance in all states of the device. The maximum current drawn from WRF_TCXO_VDD is approximately 500 µA.

Figure 5: Recommended Circuit to Use with an External Dedicated TCXO

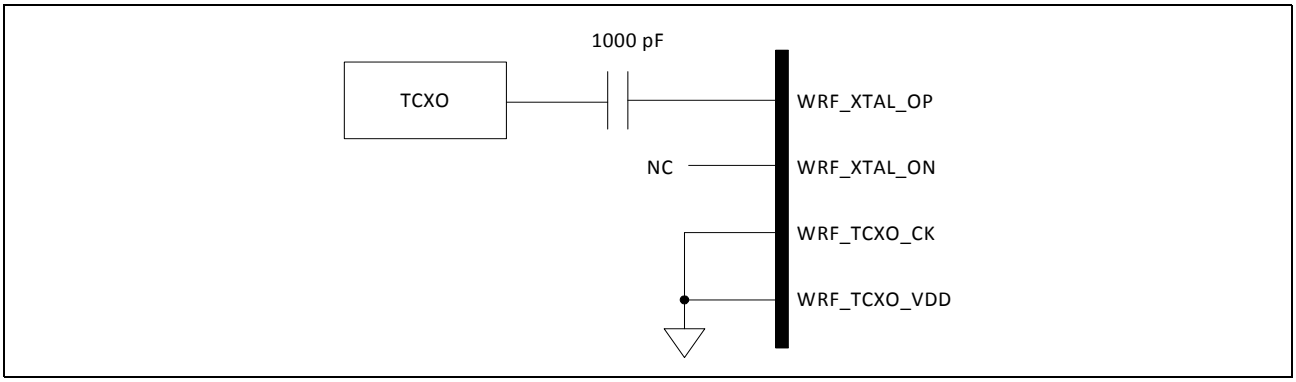


Figure 6: Recommended Circuit to Use with an External Shared TCXO

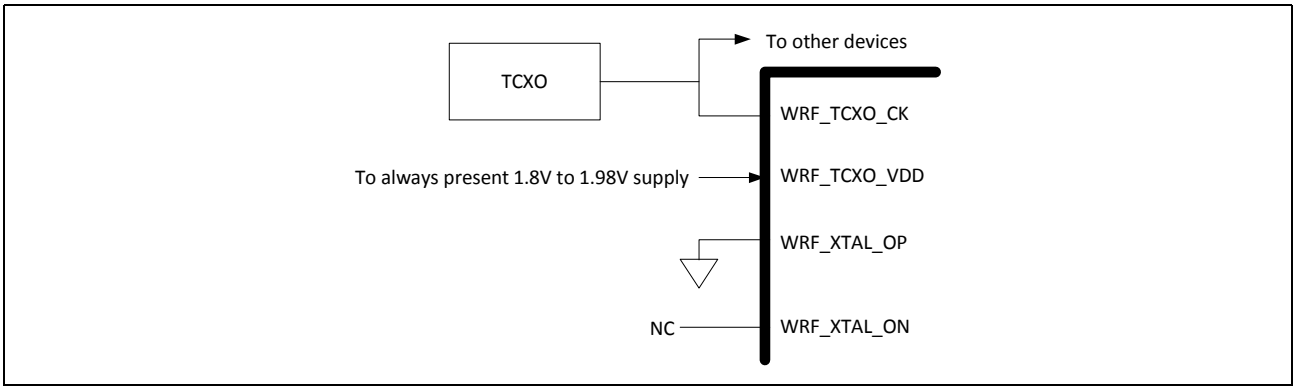


Table 2: Crystal Oscillator and External Clock – Requirements and Performance

		Crystal[a]			External Frequency Reference[b c]			
Parameter	**Conditions/Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Frequency	–	–	37.4	–	–	–	–	MHz
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal specification requirement	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_OP)	Resistive	–	–	–	12k	17k	–	Ω
	Capacitive	–	–	–	–	–	6	pF
Input impedance (WRF_TCXO_IN)	Resistive	–	–	–	17k	31k	–	Ω
	Capacitive	–	–	–	–	–	2	pF
WRF_XTAL_OP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_OP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_OP input voltage (see Figure 5)	AC-coupled analog signal	–	–	–	400	–	1200	mV_{p-p}
WRF_TCXO_IN Input voltage (see Figure 6)	DC-coupled analog signal	–	–	–	400	–	2500	mV_{p-p}
Frequency tolerance Initial + over temp.	Without trimming	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–131	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–138	dBc/Hz
Phase Noise (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–139	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–146	dBc/Hz
Phase Noise (IEEE 802.11n, 2.4 GHz	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–136	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–143	dBc/Hz
Phase Noise (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–144	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–151	dBc/Hz

a. (Crystal) Use WRF_XTAL_OP and WRF_XTAL_ON, internal power to pin WRF_XTAL_VDD1P2.
b. (TCXO) See "TCXO" on page 21 for alternative connection methods.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.

Section 4: Bluetooth Subsystem Overview

The Broadcom BCM43242 is a Bluetooth 4.0 + HS-compliant baseband processor and 2.4 GHz transceiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth radio solution.

The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed USB and UART, and I^2S for audio. The BCM43242 incorporates all Bluetooth 4.0 features including Secure Simple Pairing, Sniff Subrating, Encryption Pause and Resume, and Bluetooth Low Energy.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

Features

Major Bluetooth features include:

- Fully supports Bluetooth Core Specification version 4.0 + (Enhanced Data Rate) EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO)—Voice Connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
  - Bluetooth Low Energy (BLE)
- UART baud rates up to 4 Mbps
- Full-speed USB 1.1
- Supports all Bluetooth 4.0 + HS packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger beacon fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see “Host Controller Power Management” on page 29)
- Channel quality driven data rate and packet type selection

- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and autodetection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.
- Bluetooth peripheral features include the following:
  - SPI for external serial flash access
  - Broadcom Serial Control (BSC) for external EEPROM access. BSC is an I^2C-compatible interface.
  - USB 1.1 and UART host interfaces
  - PCM and I^2S for audio transport
  - Support for 3D glasses

Bluetooth Radio

The BCM43242 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmit

The BCM43242 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates $\pi/4$–DQPSK for 2 Mbps and 8–DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, $\pi/4$–DQPSK, and 8–DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements.

The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the BCM43242 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM43242 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM43242 uses an internal RF and IF loop filter.

Calibration

The BCM43242 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation throughout the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Section 5: Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Bluetooth Low Energy (BLE) operation: This provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.
- Dual-mode Bluetooth Low Energy (BT and BLE operation).
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller, which takes commands from the software, and other controllers, which are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

Test Mode Support

The BCM43242 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM43242 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the BCM43242 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

Host Controller Power Management

When running in UART mode, the BCM43242 may be configured so that dedicated signals are used for power management handshaking between the BCM43242 and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth-defined power saving modes and standby modes of operation.

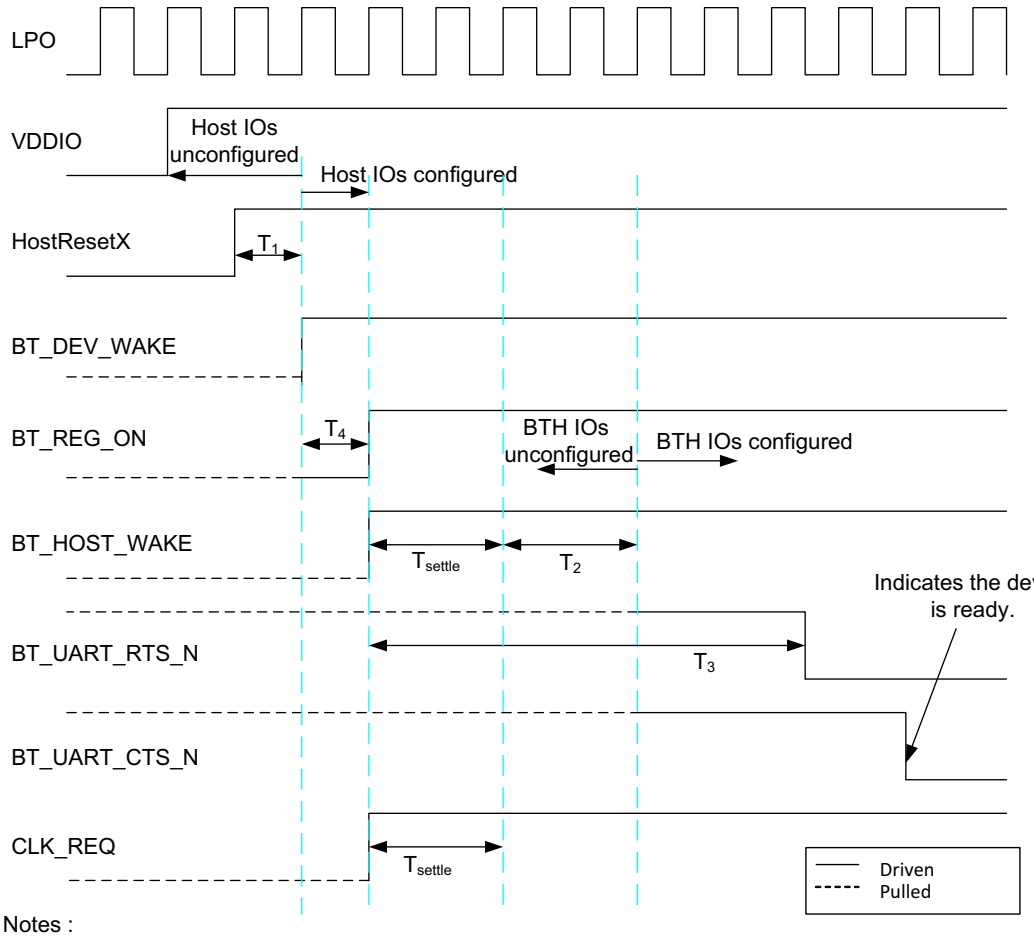
Table 3 describes the power-control handshake signals used with the UART interface.

Table 3: Power Control Pin Description

Signal	*Type*	*Description*
BT_DEV_WAKE	I	Bluetooth device wake-up: Signal from the host to the BCM43242 indicating that the host requires attention. • Asserted: The Bluetooth device must wake up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	O	Host wake-up. Signal from the BCM43242 to the host indicating that the BCM43242 requires attention. • Asserted: Host device must wake up or remain awake. • Deasserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_CLK_REQ	O	The BCM43242 asserts BT_CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the BCM43242 powers up or resets when VDDIO is present.

Note: Pad function Control Register is set to 0 for these pins. See "Multiplexed Bluetooth Digital I/O Signals" on page 80 for more details.

Figure 7: Start-up Signaling Sequence



Notes :

- T_1 is the time for host to settle its IOs after a reset.
- T_2 is the time for the BTH device to settle its IOs after a reset and ref clk settling time elapsed.
- T_3 is the time for the BT device to complete initialization and drive BT_UART_RTS_N low.
- T_4 is the setup time for BT_WAKE prior to driving BT_REG_ON high; BT_DEV_WAKE must be high prior to BT_REG_ON being released. BT_DEV_WAKE should not be driven low until after the host has completed configuration.
- T_{settle} is the time for the ref clk signal from the host to be guaranteed to have settled.

BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the BCM43242 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the BCM43242 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the BCM43242 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

  During the low-power shutdown state, provided VDDIO remains applied to the BCM43242, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the BCM43242 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

  One BCM43242 input signal is designed to be a high-impedance input that does not load the driving signal, even if the chip does not have VDDIO power supplied to it. That signal is the frequency reference input (WRF_TCXO_IN). When the BCM43242 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

Adaptive Frequency Hopping

The BCM43242 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

Advanced Bluetooth/WLAN Coexistence

The BCM43242 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The BCM43242 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The BCM43242 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The BCM43242 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core’s channel information.

Fast Connection (Interlaced Page and Inquiry Scans)

The BCM43242 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

Section 6: Bluetooth Media Support

The BCM43242 provides superior total system current during music or audio playback and recording. To enable these functions, several features of the device are combined to provide superior system power consumption.

Wideband Speech

The BCM43242 provides support for wideband speech (WBS). The BCM43242 can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bitstream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bitstream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The BCM43242 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 8 and Figure 9 show audio waveforms with and without Packet Loss Concealment. Broadcom PLC/BEC algorithms also support wideband speech.

Figure 8: CVSD Decoder Output Waveform Without PLC

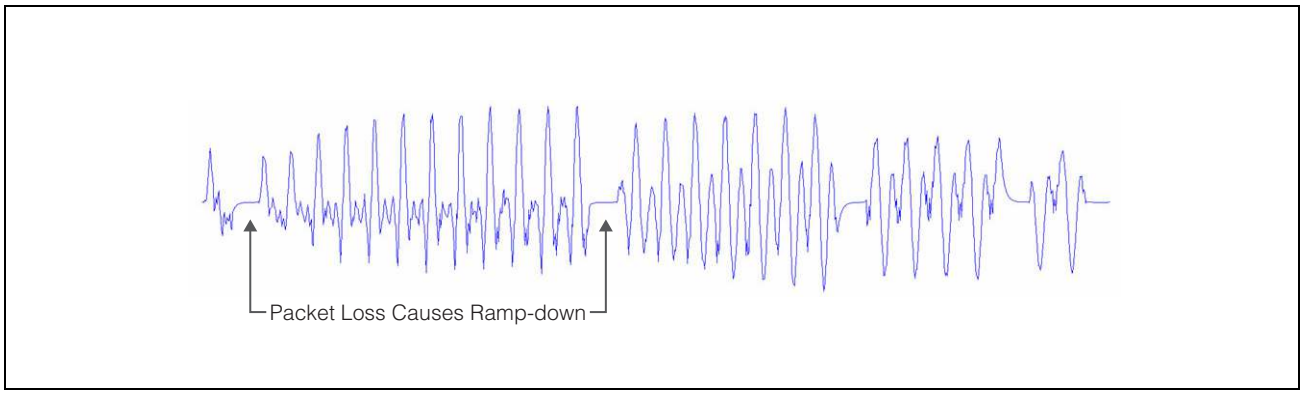
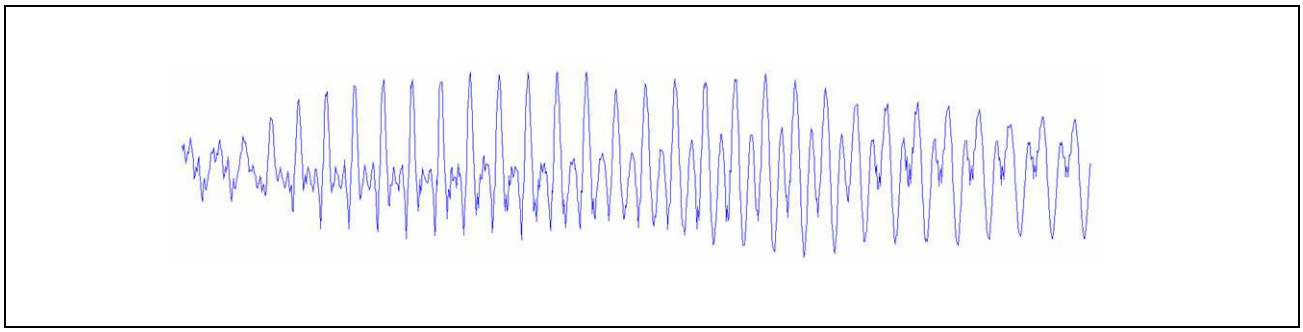


Figure 9: CVSD Decoder Output Waveform After Applying PLC



Encoders

The BCM43242 can support SBC and mSBC encoding and decoding for wideband speech.

Decoders

The BCM43242 includes an MP3 decoder that supports mono and stereo audio recording with the following specifications:

- Supports MPEG-1 Layer 3 decoding
- Output is fully bit compliant with MPEG-1 standard specification
- Supports sampling frequencies from 32 kHz to 48 kHz
- Minimum bit-rate supported 32 kbps and maximum bit-rate supported 320 kbps for Layer 3

Multiple Simultaneous A2DP Audio Streams

The BCM43242 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

Burst Buffer Operation

The BCM43242 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

SBC Offloading Support

The BCM43242 can help offload the host by encoding an audio stream received over I^2S and transmitting it over A2DP. This can be configured by the host via Bluetooth HCI vendor-specific commands.

3D DTV Support

The BCM43242 has hardware and firmware resources required for supporting operation of compatible Bluetooth 3D glasses. The 3D feature allows for periodically sending TV vertical-frame timing information and related parameters to the 3D glasses to enable proper viewing of 3D media.

Section 7: Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM® Cortex-M3™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 606 KB of ROM memory for program storage and boot ROM, 166 KB of RAM for data scratch-pad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the BCM43242 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the BCM4329 and BCM4330 devices.

RAM, ROM, and Patch Memory

The BCM43242 Bluetooth core has 173 KB of internal RAM which is mapped between general-purpose scratch pad memory and patch memory and 680 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

Reset

The BCM43242 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

Section 8: Bluetooth Peripheral Transport Unit

PCM Interface

The BCM43242 supports two independent PCM interfaces that share the pins with the I^2S interfaces. The PCM Interface on the BCM43242 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM43242 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43242.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Slot Mapping

The BCM43242 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The BCM43242 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is 3-bit periods, and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The BCM43242 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM43242 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The BCM43242 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. Also, the PCM bus can operate at a rate of up to 24 MHz in this mode. This mode of operation is initiated with an HCI command from the host.

PCM Interface Timing

Short Frame Sync, Master Mode

Figure 10: PCM Timing Diagram (Short Frame Sync, Master Mode)

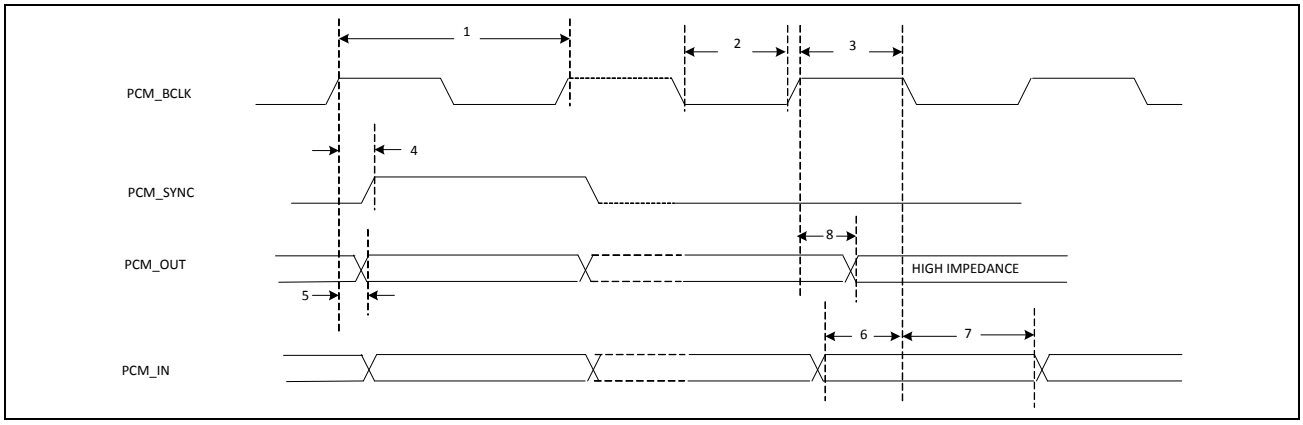


Table 4: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 11: PCM Timing Diagram (Short Frame Sync, Slave Mode)

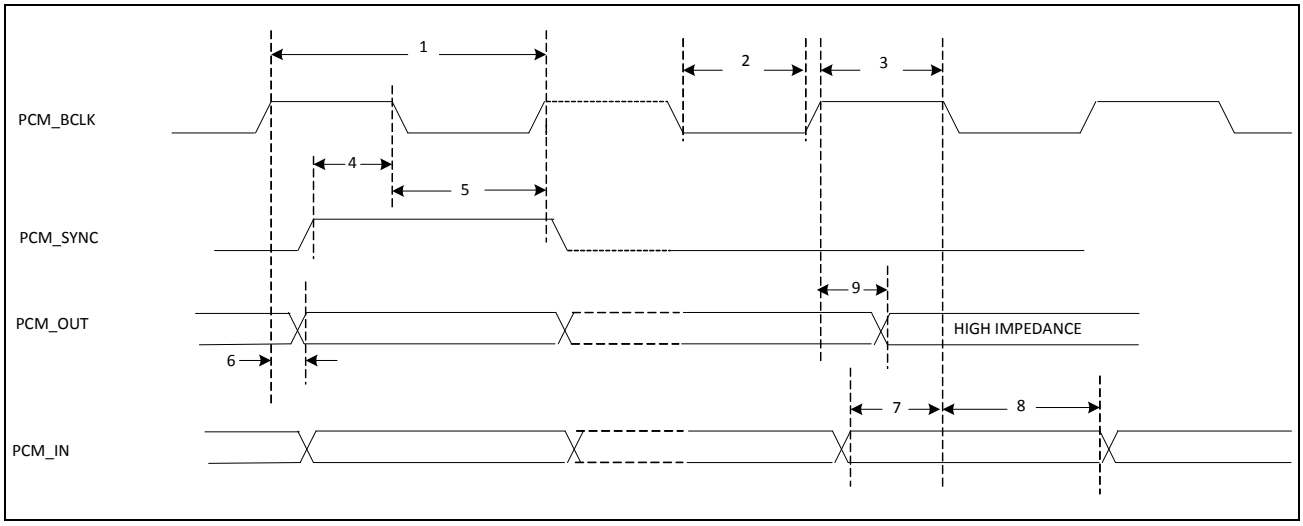


Table 5: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

Figure 12: PCM Timing Diagram (Long Frame Sync, Master Mode)

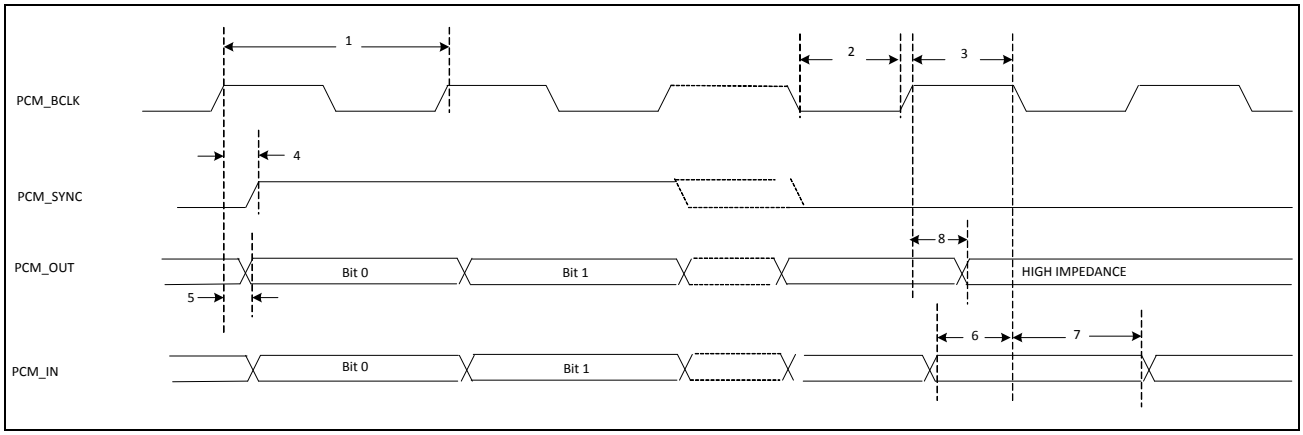


Table 6: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 13: PCM Timing Diagram (Long Frame Sync, Slave Mode)

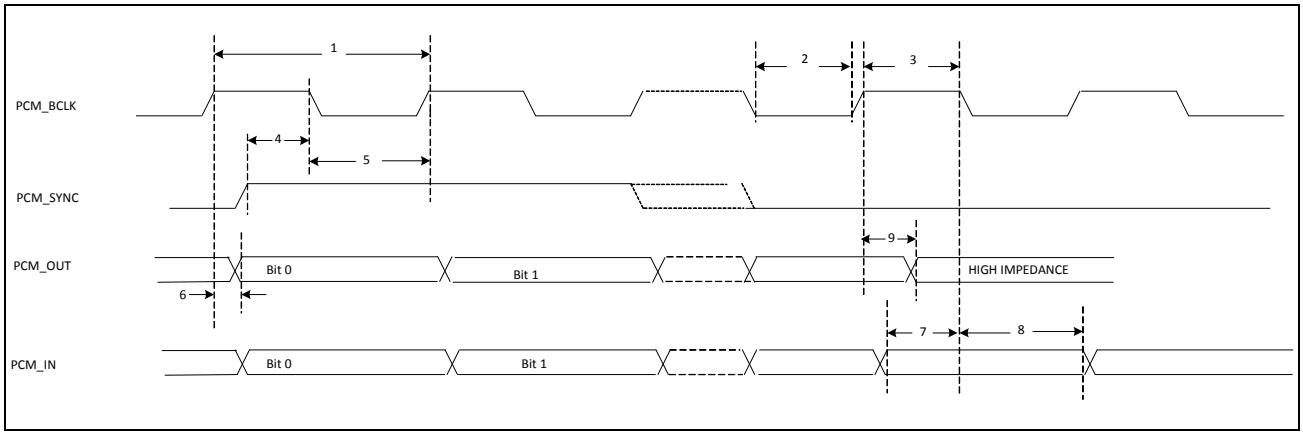


Table 7: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock HIGH	41	–	–	ns
3	PCM bit clock LOW	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

Figure 14: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

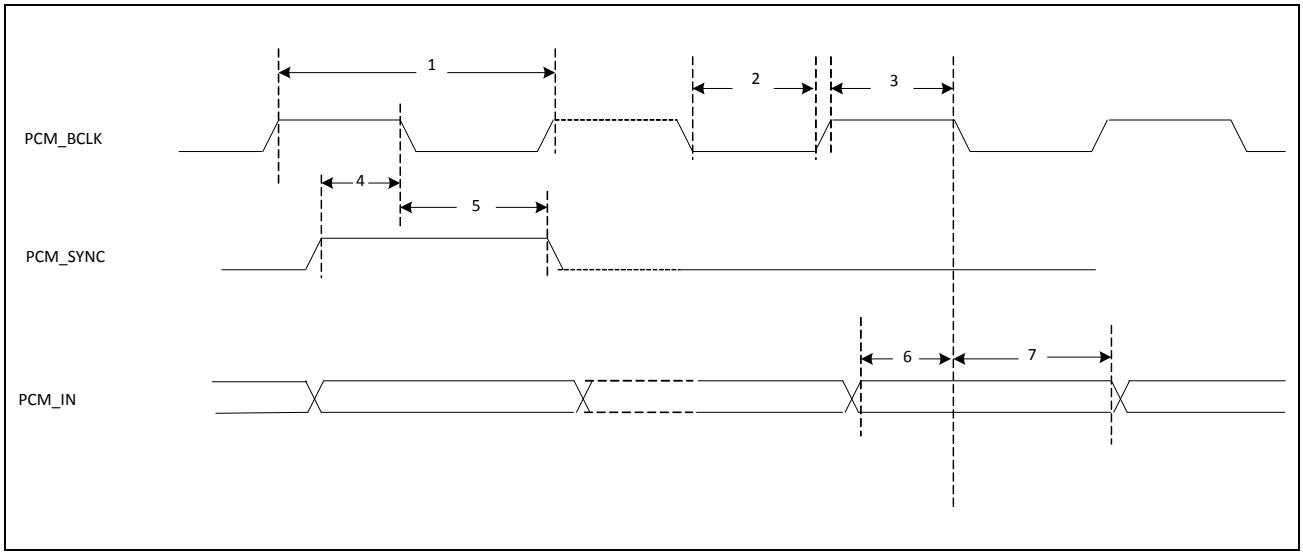


Table 8: PCM Burst Mode (Receive Only, Short Frame Sync)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock HIGH	20.8	–	–	ns
3	PCM bit clock LOW	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

Figure 15: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

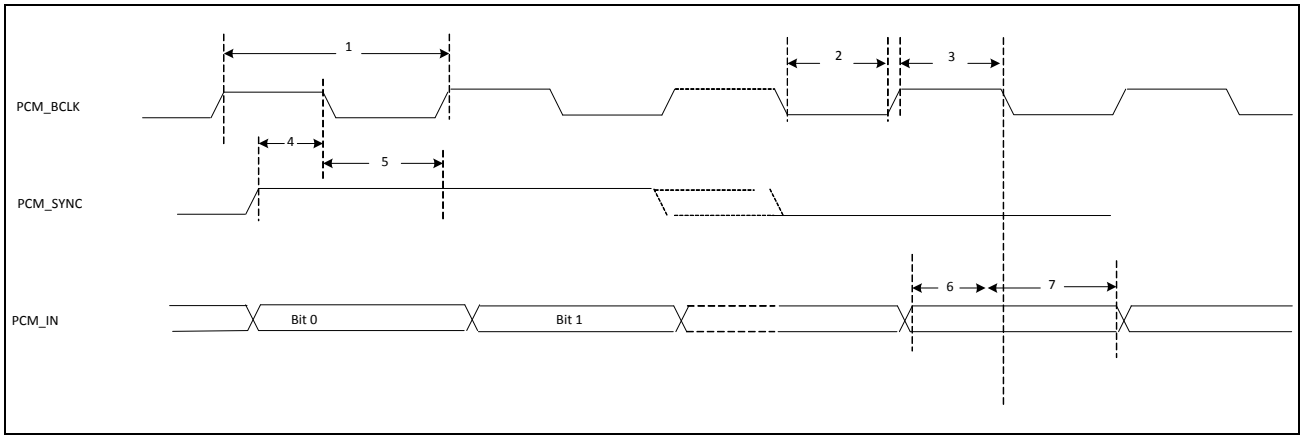


Table 9: PCM Burst Mode (Receive Only, Long Frame Sync)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock HIGH	20.8	–	–	ns
3	PCM bit clock LOW	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

UART Interface

The BCM43242 has a single UART for Bluetooth host communication. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4 and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM43242 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM43242 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 10: Example of Common Baud Rates

Desired Rate	*Actual Rate*	*Error (%)*
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 16: UART Timing

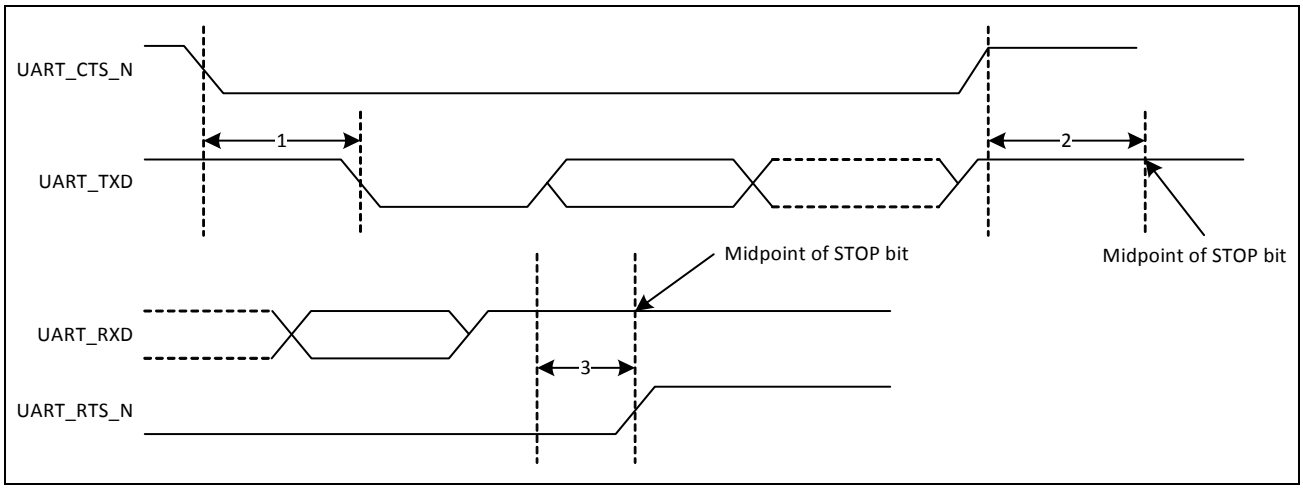


Table 11: UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

I2S Interface

The BCM43242 supports an independent I2S digital audio port for Bluetooth audio. The I2S signals are:

- I2S clock: I2S SCK
- I2S Word Select: I2S WS
- I2S Data Out: I2S SDO
- I2S Data In: I2S SDI

I2S SCK and I2S WS become outputs in master mode and inputs in slave mode, while I2S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I2S bus, per the I2S specification. The MSB of each data word is transmitted one bit clock cycle after the I2S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I2S WS is low, and right-channel data is transmitted when I2S WS is high. Data bits sent by the BCM43242 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

I²S Timing

Note: Timing values specified in Table 12 are relative to high and low threshold levels.

Table 12: Timing for I²S Transmitters and Receivers

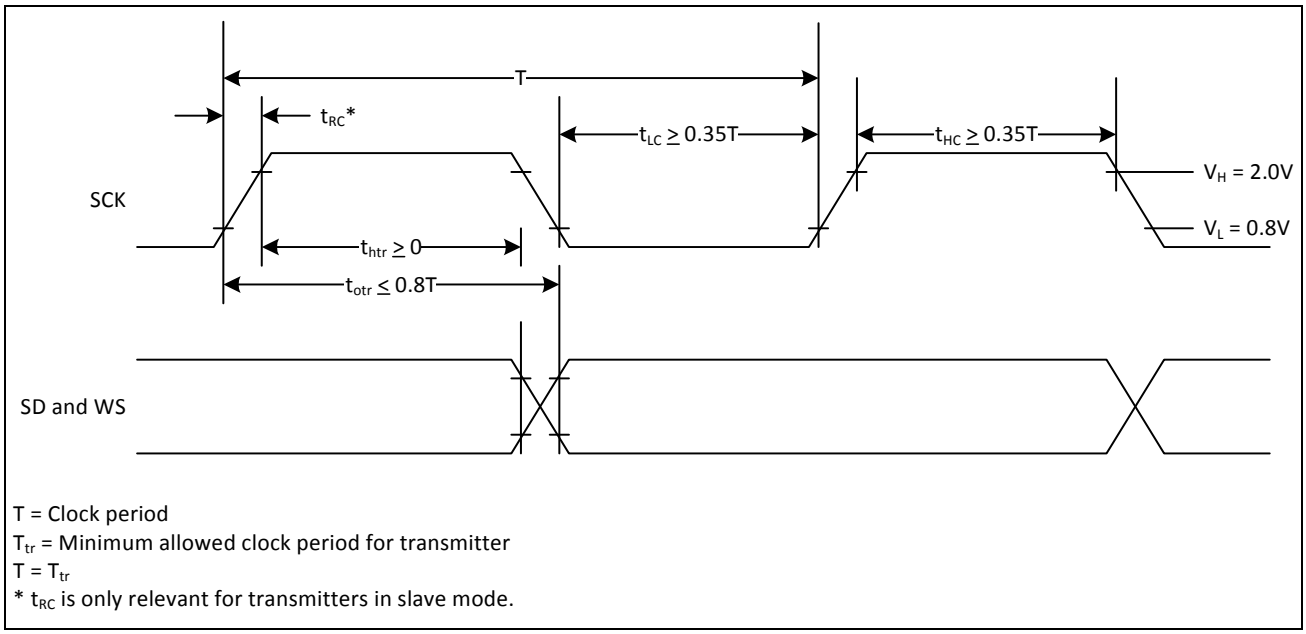
	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	1
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	4
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	5
Hold time t_{htr}	0	–	–	–	–	–	–	–	4
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time t_{hr}	–	–	–	–	–	0	–	–	6

Note:

- The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
- Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC}, which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- The data setup and hold time must not be less than the specified receiver setup and hold time.

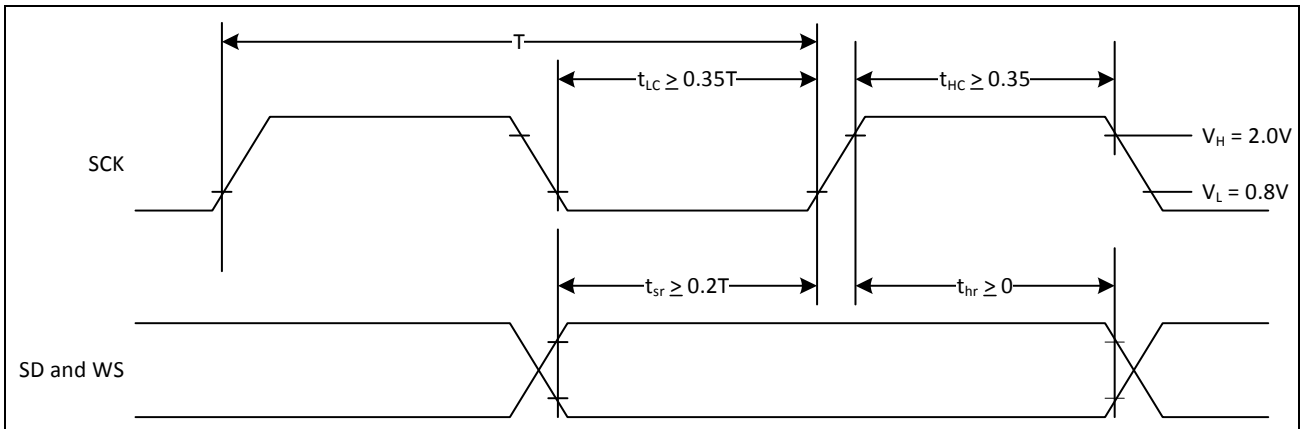
Note: The time periods specified in Figure 17 and Figure 18 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 17: I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 18: I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Section 9: WLAN Global Functions

WLAN CPU and Memory Subsystem

The BCM43242 includes an integrated ARM Cortex-M3™ processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for Thumb®-2 instruction set. ARM Cortex-M3 delivers 30% more performance gain over ARM7TDMI.

At 0.19 µW/MHz, the Cortex-M3 is the most power-efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for Code and Data access (ICode/DCode and System buses). ARM Cortex-M3 supports extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 544 KB RAM and 640 KB ROM.

One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 3072-bit One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

GPIO Interface

The BCM43242 has 13 general-purpose I/O (GPIO) that can be used to connect to various external devices.

Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. An internal (programmable) pull-up/pull-down resistor is included on each GPIO.

External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external colocated wireless device, such as GPS, WiMAX, or UWB, to manage wireless medium sharing for optimum performance. The following signals can be enabled by software on the indicated WLAN GPIO pins:

- ERCX_STATUS GPIO_2
- ERCX_FREQGPIO_3
- ERCX_RF_ACTIVEGPIO_4
- ERCX_TXCONFGPIO_5
- ERCX_PRISELGPIO_12

UART Interface

One UART interface can be enabled by software as an alternate function on pins UART_RX (muxed on GPIO_6) and UART_TX (muxed on GPIO_7). Provided primarily for debugging during development, this UART enables the BCM43242 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of 64 × 8 in each direction.

JTAG Interface

The BCM43242 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

The JTAG interface (multiplexed on the GPIO pins) is enabled when the JTAG_SEL pin is asserted high. The JTAG to GPIO signal mapping is as follows:

- TCKGPIO_2
- TMSGPIO_3
- TDIGPIO_4
- TDOGPIO_5

Section 10: USB Interfaces

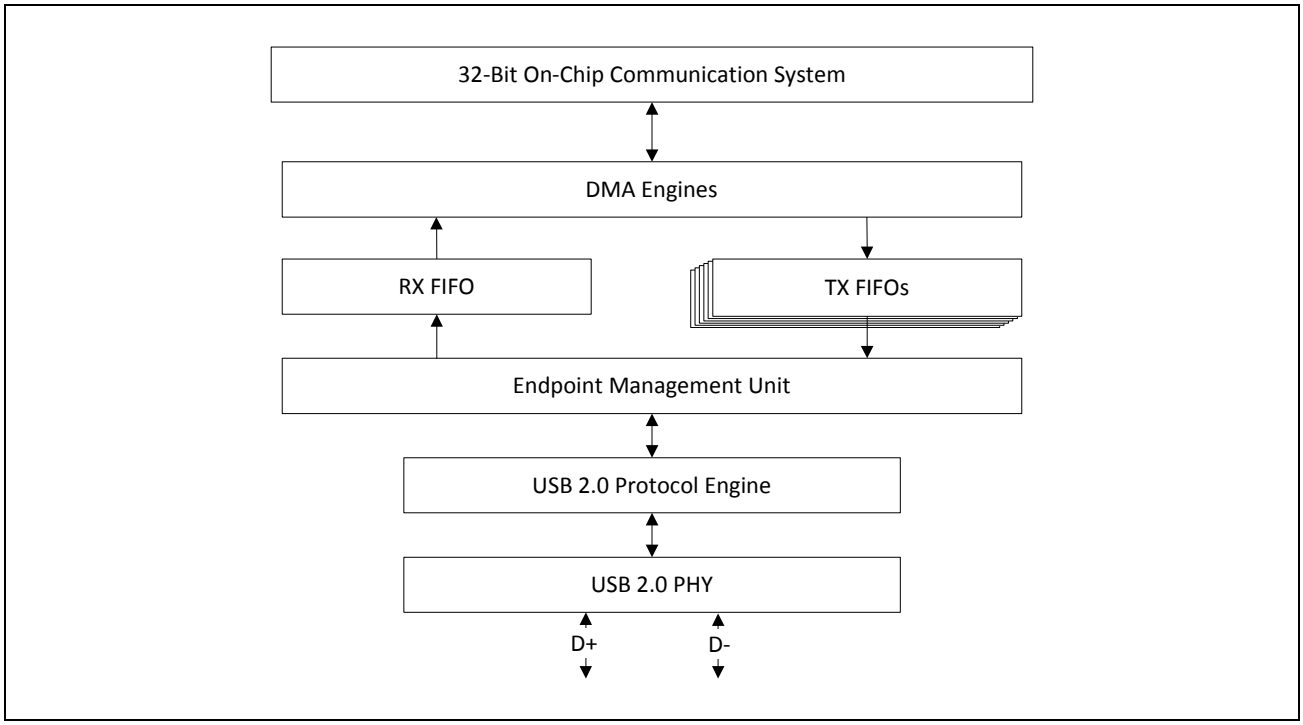
WLAN USB 2.0 Interface

The BCM43242 USB interface can be set to operate as a USB 2.0 port. Features include the following:

- A USB 2.0 protocol engine that supports the following:
  - A Parallel Interface Engine (PIE) between packet buffers and USB transceiver
  - Up to nine endpoints, including Configurable Control Endpoint 0
- Separate endpoint packet buffers with a 512-byte FIFO buffer each
- Host-to-device communication for bulk, control, and interrupt transfers
- Configuration and status registers

Figure 19 shows the blocks in the device core.

Figure 19: WLAN USB 2.0 Host Interface Block Diagram



The USB 2.0 PHY handles the USB protocol and the serial signaling interface between the host and device. It is primarily responsible for data transmission and recovery. On the transmit side, data is encoded, along with a clock, using the NRZI scheme with bit stuffing to ensure that the receiver detects a transition in the data stream. A SYNC field that precedes each packet enables the receiver to synchronize the data and clock recovery circuits. On the receive side, the serial data is deserialized, unstuffed, and checked for errors. The recovered data and clock are then shifted to the clock domain that is compatible with the internal bus logic.

The endpoint management unit contains the PIE control logic and the endpoint logic. The PIE interfaces between the packet buffers and the USB transceiver. It handles packet identification (PID), USB packets, and transactions.

The endpoint logic contains nine uniquely addressable endpoints. These endpoints are the source or sink of communication flow between the host and the device. Endpoint zero is used as a default control port for both the input and output directions. The USB system software uses this default control method to initialize and configure the device information and allows USB status and control access. Endpoint zero is always accessible after a device is attached, powered, and reset.

Endpoints are supported by 512-byte FIFO buffers, one for each IN endpoint and one shared by all OUT endpoints. Both TX and RX data transfers support a DMA burst of 4, which guarantees low latency and maximum throughput performance. The RX FIFO can never overflow by design. The maximum USB packet size cannot be more than 512 bytes.

Bluetooth USB 1.1 Host Interface

The BCM43242 has a USB 1.1 host interface for Bluetooth. Features include the following:

- A 90Ω differential interface
- USB signal absolute maximum voltage range from –0.5V to 5.25V

Section 11: Wireless LAN MAC and PHY

MAC Features

The BCM43242 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

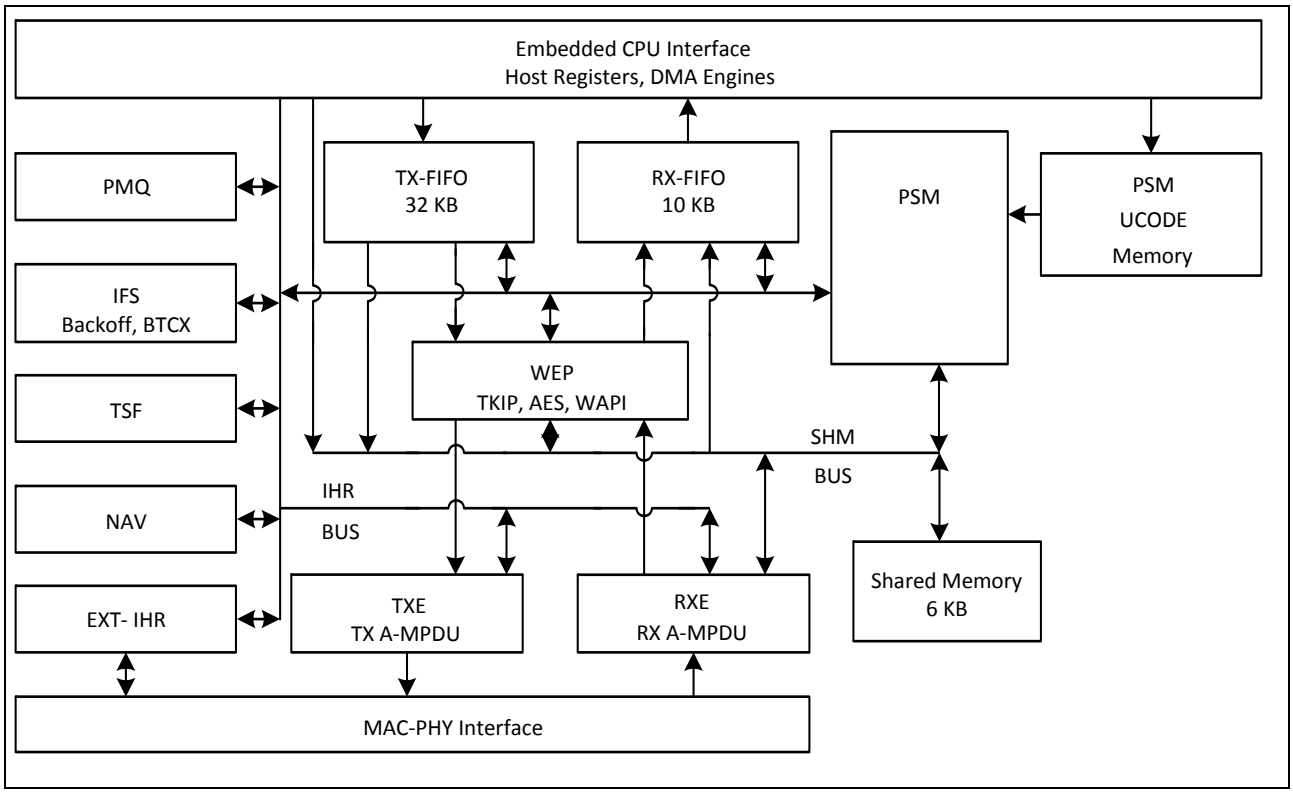
- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

MAC Description

The BCM43242 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 20 on page 54.

The following sections provide an overview of the important modules in the MAC.

Figure 20: WLAN MAC Architecture



PSM

The programmable state machine (PSM) is a microcoded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are colocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratch-pad, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface, which can be controlled either by the host or by the PSM to configure and control the PHY.

WLAN PHY Description

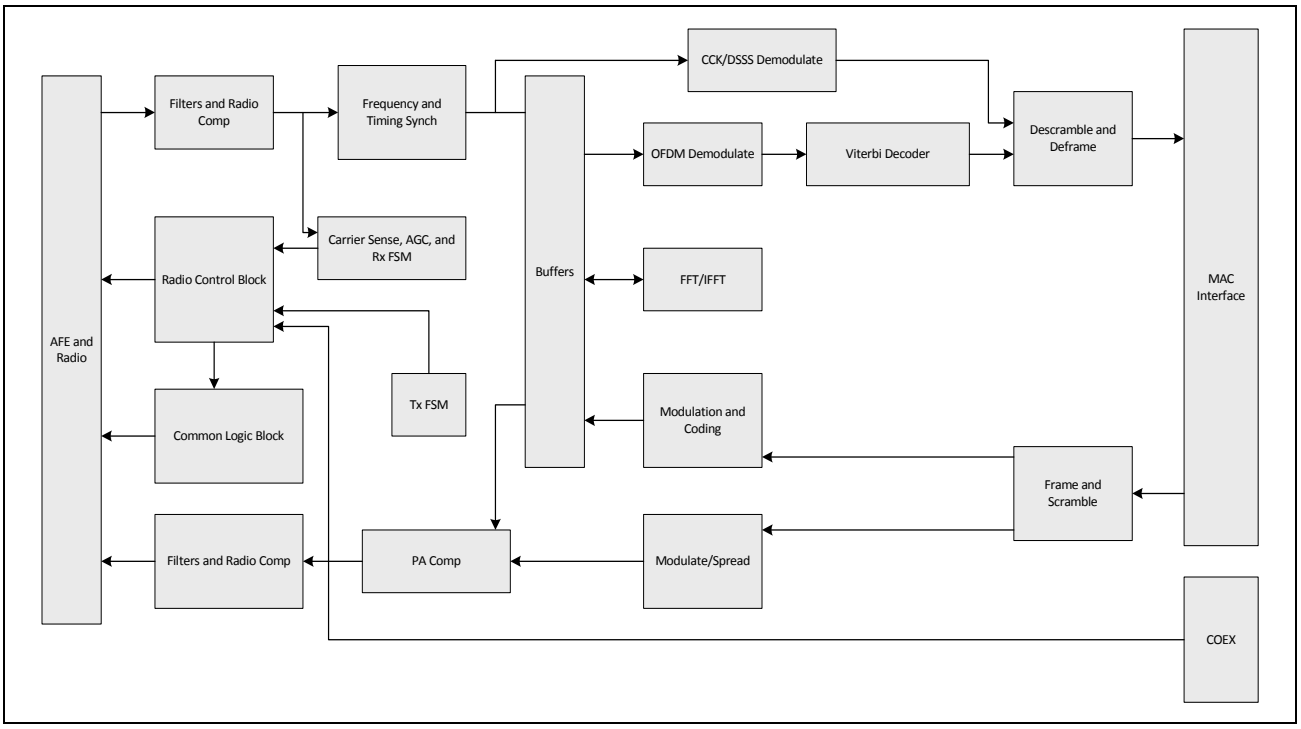
The BCM43242 supports IEEE 802.11a/b/g/n dual-stream to provide maximum data rates up to 300 Mbps.

The PHY has been designed to work with interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous RX.

PHY Features

- Supports IEEE 802.11a, 11b, 11g, and 11n dual-stream PHY standards
- IEEE 802.11n dual-stream operation in 20 MHz and 40 MHz channels
- Supports Optional Short GI and Green Field modes in TX and RX
- Supports optional space-time block code (STBC) receive of two space-time streams
- Supports IEEE 802.11h/k for worldwide operation
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Supports power saving schemes such as single-core listen (OCL), single-core demodulation of SISO/STBC packets based on RSSI, and dynamic ML turn-off based on RSSI
- Algorithms to improve performance in presence of Bluetooth
- Simultaneous RX (WL-BT) architecture
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications
- Closed-loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet RX antenna diversity for IEEE 802.11b PHY rates.
- Designed to meet FCC and other worldwide regulatory requirements
- TX LDPC for improved range and power efficiency
- Hardware support for faster switch times between channels/bands

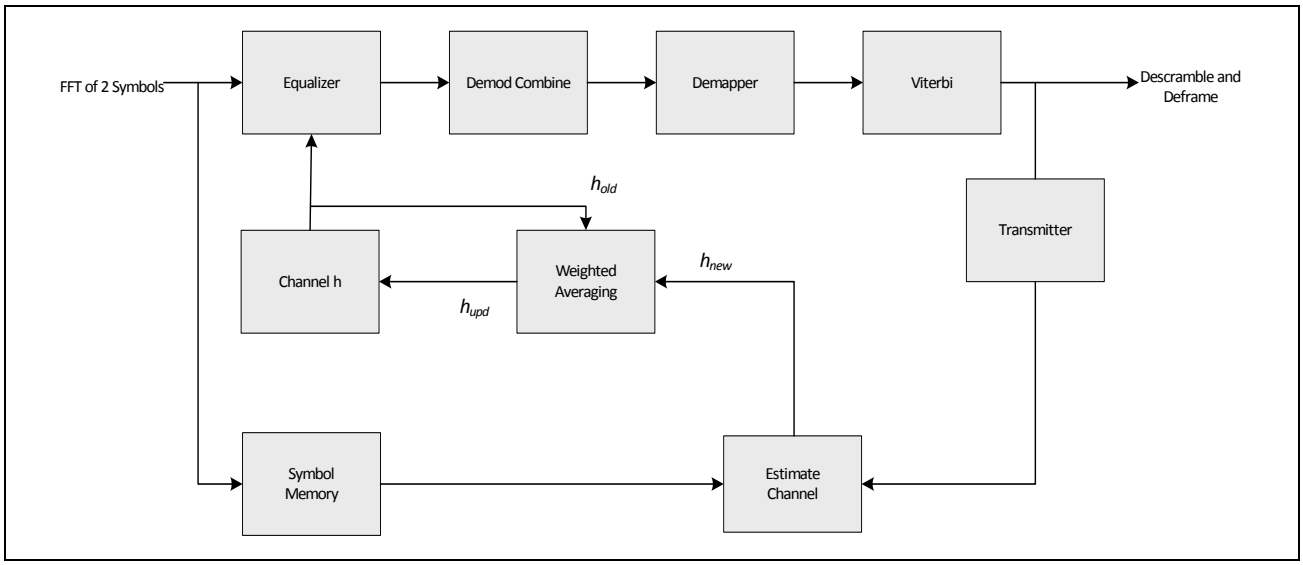
Figure 21: WLAN PHY Block Diagram



The PHY is capable of fully calibrating the RF front end to extract the highest performance. On power-up, the PHY performs a full suite of calibration to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift thus maintaining high-performance over time. A closed loop transmit control algorithm maintains the output power to required level with capability control TX power on a per packet basis.

One of the key feature of the PHY is two space-time stream receive capability. The STBC scheme can obtain diversity gains by using multiple transmit antennas in AP (Access Point) in a fading channel environment, without increasing the complexity at the STA. Details of the STBC receive are shown in the block diagram in Figure 22 on page 59.

Figure 22: STBC Receive Block Diagram



In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. Channel estimate is refined on every pair of symbols using the received symbols and reconstructed symbols.

Section 12: WLAN Radio Subsystem

The BCM43242 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems (but not both simultaneously). It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Up to 11 RF control signals are available to drive the external RF switches and support external power amplifiers and low noise amplifiers for each band. See the reference board schematics for further details.

Receiver Path

The BCM43242 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. Control signals are available that can support the use of optional external low noise amplifiers (LNA), which can increase the receive sensitivity by several dB.

Transmit Path

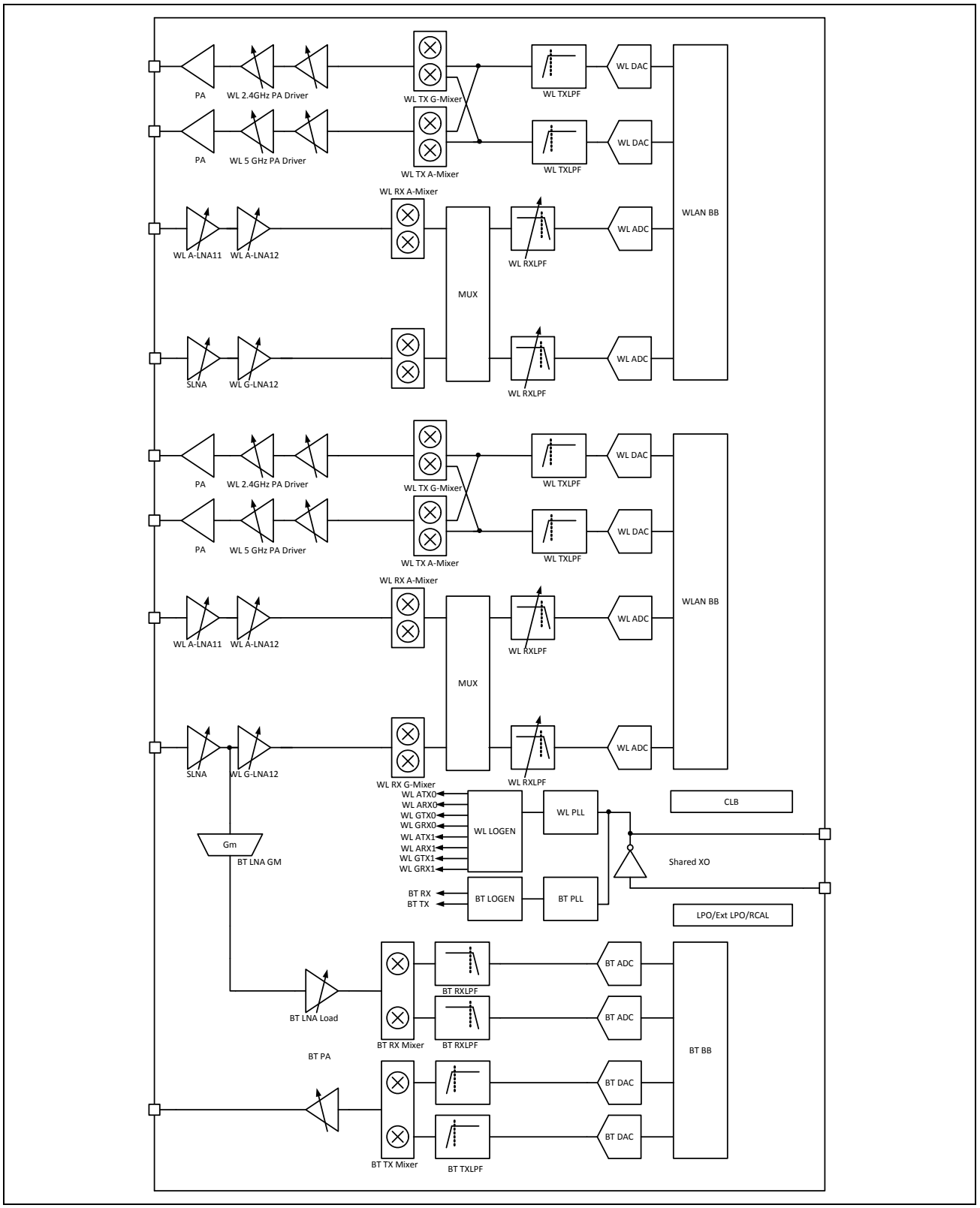
Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively.

Linear on-chip power amplifiers are included for both 2.4 GHz and 5 GHz. Closed loop power control is also provided, as are spare RF control signals that can be used to support external RF switches for either or both bands.

Calibration

The BCM43242 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variation across components. This enables the BCM43242 to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip.

Figure 23: Radio Functional Block Diagram



Section 13: Pinouts and Signal Descriptions

Ball Map

Figure 24 on page 63 shows the first page of the ball map (top view).

Figure 25 on page 64 shows the second page of the ball map (top view).

Figure 24: FCFBGA Ball Map Top View—Page 1 of 2

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	BT_UART_CTS_N		BT_GPIO_4		BT_USB_DN	BT_USB_DP		BT_PCM_OUT		RF_SW_CTRL_6		A
B	VSS	VSS	BT_UART_RTS_N	BT_GPIO_5	BT_I2S_WS	BT_PCM_SYNC	VSS	BT_PCM_IN	BT_PCM_CLK		RF_SW_CTRL_7	RF_SW_CTRL_5	B
C	BT_UART_RXD	BT_UART_TXD											C
D		BT_I2S_CLK											D
E	BT_I2S_DI	BT_I2S_DO			BT_VDDC_ISO_1		VSS	VSS	BT_GPIO_3	BT_GPIO_2	VSS	GMODE_EXT_LNA_PU_CORE0	E
F		BT_CLK_REQ			BT_VDDC_ISO_2								F
G	BT_DEV_WAKE	BT_HOST_WAKE			BT_VDDO								G
H		VSS			BT_TM1								H
J	BT_VCOVDD	BT_PLLVDD						BTRGND		OTP_VDD33			J
K	BT_LNAVDD	BTRGND			BTVDD			BTRGND		BT_VDDC	VDDIO_RF		K
L		BT_IFVDD			BTRGND					BT_VDDC	VDD		L
M	BT_RF	BTRGND			BTRGND			BTRGND	BTRGND	VSS			M
N		V_BTBAT			BTRGND				BTRGND			VDD	N
P	BT_PAVDD	BTRGND			BTRGND			BTRGND		VSS		VDD	P
R	WRF_RFIN_2G_CORE0	RGND			RGND		RGND	RGND	RGND	RGND	VSS	VSS	R
T	RGND	RGND			RGND		RGND	RGND		RGND	RGND		T
U	WRF_PAOUT_2G_CORE0	RGND			WRF_RX2G_VDD1P2_CORE0			RGND			RGND		U
V	RGND	RGND			RGND			RGND	RGND		RGND		V
W	WRF_PADRV2G_VDD3P3_CORE0	RGND			RGND	RGND	RGND	WRF_GPIO_OUT	RGND	WRF_AFE_VDD1P2_CORE0	RGND	WRF_RX2G_VDD1P2_CORE1	W
Y	RGND	RGND											Y
AA	WRF_PA_VDD3P3_CORE0	RGND											AA
AB	WRF_PADRV5G_VDD3P3_CORE0	RGND	RGND	RGND	RGND	WRF_TX_VDD1P2_CORE0	RGND	WRF_RX5G_VDD1P2_CORE0	RGND	WRF_TX_VDD1P2_CORE1	RGND	RGND	AB
AC	RGND	WRF_PAOUT_5G_CORE0	RGND	WRF_RFIN_5G_CORE0	RGND	RGND	WRF_VCO_VDD1P2		WRF_SYNTH_VDD1P2	RGND	WRF_RFIN_2G_CORE1	RGND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 25: FCFBGA Ball Map Top View—Page 2 of 2

	13	14	15	16	17	18	19	20	21	22	23	
A	RF_SW_ CTRL_3		GPIO_7		GPIO_8		GPIO_6		GPIO_3		GPIO_0	A
B	RF_SW_ CTRL_1	RF_SW_ CTRL_4	RF_SW_ CTRL_2	RF_SW_ CTRL_0	GPIO_2	JTAG_SEL	GPIO_12	GPIO_9	GPIO_4	GPIO_5	GPIO_1	B
C										SR_VLX	SR_VLX	C
D										SR_PVSS	SR_PVSS	D
E	AMODE_EXT_ LNA_PU_CORE0		EXT_XTAL_PU							SR_PVSS	SR_PVSS	E
F							**PMU_AVSS**			SR_ VDDBATP5V	SR_ VDDBATP5V	F
G										SR_ VDDBATA5V	SR_ VDDBATA5V	G
H										VOUT_CLDO	VOUT_CLDO	H
J		GPIO_11		WLREG_ON			VOUT_LNLDO2			VOUT_LNLDO1	VOUT_LNLDO1	J
K	GPIO_10	VSS		VDDIO			VSS			LDO_VDD1P5	LDO_VDD1P5	K
L	VDD	VDD		BTREG_ON			AVSS			VSS	VSS	L
M		VDD		VSS			MONPLL			AVDD33		M
N		VDD					AVDD_BBPLL			RREF	DP	N
P	VDD	VDD	VSS	VSS			VDDIO_RF			VSS	DM	P
R	VSS	VSS	VSS				AMODE_EXT_ LNA_PU_CORE1			MONCDR	DVSS	R
T	RGND	RGND		RGND	WRF_XTAL_ CAB_GND1P2		VSS			VSS		T
U	RGND			RGND			WRF_XTAL_ CAB_GND1P2			GMODE_EXT_ LNA_PU_CORE1	RF_SW_CTRL_8	U
V	RGND		RGND	RGND			WRF_XTAL_ CAB_GND1P2			VSS	VSS	V
W	RGND	WRF_AFE_ VDD1P2_CORE1	RGND	RGND	WRF_RX5G_ VDD1P2_CORE1	RGND	WRF_XTAL_ CAB_GND1P2			WRF_TCXO_ VDD1P8	WRF_XTAL_ CAB_XON	W
Y										WRF_TCXO_ CKIN2V		Y
AA										WRF_XTAL_ CAB_GND1P2	WRF_XTAL_ CAB_XOP	AA
AB	RGND	RGND	RGND	RGND	RGND	RGND	RGND	RGND	WRF_XTAL_ CAB_GND1P2	WRF_XTAL_ CAB_GND1P2	WRF_XTAL_ CAB_GND1P2	AB
AC	WRF_PAOUT_ 2G_CORE1	WRF_PADRV2G_ VDD3P3_CORE1	WRF_PA_ VDD3P3_CORE1	WRF_PADRV5G_ VDD3P3_CORE1	WRF_PAOUT_ 5G_CORE1	RGND	WRF_RFIN_5G_ CORE1	RGND	WRF_XTAL_ CAB_GND1P2	WRF_XTAL_ CAB_VDD1P2	WRF_XTAL_ CAB_GND1P2	AC
	13	14	15	16	17	18	19	20	21	22	23	

Pin List—Ordered By Pin Number

Table 13 lists the pins in pin order.

Table 13: Pin List By Pin Number

Pin	Name
A1	VSS
A2	BT_UART_CTS_N
A4	BT_GPIO_4
A6	BT_USB_DN
A7	BT_USB_DP
A9	BT_PCM_OUT
A11	RF_SW_CTRL_6
A13	RF_SW_CTRL_3
A15	GPIO_7
A17	GPIO_8
A19	GPIO_6
A21	GPIO_3
A23	GPIO_0
AA1	WRF_PA_VDD3P3_CORE0
AA2	RGND
AA22	WRF_XTAL_CAB_GND1P2
AA23	WRF_XTAL_CAB_XOP
AB1	WRF_PADRV5G_VDD3P3_CORE0
AB2	RGND
AB3	RGND
AB4	RGND
AB5	RGND
AB6	WRF_TX_VDD1P2_CORE0
AB7	RGND
AB8	WRF_RX5G_VDD1P2_CORE0
AB9	RGND
AB10	WRF_TX_VDD1P2_CORE1
AB11	RGND
AB12	RGND
AB13	RGND
AB14	RGND
AB15	RGND
AB16	RGND
AB17	RGND
AB18	RGND
AB19	RGND
AB20	RGND
AB21	WRF_XTAL_CAB_GND1P2
AB22	WRF_XTAL_CAB_GND1P2
AB23	WRF_XTAL_CAB_GND1P2
AC1	RGND
AC2	WRF_PAOUT_5G_CORE0
AC3	RGND
AC4	WRF_RFIN_5G_CORE0
AC5	RGND
AC6	RGND
AC7	WRF_VCO_VDD1P2
AC9	WRF_SYNTH_VDD1P2
AC10	RGND
AC11	WRF_RFIN_2G_CORE1
AC12	RGND
AC13	WRF_PAOUT_2G_CORE1
AC14	WRF_PADRV2G_VDD3P3_CORE1
AC15	WRF_PA_VDD3P3_CORE1
AC16	WRF_PADRV5G_VDD3P3_CORE1
AC17	WRF_PAOUT_5G_CORE1
AC18	RGND
AC19	WRF_RFIN_5G_CORE1
AC20	RGND
AC21	WRF_XTAL_CAB_GND1P2
AC22	WRF_XTAL_CAB_VDD1P2
AC23	WRF_XTAL_CAB_GND1P2
B1	VSS
B2	VSS
B3	BT_UART_RTS_N
B4	BT_GPIO_5
B5	BT_I2S_WS
B6	BT_PCM_SYNC
B7	VSS
B8	BT_PCM_IN

Pin	Name
B9	BT_PCM_CLK
B11	RF_SW_CTRL_7
B12	RF_SW_CTRL_5
B13	RF_SW_CTRL_1
B14	RF_SW_CTRL_4
B15	RF_SW_CTRL_2
B16	RF_SW_CTRL_0
B17	GPIO_2
B18	JTAG_SEL
B19	GPIO_12
B20	GPIO_9
B21	GPIO_4
B22	GPIO_5
B23	GPIO_1
C1	BT_UART_RXD
C2	BT_UART_TXD
C22	SR_VLX
C23	SR_VLX
D2	BT_I2S_CLK
D22	SR_PVSS
D23	SR_PVSS
E1	BT_I2S_DI
E2	BT_I2S_DO
E5	BT_VDDC_ISO_1
E7	VSS
E8	VSS
E9	BT_GPIO_3
E10	BT_GPIO_2
E11	VSS
E12	GMODE_EXT_LNA_PU_CORE0
E13	AMODE_EXT_LNA_PU_CORE0
E15	EXT_XTAL_PU
E22	SR_PVSS
E23	SR_PVSS
F2	BT_CLK_REQ
F5	BT_VDDC_ISO_2
F19	PMU_AVSS
F22	SR_VDDBATP5V
F23	SR_VDDBATP5V
G1	BT_DEV_WAKE
G2	BT_HOST_WAKE
G5	BT_VDDO
G22	SR_VDDBATA5V
G23	SR_VDDBATA5V
H2	VSS
H5	BT_TM1
H22	VOUT_CLDO
H23	VOUT_CLDO
J1	BT_VCOVDD
J2	BT_PLLVDD
J8	BTRGND
J10	OTP_VDD33
J14	GPIO_11
J16	WL_REG_ON
J19	VOUT_LNLDO2
J22	VOUT_LNLDO1
J23	VOUT_LNLDO1
K1	BT_LNAVDD
K2	BTRGND
K5	BTVDD
K8	BTRGND
K10	BT_VDDC
K11	VDDIO_RF
K13	GPIO_10
K14	VSS
K16	VDDIO
K19	VSS
K22	LDO_VDD1P5
K23	LDO_VDD1P5
L2	BT_IFVDD
L5	BTRGND
L10	BT_VDDC
L11	VDD
L13	VDD
L14	VDD
L16	BT_REG_ON
L19	AVSS
L22	VSS
L23	VSS
M1	BT_RF

Pin	Name
M2	BTRGND
M5	BTRGND
M8	BTRGND
M9	BTRGND
M10	VSS
M14	VDD
M16	VSS
M19	MONPLL
M22	AVDD33
N2	V_BTBAT
N5	BTRGND
N9	BTRGND
N12	VDD
N14	VDD
N19	AVDD_BBPLL
N22	RREF
N23	DP
P1	BT_PAVDD
P2	BTRGND
P5	BTRGND
P8	BTRGND
P10	VSS
P12	VDD
P13	VDD
P14	VDD
P15	VSS
P16	VSS
P19	VDDIO_RF
P22	VSS
P23	DM
R1	WRF_RFIN_2G_CORE0
R2	RGND
R5	RGND
R7	RGND
R8	RGND
R9	RGND
R10	RGND
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R19	AMODE_EXT_LNA_PU_CORE1
R22	MONCDR
R23	DVSS
T1	RGND
T2	RGND
T5	RGND
T7	RGND
T8	RGND
T10	RGND
T11	RGND
T13	RGND
T14	RGND
T16	RGND
T17	WRF_XTAL_CAB_GND1P2
T19	VSS
T22	VSS
U1	WRF_PAOUT_2G_CORE0
U2	RGND
U5	WRF_RX2G_VDD1P2_CORE0
U8	RGND
U11	RGND
U13	RGND
U16	RGND
U19	WRF_XTAL_CAB_GND1P2
U22	GMODE_EXT_LNA_PU_CORE1
U23	RF_SW_CTRL_8
V1	RGND
V2	RGND
V5	RGND
V8	RGND
V9	RGND
V11	RGND
V13	RGND
V15	RGND
V16	RGND
V19	WRF_XTAL_CAB_GND1P2
V22	VSS
V23	VSS

Pin	*Name*
W1	WRF_PADRV2G_VDD3P3_CORE0
W2	RGND
W5	RGND
W6	RGND
W7	RGND
W8	WRF_GPIO_OUT
W9	RGND
W10	WRF_AFE_VDD1P2_CORE0
W11	RGND
W12	WRF_RX2G_VDD1P2_CORE1
W13	RGND
W14	WRF_AFE_VDD1P2_CORE1
W15	RGND
W16	RGND
W17	WRF_RX5G_VDD1P2_CORE1
W18	RGND
W19	WRF_XTAL_CAB_GND1P2
W22	WRF_TCXO_VDD1P8
W23	WRF_XTAL_CAB_XON
Y1	RGND
Y2	RGND
Y22	WRF_TCXO_CKIN2V

Pin List—Listed Alphabetically By Pin Name

Table 14 lists the pins alphabetically by name.

Table 14: Alphabetical Pin List By Pin Name

Name	Pin
AMODE_EXT_LNA_PU_CORE0	E13
AMODE_EXT_LNA_PU_CORE1	R19
AVDD_BBPLL	N19
AVDD33	M22
AVSS	L19
BT_CLK_REQ	F2
BT_DEV_WAKE	G1
BT_GPIO_2	E10
BT_GPIO_3	E9
BT_GPIO_4	A4
BT_GPIO_5	B4
BT_HOST_WAKE	G2
BT_I2S_CLK	D2
BT_I2S_DI	E1
BT_I2S_DO	E2
BT_I2S_WS	B5
BT_IFVDD	L2
BT_LNAVDD	K1
BT_PAVDD	P1
BT_PCM_CLK	B9
BT_PCM_IN	B8
BT_PCM_OUT	A9
BT_PCM_SYNC	B6
BT_PLLVDD	J2
BT_RF	M1
BT_TM1	H5
BT_UART_CTS_N	A2
BT_UART_RTS_N	B3
BT_UART_RXD	C1
BT_UART_TXD	C2
V_BTBAT	N2
BT_VCOVDD	J1
BT_VDDC	K10
BT_VDDC	L10
BT_VDDC_ISO_1	E5
BT_VDDC_ISO_2	F5
BT_VDDO	G5
BT_REG_ON	L16
BTRGND	J8
BTRGND	K2
BTRGND	K8
BTRGND	L5
BTRGND	M2
BTRGND	M5
BTRGND	M8
BTRGND	M9
BTRGND	N5
BTRGND	N9
BTRGND	P2
BTRGND	P5
BTRGND	P8
BTVDD	K5
DM	P23
DP	N23
DVSS	R23
EXT_XTAL_PU	E15
GMODE_EXT_LNA_PU_CORE0	E12
GMODE_EXT_LNA_PU_CORE1	U22
GPIO_0	A23
GPIO_1	B23
GPIO_10	K13
GPIO_11	J14
GPIO_12	B19
GPIO_2	B17
GPIO_3	A21
GPIO_4	B21
GPIO_5	B22
GPIO_6	A19
GPIO_7	A15
GPIO_8	A17

Name	Pin
GPIO_9	B20
BT_USB_DN	A6
BT_USB_DP	A7
JTAG_SEL	B18
LDO_VDD1P5	K22
LDO_VDD1P5	K23
MONCDR	R22
MONPLL	M19
OTP_VDD33	J10
PMU_AVSS	F19
RF_SW_CTRL_0	B16
RF_SW_CTRL_1	B13
RF_SW_CTRL_2	B15
RF_SW_CTRL_3	A13
RF_SW_CTRL_4	B14
RF_SW_CTRL_5	B12
RF_SW_CTRL_6	A11
RF_SW_CTRL_7	B11
RF_SW_CTRL_8	U23
RGND	R2
RGND	R5
RGND	R7
RGND	R8
RGND	R9
RGND	R10
RGND	T1
RGND	T2
RGND	T5
RGND	T7
RGND	T8
RGND	T10
RGND	T11
RGND	T13
RGND	T14
RGND	T16
RGND	U2
RGND	U8
RGND	U11
RGND	U13
RGND	U16

Name	Pin
RGND	V1
RGND	V2
RGND	V5
RGND	V8
RGND	V9
RGND	V11
RGND	V13
RGND	V15
RGND	V16
RGND	W2
RGND	W5
RGND	W6
RGND	W7
RGND	W9
RGND	W11
RGND	W13
RGND	W15
RGND	W16
RGND	W18
RGND	Y1
RGND	Y2
RGND	AA2
RGND	AB2
RGND	AB3
RGND	AB4
RGND	AB5
RGND	AB7
RGND	AB9
RGND	AB11
RGND	AB12
RGND	AB13
RGND	AB14
RGND	AB15
RGND	AB16
RGND	AB17
RGND	AB18
RGND	AB19
RGND	AB20
RGND	AC1
RGND	AC3

Name	Pin
RGND	AC5
RGND	AC6
RGND	AC10
RGND	AC12
RGND	AC18
RGND	AC20
RREF	N22
SR_PVSS	D22
SR_PVSS	D23
SR_PVSS	E22
SR_PVSS	E23
SR_VDDBATA5V	G22
SR_VDDBATA5V	G23
SR_VDDBATP5V	F22
SR_VDDBATP5V	F23
SR_VLX	C22
SR_VLX	C23
VDD	L11
VDD	L13
VDD	L14
VDD	M14
VDD	N12
VDD	N14
VDD	P12
VDD	P13
VDD	P14
VDDIO	K16
VDDIO_RF	K11
VDDIO_RF	P19
VOUT_CLDO	H22
VOUT_CLDO	H23
VOUT_LNLDO1	J22
VOUT_LNLDO1	J23
VOUT_LNLDO2	J19
VSS	A1
VSS	B1
VSS	B2
VSS	B7
VSS	E7
VSS	E8

Name	Pin
VSS	E11
VSS	H2
VSS	K14
VSS	K19
VSS	L22
VSS	L23
VSS	M10
VSS	M16
VSS	P10
VSS	P15
VSS	P16
VSS	P22
VSS	R11
VSS	R12
VSS	R13
VSS	R14
VSS	R15
VSS	T19
VSS	T22
VSS	V22
VSS	V23
WL_REG_ON	J16
WRF_AFE_VDD1P2_CORE0	W10
WRF_AFE_VDD1P2_CORE1	W14
WRF_GPIO_OUT	W8
WRF_PA_VDD3P3_CORE0	AA1
WRF_PA_VDD3P3_CORE1	AC15
WRF_PADRV2G_VDD3P3_CORE0	W1
WRF_PADRV2G_VDD3P3_CORE1	AC14
WRF_PADRV5G_VDD3P3_CORE0	AB1
WRF_PADRV5G_VDD3P3_CORE1	AC16
WRF_PAOUT_2G_CORE0	U1
WRF_PAOUT_2G_CORE1	AC13
WRF_PAOUT_5G_CORE0	AC2
WRF_PAOUT_5G_CORE1	AC17
WRF_RFIN_2G_CORE0	R1
WRF_RFIN_2G_CORE1	AC11
WRF_RFIN_5G_CORE0	AC4
WRF_RFIN_5G_CORE1	AC19
WRF_RX2G_VDD1P2_CORE0	U5

Name	*Pin*
WRF_RX2G_VDD1P2_CORE1	W12
WRF_RX5G_VDD1P2_CORE0	AB8
WRF_RX5G_VDD1P2_CORE1	W17
WRF_SYNTH_VDD1P2	AC9
WRF_TCXO_CKIN2V	Y22
WRF_TCXO_VDD1P8	W22
WRF_TX_VDD1P2_CORE0	AB6
WRF_TX_VDD1P2_CORE1	AB10
WRF_VCO_VDD1P2	AC7
WRF_XTAL_CAB_GND1P2	T17
WRF_XTAL_CAB_GND1P2	U19
WRF_XTAL_CAB_GND1P2	V19
WRF_XTAL_CAB_GND1P2	W19
WRF_XTAL_CAB_GND1P2	AA22
WRF_XTAL_CAB_GND1P2	AB21
WRF_XTAL_CAB_GND1P2	AB22
WRF_XTAL_CAB_GND1P2	AB23
WRF_XTAL_CAB_GND1P2	AC21
WRF_XTAL_CAB_GND1P2	AC23
WRF_XTAL_CAB_VDD1P2	AC22
WRF_XTAL_CAB_XON	W23
WRF_XTAL_CAB_XOP	AA23

Signal Descriptions

The signal name, type, and description of each pin in the BCM43242 is listed in Table 15. The Type indicates pin direction (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 15: FCFBGA Signal Descriptions

Signal Name	*FCFBGA Ball#*	*Type*	*Description*
WLAN Radio			
AVDD_BBPLL	N19	I	Baseband PLL supply
WRF_XTAL_CAB_XON	W23	O	XTAL output
WRF_XTAL_CAB_XOP	AA23	I	XTAL input
WRF_RFIN_2G_CORE1	AC11	I	2.4G RF input core 1
WRF_RFIN_5G_CORE1	AC19	I	5G RF input core 1
WRF_GPIO_OUT	W8	O	WLAN Radio GPIO
WRF_TCXO_CKIN2V	Y22	I	TCXO buffered input. When not using a TCXO this pin should be connected to ground.
WRF_SYNTH_VDD1P2	AC9	I	Clock and miscellaneous supplies
WRF_TCXO_VDD1P8	W22		
WRF_VCO_VDD1P2	AC7		
WRF_XTAL_CAB_VDD1P2	AC22		
WRF_XTAL_CAB_GND1P2	T17, U19, V19, W19, AA22, AB21, AB22, AB23, AC21, AC23	I	Clock and miscellaneous grounds
WRF_AFE_VDD1P2_CORE1	W14	I	WLAN core 1 radio supplies
WRF_PADRV2G_VDD3P3_CORE1	AC14		
WRF_PADRV5G_VDD3P3_CORE1	AC16		
WRF_TX_VDD1P2_CORE1	AB10		
WRF_RX2G_VDD1P2_CORE1	W12		
WRF_RX5G_VDD1P2_CORE1	W17		
WRF_RFIN_2G_CORE0	R1	I	2.4G RF input core 0
WRF_RFIN_5G_CORE0	AC4	I	5G RF input core 0
WRF_PAOUT_2G_CORE0	U1	O	2.4 GHz RF output for Core 0
WRF_PAOUT_2G_CORE1	AC13	O	2.4 GHz RF output for Core 1
WRF_PAOUT_5G_CORE0	AC2	O	5 GHz RF output for Core 0
WRF_PAOUT_5G_CORE1	AC17	O	5 GHz RF output for Core 1

Table 15: FCFBGA Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	Type	Description
WRF_AFE_VDD1P2_CORE0	W10	I	WLAN core 0 radio supplies
WRF_PADRV2G_VDD3P3_CORE0	W1		
WRF_PADRV5G_VDD3P3_CORE0	AB1		
WRF_TX_VDD1P2_CORE0	AB6		
WRF_RX2G_VDD1P2_CORE0	U5		
WRF_RX5G_VDD1P2_CORE0	AB8		
WRF_PA_VDD3P3_CORE1	AC15	I	WLAN PA Supplies (Core 1)
WRF_PA_VDD3P3_CORE0	AA1	I	WLAN PA Supplies (Core 0)
WLAN Digital			
RF_SW_CTRL_0	B16	O	WLAN RF switch control outputs
RF_SW_CTRL_1	B13		
RF_SW_CTRL_2	B15		
RF_SW_CTRL_3	A13		
RF_SW_CTRL_4	B14		
RF_SW_CTRL_5	B12		
RF_SW_CTRL_6	A11		
RF_SW_CTRL_7	B11		
RF_SW_CTRL_8	U23		
GMODE_EXT_LNA_PU_CORE0	E12	O	2.4G external LNA control core 0
AMODE_EXT_LNA_PU_CORE0	E13	O	5G external LNA control core 0
GMODE_EXT_LNA_PU_CORE1	U22	O	2.4G external LNA control core 1
AMODE_EXT_LNA_PU_CORE1	R19	O	5G external LNA control core 1
GPIO_11	J14	I/O	WLAN GPIO
GPIO_10	K13	I/O	WLAN GPIO
GPIO_9	B20	I/O	WLAN GPIO
GPIO_8	A17	I/O	WLAN GPIO
GPIO_7	A15	I/O	WLAN GPIO
GPIO_12	B19	I/O	This pin can be programmed to be a GPIO, the JTAG TRST_L signal, or the external coexistence ERCX_PRISEL signal.
GPIO_6	A19	I/O	WLAN GPIO
GPIO_5	B22	I/O	This pin can be programmed to be a GPIO, the JTAG TDO signal, or the external coexistence ERCX_TXCONF signal.
GPIO_4	B21	I/O	This pin can be programmed to be a GPIO, the JTAG TDI signal, or the external coexistence ERCX_RF_ACTIVE signal.
GPIO_3	A21	I/O	This pin can be programmed to be a GPIO, the JTAG TMS signal, or the external coexistence ERCX_FREQ signal.

Table 15: FCFBGA Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	Type	Description
GPIO_2	B17	I/O	This pin can be programmed to be a GPIO, the JTAG TCK signal, or the external coexistence ERCX_STATUS signal.
GPIO_1	B23	I/O	This pin can be programmed to be a GPIO or AP_READY.
GPIO_0	A23	I/O	This pin can be programmed to be a GPIO or a WLAN_HOST_WAKE output indicating that host wake-up should be performed.
JTAG_SEL	B18	I	JTAG select. The JTAG interface (multiplexed on the GPIO pins) is enabled when this pin is asserted high.
EXT_XTAL_PU	E15	O	External Xtal oscillator power-up signal
VDD	L11, L13, L14, M14, N12, N14, P12–P14	I	Digital always-on core supply
OTP_VDD33	J10	I	3.3V OTP power supply
VDDIO	K16	I	3.3V IO supply
VDDIO_RF	K11, P19	I	3.3V RF control IO supply
VSS	A1, B1, B2, B7, E7, E8, E11, H2, K14, K19, L22, L23, M10, M16, P10, P15, P16, P22, R11–R15, T19, T22, V22, V23	I	Core ground
RGND	R2, R5, R7–R10, T1, T2, T5, T7, T8, T10, T11, T13, T14, T16, U2, U8, U11, U13, U16, V1, V2, V5, V8, V9, V11, V13, V15, V16, W2, W5–7, W9, W11, W13, W15, W16, W18, Y1, Y2, AA2, AB2–AB5, AB7, AB9, AB11–AB20, AC1, AC3, AC5, AC6, AC10, AC12, AC18, AC20	I	WLAN Radio ground
WLAN USB			
DP	N23	–	Data+
DM	P23	–	Data–

Table 15: FCFBGA Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	Type	Description
MONCDR	R22	–	USB 2.0 debug
MONPLL	M19	–	USB 2.0 debug
RREF	N22	–	USB 2.0 reference resistor
AVDD33	M22	–	USB 2.0 3.3V supply
Bluetooth Radio			
BT_IFVDD	L2	I	1.2V Bluetooth IF block power supply
BT_LNAVDD	K1	I	1.2V Bluetooth LNA power supply
BT_PAVDD	P1	I	Bluetooth PA supply
BT_PLLVDD	J2	I	Bluetooth RF PLL power supply
BT_RF	M1	O	Bluetooth transceiver RF antenna port
VB_TBAT	N2	I	5.25V for Bluetooth
BT_VCOVDD	J1	I	Bluetooth VCO Supply
BTVDD	K5	I	Bluetooth 1.2V
AVSS	L19	I	Ground
BTRGND	J8, K2, K8, L5, M2, M5, M8, M9, N5, N9, P2, P5, P8	I	Bluetooth Vss
Bluetooth Digital			
BT_TM1	H5	I/O	BT test mode pin
BT_DEV_WAKE	G1	I/O	BT device wake
BT_HOST_WAKE	G2	I/O	BT host wake
BT_GPIO_2	E10	I/O	BT GPIO
BT_GPIO_3	E9	I/O	BT GPIO
BT_GPIO_4	A4	I/O	BT GPIO
BT_GPIO_5	B4	I/O	BT GPIO
BT_UART_CTS_N	A2	I/O	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface
BT_UART_RTS_N	B3	I/O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface
BT_UART_TXD	C2	I/O	UART serial output. Serial data output for the HCI UART interface
BT_UART_RXD	C1	I/O	UART serial input. Serial data input for the HCI UART interface
BT_I2S_CLK	D2	I/O	I^2S clock; can be master (output) or slave (input)
BT_I2S_DO	E2	I/O	I^2S data output
BT_I2S_DI	E1	I/O	I^2S data input
BT_I2S_WS	B5	I/O	I^2S WS: can be master (output) or slave (input)

Table 15: FCFBGA Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	Type	Description
BT_PCM_IN	B8	I/O	PCM data input or SLIMbus transport sensing
BT_PCM_CLK	B9	I/O	PCM or SLIMbus clock; can be master (output) or slave (input)
BT_PCM_SYNC	B6	I/O	PCM sync; can be master (output) or slave (input); or SLIMbus data
BT_PCM_OUT	A9	I/O	PCM data output
BT_CLK_REQ	F2	I/O	BT clock request
BT_VDDC	K10, L10	I	BT digital core 1.2V supply
BT_VDDC_ISO_1	E5	I	Core supply for power-on/off island VDDC_G
BT_VDDC_ISO_2	F5	I	Core supply for power-on/off island VDDB
BT_VDDO	G5	I	I/O supply for Bluetooth
Bluetooth USB			
BT_USB_DP	A7	I/O	USB D+
BT_USB_DN	A6	I/O	USB D–
DVSS	R23	I	Ground

Table 15: FCFBGA Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball#	Type	Description
PMU			
SR_PVSS	D22, D23, E22, E23	I	Switcher ground
SR_VDDBATA5V	G22, G23	I	Battery voltage input for band-gap and LDO3P3
SR_VDDBATP5V	F22, F23	I	Battery voltage input for the CBUCK switcher
SR_VLX	C22, C23	O	Switcher output (1.35V default)
LDO_VDD1P5	K22, K23	I	LDO input for CLDO, LNLDO1, and LNLDO2. Also voltage feedback input for CBUCK. (1.35V default)
BT_REG_ON	L16	I	Used by PMU to power up or power down the internal BCM43242 regulators used by Bluetooth circuits. Also, when deasserted, this pin holds Bluetooth circuits in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
WL_REG_ON	J16	I	Used by PMU to power up or power down the internal BCM43242 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
PMU_AVSS	F19	I	PMU ground
VOUT_LNLDO1	J22, J23	O	1.2V LNLDO1 output
VOUT_LNLDO2	J19	O	1.2V LNLDO2 output
VOUT_CLDO	H22, H23	O	1.2V Digital core LDO output

WLAN GPIO Signals and Strapping Options

The pins listed in Table 15 are sampled at power-on reset (POR) to determine various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 16: WLAN GPIO Functions and Strapping Options

Pin Name(s)	FCFBGA Pin	Function	Default	Description
GPIO_6, AMODE_EXT_LNA_PU_CORE0	A19 E13	strap_host_ifc_2 strap_host_ifc_1	00	The 2 strap pins strap_host_ifc_[2:1] together select the host interface to enable: 00: Normal USB 01: Bootloader-less USB
GPIO_7	A15	OTPEnabled	1	When this bit is 0, the OTP memory is not powered up by default.
GPIO_8	A17	SFlash Present	0	SFlash present strap
GPIO_9	B20	ARM Remap[0]	1	0: Boot from SRAM, ARM held in reset. 1: Boot from ROM by remapping the ARM core exception vectors, with the ARM held in reset.
GPIO_10	K13	SFlash type	0	Type of sflash used: 1 = Atmel®, 0 = ST®
GPIO_0, GPIO_1	A23 B23	ResourceInitMode[1:0]	10	00: PMU to power up to ILP clock available (no backplane clock). 01: Power up to ILP clock request. 10: ALP clock available. 11: HT clock available. This field may not be set to 11 for implementations using an oscillator running at other than 30 MHz because the PLL must be reprogrammed before it is enabled.
EXT_XTAL_PU	E15	strap_ext_xtal_pu_pol	0	This strap defines the output polarity of the ext_xtal_pu signal. 0 = Active high output polarity. 1 = Active low output polarity.

Multiplexed Bluetooth Digital I/O Signals

Table 17 shows the pad function to pin name mapping of the Bluetooth digital I/O signals.

Table 17: Multiplexed Bluetooth Digital I/O Signal Matrix

	Functional Programming Modes									
Pin Name	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**13**	**15**
BT_GPIO_5	GPIO[5]	–	–	I2S_MSCK	I2S_SSCK	–	WLAN CLK REQ	–	–	–
BT_GPIO_4	GPIO[4]	–	–	I2S_MSDO	I2S_SSDO	–	WLAN CLK REQ	–	–	–
BT_GPIO_3	GPIO[3]	–	–	I2S_MWS	I2S_SWS	–	–	–	–	–
BT_GPIO_2	GPIO[2]	–	–	–	I2S_MSDI	–	–	–	–	–
BT_PCM_IN	A_GPIO[3]	PCM_IN	–	–	–	–	–	I2S_MSDI	–	SPI_MISO
BT_PCM_OUT	A_GPIO[2]	PCM_OUT	–	–	–	I2S_MSDO	–	I2S_SSDO	–	SPI_MOSI
BT_PCM_SYNC	A_GPIO[1]	PCM_SYNC	–	–	–	I2S_MWS	–	I2S_SWS	–	SPI_CS
BT_PCM_CLK	A_GPIO[0]	PCM_CLK	–	–	–	I2S_MSCK	–	I2S_SSCK	–	SPI_CLK
BT_UART_RXD	UART_RXD	–	–	–	–	–	–	GPIO[5]	–	–
BT_UART_TXD	UART_TXD	–	–	–	–	–	–	GPIO[4]	–	–
BT_UART_RTS_N	UART_RTS_N	–	–	–	–	–	–	A_GPIO[0]	–	–
BT_UART_CTS_N	UART_CTS_N	–	–	–	–	–	–	A_GPIO[1]	–	–
BT_I2S_DI	A_GPIO[6]	PCM_IN	–	–	–	–	–	–	–	–
BT_I2S_DO	A_GPIO[5]	PCM_OUT	–	–	–	I2S_MSDO	–	SPI_INT	SPI_INT	–
BT_I2S_WS	GPIO[7]	PCM_SYNC	–	–	–	I2S_MWS	–	I2S_SWS	–	–
BT_I2S_CLK	GPIO[6]	PCM_CLK	–	–	–	I2S_MSCK	–	I2S_SSCK	–	–
BT_CLK_REQ	WLAN_CLK_REQ	–	–	–	–	–	–	A_GPIO[7]	–	–
BT_HOST_WAKE	GPIO[1]	–	–	–	–	–	–	–	–	–
BT_DEV_WAKE	GPIO[0]	–	–	–	–	–	–	–	–	–

The multiplexed digital I/O signals are described in Table 18.

Table 18: Multiplexed Digital I/O Signals

Pin Name	*Type*	*Function*
BT_GPIO_5	I/O	General purpose I/O.
BT_GPIO_4	I/O	General purpose I/O.
BT_GPIO_3	I/O	General purpose I/O.
BT_GPIO_2	I/O	General purpose I/O.
BT_PCM_IN	I	PCM audio serial data input.
BT_PCM_OUT	O	PCM audio serial data output.
BT_PCM_SYNC	I/O	PCM SYNC (master & slave modes).
BT_PCM_CLK	I/O	PCM CLK (master and slave modes).
BT_UART_RXD	I	Host UART receive data.
BT_UART_TXD	O	Host UART transmit data.
BT_UART_RTS_N	O	Host UART RTS.
BT_UART_CTS_N	I	Host UART CTS.
BT_I2S_DI	I	I^2S audio data serial input.
BT_I2S_DO	O	I^2S audio data serial output.
BT_I2S_WS	I/O	I^2S word strobe (master & slave modes).
BT_I2S_CLK	I/O	I^2S clock (master & slave modes).
BT_CLK_REQ	O	Reference clock request to host from BT or WLAN.
BT_HOST_WAKE	O	Signal to tell the host that the BCM43242 needs attention.
BT_DEV_WAKE	I	Signal to tell the BCM43242 that the host requires attention.

Note: See Table 17 for alternate I/O functions.

Section 14: DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 19 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 19: Absolute Maximum Ratings

Rating	*Symbol*	*Value*	*Unit*
DC supply voltage for I/O	VDDIO	–0.5 to 3.8	V
DC supply voltage for RF	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
DC supply voltage for RF I/Os and PA driver supply	VDDIO_RF	–0.5 to 3.8	V
DC supply voltage for battery-supplied pins	SR_VDDBATA5V (VBAT)	–0.5 to 5.25	V
DC input supply voltage for CLDO and LNLDO1	–	–0.5 to 2.1	V
WRF_TCXO_VDD	–	–0.5 to 1.98	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum Junction Temperature	T_j	125	°C

Environmental Ratings

The environmental ratings are shown in Table 20.

Table 20: Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	0 to +70	°C	Functional operation[a]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 21: ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1000	V
Machine Model (MM)	ESD_HAND_MM	Machine model contact	75	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	500	V

Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 22 and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 22: Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage	VDD33	3.0	3.3	3.6	V
	VDDIO	3.0	3.3	3.6	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for core CBUCK	VBAT	3.0	3.3	5.25	V
DC supply voltage for BT PA	BT_VBAT	3.0	3.3	5.25	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
Other Digital I/O Pins					
VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output Low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins					
For VDDIO_RF = 3.3V:					
Output High Voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output Low Voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

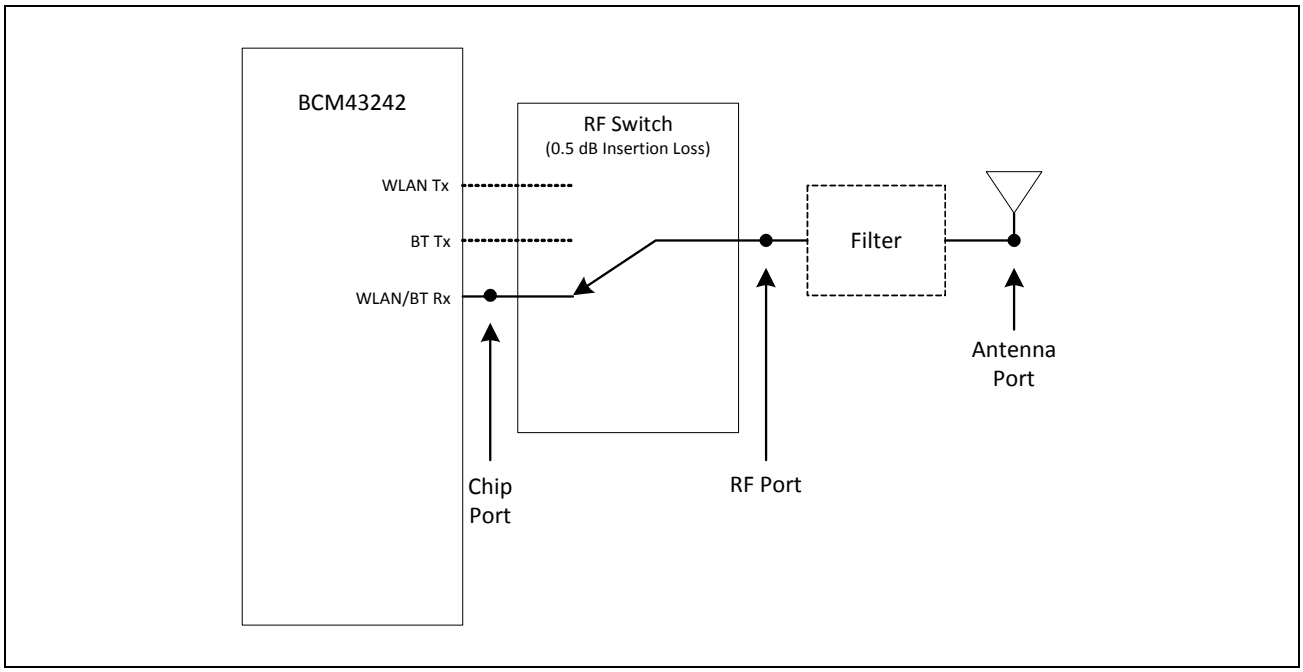
Section 15: Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 20: “Environmental Ratings,” on page 83 and Table 22: “Recommended Operating Conditions and DC Characteristics,” on page 84. Typical values apply for the following conditions:

- VDD33 = 3.3V ± 10%.
- Ambient temperature +25°C

Figure 26: RF Port Location for Bluetooth Testing



Note: All Bluetooth specifications are measured at the Chip port unless otherwise specified.

Table 23: Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4–DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8–DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
Interference Performance[a]					
C/I co-channel	GFSK, 0.1% BER	–	8.5	–	dB
C/I 1-MHz adjacent channel	GFSK, 0.1% BER	–	–5	–	dB
C/I 2-MHz adjacent channel	GFSK, 0.1% BER	–	–35	–	dB
C/I ≥ 3-MHz adjacent channel	GFSK, 0.1% BER	–	–49	–	dB
C/I image channel	GFSK, 0.1% BER	–	–31	–	dB
C/I 1-MHz adjacent to image channel	GFSK, 0.1% BER	–	–42	–	dB
C/I co-channel	π/4–DQPSK, 0.1% BER	–	10	–	dB
C/I 1-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–10	–	dB
C/I 2-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–35	–	dB
C/I ≥ 3-MHz adjacent channel	8–DPSK, 0.1% BER	–	–50	–	dB
C/I image channel	π/4–DQPSK, 0.1% BER	–	–28	–	dB
C/I 1-MHz adjacent to image channel	π/4–DQPSK, 0.1% BER	–	–45	–	dB
C/I co-channel	8–DPSK, 0.1% BER	–	17	–	dB
C/I 1 MHz adjacent channel	8–DPSK, 0.1% BER	–	–4	–	dB
C/I 2 MHz adjacent channel	8–DPSK, 0.1% BER	–	–33	–	dB
C/I ≥ 3-MHz adjacent channel	8–DPSK, 0.1% BER	–	–47	–	dB
C/I image channel	8–DPSK, 0.1% BER	–	–21	–	dB
C/I 1-MHz adjacent to image channel	8–DPSK, 0.1% BER	–	–39	–	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer					

Table 23: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
		GFSK (1 Mbps)[b]			
698–716 MHz	WCDMA	–	–8.5	–	dBm
776–794 MHz	WCDMA	–	–8.5	–	dBm
824–8249 MHz	GSM850	–	–10.9	–	dBm
824–8249 MHz	WCDMA	–	–10.5	–	dBm
880–915 MHz	E-GSM	–	–11.3	–	dBm
880–915 MHz	WCDMA	–	–10.9	–	dBm
1710–1785 MHz	GSM1800	–	–17.3	–	dBm
1710–1785 MHz	WCDMA	–	–16.4	–	dBm
1850–1910 MHz	GSM1900	–	–18.5	–	dBm
1850–1910 MHz	WCDMA	–	–17.8	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18.8	–	dBm
1920–1980 MHz	WCDMA	–	–18.1	–	dBm
2010–2025 MHz	TD–SCDMA	–	–19.3	–	dBm
2500–2570 MHz	WCDMA	–	–18.1	–	dBm
		π/4 DPSK (2 Mbps)[b]			
698–716 MHz	WCDMA	–	–5.9	–	dBm
776–794 MHz	WCDMA	–	–5.9	–	dBm
824–8249 MHz	GSM850	–	–8.4	–	dBm
824–8249 MHz	WCDMA	–	–8	–	dBm
880–915 MHz	E-GSM	–	–8.6	–	dBm
880–915 MHz	WCDMA	–	–8.6	–	dBm
1710–1785 MHz	GSM1800	–	–14.4	–	dBm
1710–1785 MHz	WCDMA	–	–14.3	–	dBm
1850–1910 MHz	GSM1900	–	–15.2	–	dBm
1850–1910 MHz	WCDMA	–	–14.6	–	dBm
1880–1920 MHz	TD-SCDMA	–	–16.3	–	dBm
1920–1980 MHz	WCDMA	–	–15.2	–	dBm
2010–2025 MHz	TD-SCDMA	–	–16.7	–	dBm
2500–2570 MHz	WCDMA	–	–16.7	–	dBm
		8DPSK (3 Mbps)[c]			
698-716 MHz	WCDMA	–	-7.5	–	dBm
776-794 MHz	WCDMA	–	-7.5	–	dBm
824-8249 MHz	GSM850	–	-10.0	–	dBm
824-8249 MHz	WCDMA	–	-9.7	–	dBm
880-915 MHz	E-GSM	–	-10.0	–	dBm
880-915 MHz	WCDMA	–	-9.7	–	dBm
1710-1785 MHz	GSM1800	–	-16.3	–	dBm

Table 23: Bluetooth Receiver RF Specifications (Cont.)

Parameter	*Conditions*	*Minimum*	*Typical*	*Maximum*	*Unit*
1710-1785 MHz	WCDMA	–	-15.6	–	dBm
1850-1910 MHz	GSM1900	–	-17.4	–	dBm
1850-1910 MHz	WCDMA	–	-16.9	–	dBm
1880-1920 MHz	TD-SCDMA	–	-18.1	–	dBm
1920-1980 MHz	WCDMA	–	-17.5	–	dBm
2010-2025 MHz	TD-SCDMA	–	-19.1	–	dBm
2500-2570 MHz	WCDMA	–	-18.5	–	dBm
Spurious Emissions					
30 MHz–1 GHz		–	–	–62	dBm
1–12.75 GHz		–	–	–47	dBm
851–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
b. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = –84.5 dBm.
c. Bluetooth reference level for the wanted signal at the Bluetooth chip port = –79.5 dBm.

Table 24: Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		11.0	13.0	–	dBm
QPSK TX Power at Bluetooth		8.0	10.0	–	dBm
8PSK TX Power at Bluetooth		8.0	10.0	–	dBm
Power control step		2	4	6	dB
Note: Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	–	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–	–20.0	dBm
|M – N| ≥ 2.5 MHz		–	–	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [a, b]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [b, c, d]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
RX LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–150	–127	dBm
776–794 MHz	CDMA2000	–	–140	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–140	–	dBm/Hz
925–960 MHz	E-GSM	–	–140	–	dBm/Hz
1570–1580 MHz	GPS	–	–140	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–140	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–140	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–140	–	dBm/Hz

Table 24: Bluetooth Transmitter RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Out-of-Band Noise Floor[e]					
776–794 MHz	CDMA2000	–	–140	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–140	–	dBm/Hz
925–960 MHz	E-GSM	–	–140	–	dBm/Hz
1570–1580 MHz	GPS	–	–140	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–140	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–140	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–140	–	dBm/Hz

a. The maximum value represents the value required for Bluetooth qualification as defined in the v4.0 specification.
b. The spurious emissions during Idle mode are the same as specified in Table 24 on page 89.
c. Specified at the Bluetooth Antenna port.
d. Meets this specification using a front-end band-pass filter.
e. Transmitted power in the cellular bands at the Bluetooth Antenna port. See Figure 26 on page 85 for location of the port.

Table 25: Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±10	±25	kHz
DH3 packet	–	±10	±40	kHz
DH5 packet	–	±10	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	–	175	kHz
10101010 sequence in payload[b]	115	–	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 26: BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402		2480	MHz
RX sense	GFSK, 0.1% BER, 1 Mbps	–	-95.0	–	dBm
TX power[a]	–	–	8.5	–	dBm
Mod Char: delta f1 average	–	225	–	275	kHz
Mod Char: delta f2 max[b]	–	99.9	–	–	%
Mod Char: ratio	–	0.8	–	–	%

a. BLE TX power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc.). The output is capped at 12 dBm out. The BLE TX power at the antenna port cannot exceed the 10 dBm specification limit.
b. At least 99.9% of all delta F2 maximum frequency values recorded over 10 packets must be greater than 185 kHz.

Section 16: WLAN RF Specifications

Introduction

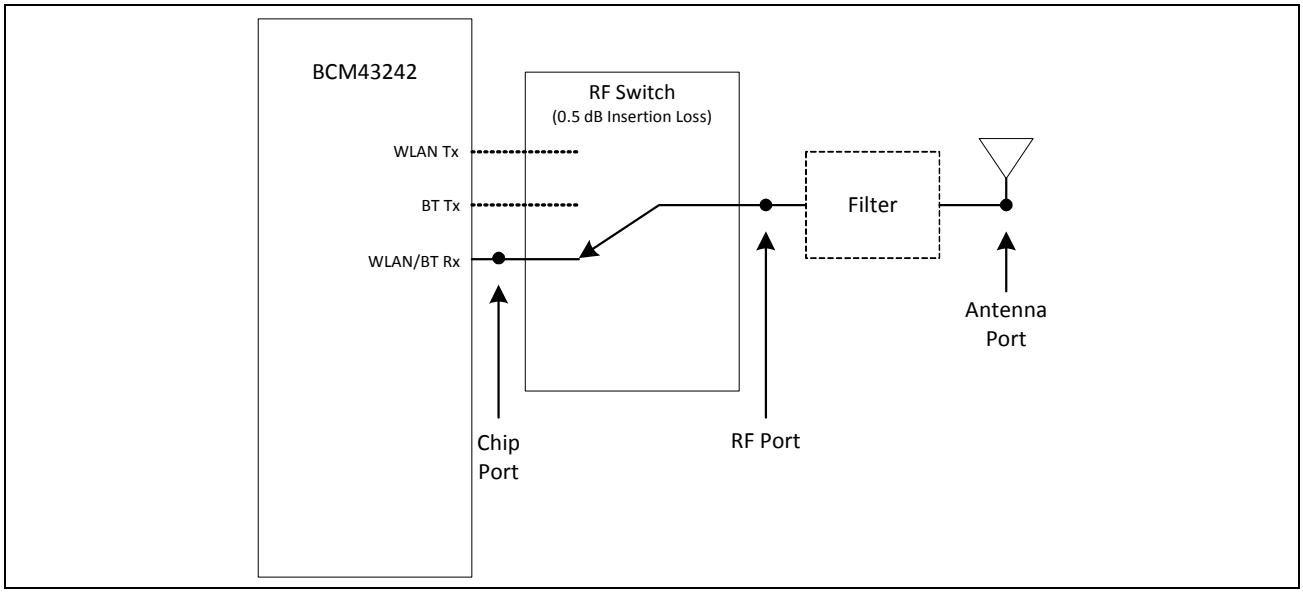
The BCM43242 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz band or the 5 GHz band. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 20: "Environmental Ratings," on page 83 and Table 22: "Recommended Operating Conditions and DC Characteristics," on page 84. Typical values apply for the following conditions:

- VDD33 = 3.3V ± 10% (VBAT tied to VDD33)
- Ambient temperature +25°C

Figure 27: Port Locations



Note: All WLAN specifications are measured at the chip port, unless otherwise specified.

2.4 GHz Band General RF Specifications

Table 27: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 28 are measured at the chip port, unless otherwise specified.

Table 28: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
SISO RX sensitivity (8% PER for 1024 octet PSDU)	1 Mbps DSSS	–	–99.0	–	dBm
	2 Mbps DSSS	–	–96.0	–	dBm
	5.5 Mbps DSSS	–	–94.2	–	dBm
	11 Mbps DSSS	–	–90.4	–	dBm
SISO RX sensitivity (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–94.0	–	dBm
	9 Mbps OFDM	–	–93.1	–	dBm
	12 Mbps OFDM	–	–91.7	–	dBm
	18 Mbps OFDM	–	–89.6	–	dBm
	24 Mbps OFDM	–	–85.6	–	dBm
	36 Mbps OFDM	–	–83	–	dBm
	48 Mbps OFDM	–	–77.7	–	dBm
	54 Mbps OFDM	–	–76.5	–	dBm
MIMO RX sensitivity (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–95.0	–	dBm/core
	9 Mbps OFDM	–	–94.2	–	dBm/core
	12 Mbps OFDM	–	–93.5	–	dBm/core
	18 Mbps OFDM	–	–92.6	–	dBm/core
	24 Mbps OFDM	–	–88.6	–	dBm/core
	36 Mbps OFDM	–	–86	–	dBm/core
	48 Mbps OFDM	–	–81.1	–	dBm/core
	54 Mbps OFDM	–	–80.1	–	dBm/core

Table 28: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
SISO RX sensitivity (10% PER for 4096 octet PSDU)[a]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS 7		–	–73.9	–	dBm
	MCS 6		–	–75.6	–	dBm
	MCS 5		–	–77	–	dBm
	MCS 4		–	–81.4	–	dBm
	MCS 3		–	–84.5	–	dBm
	MCS 2		–	–88.3	–	dBm
	MCS 1		–	–90.5	–	dBm
	MCS0		–	–92.5	–	dBm
MIMO RX sensitivity (10% PER for 4096 octet PSDU)[a]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS 15		–	–70.4	–	dBm (total)
	MCS 8		–	–90.1	–	dBm (total)
	MCS 7		–	–76.9	–	dBm/core
	MCS 6		–	–78.6	–	dBm/core
	MCS 5		–	–80	–	dBm/core
	MCS 4		–	–84.4	–	dBm/core
	MCS 3		–	–87.5	–	dBm/core
	MCS 2		–	–91.1	–	dBm/core
	MCS 1		–	–93.2	–	dBm/core
	MCS0		–	–94.0	–	dBm/core
Blocking level for 1 dB RX Sensitivity degradation (without external filtering)[b]	776–794 MHz	CDMA2000	–20	–	–	dBm
	824–849 MHz[c]	cdmaOne	–24.5	–	–	dBm
	824–849 MHz	GSM850	–20	–	–	dBm
	880–915 MHz	E-GSM	–18	–	–	dBm
	1710–1785 MHz	GSM1800	–20	–	–	dBm
	1850–1910 MHz	GSM1800	–22	–	–	dBm
	1850–1910 MHz	cdmaOne	–32	–	–	dBm
	1850–1910 MHz	WCDMA	–29	–	–	dBm
	1920–1980 MHz	WCDMA	–32	–	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Input In-Band IP3	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–19.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–19.5	–	–	dBm

Table 28: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
LPF 3 dB Bandwidth	–		9	–	10	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
Maximum receiver gain	–	–	–	105	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[d]	Range –95 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		6	10	–	dB
Receiver cascaded noise figure	At maximum gain		–	3.5	–	dB

a. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
d. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 29 are measured at the chip port output, unless otherwise specified.

Table 29: WLAN 2.4 GHz Transmitter Performance Specifications[a]

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Harmonic level (at –5 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–	TBD	dBm/ 1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–	TBD	dBm/ 1 MHz
OFDM EVM	OFDM, 64 QAM	0 dBm	–	–31	–	dB
OFDM EVM	OFDM, 64 QAM	–3 dBm	–	–33.9	–	dB
OFDM EVM	MCS7	–6 dBm	–	–35	–	dB
TX power at chip port for highest power level setting at 25°C, VDD33 = 3.3V, spectral mask and EVM compliance[b]	IEEE 802.11b: 1 Mbps		–	19.0	–	dBm
	IEEE 802.11g: 6 Mbps		–	19.5	–	dBm
	IEEE 802.11g: 54 Mbps @ 25 dB EVM, SISO + CDD		–	18.5	–	dBm
	MCS7: HT20 @ 28 dB EVM, SISO + CDD		–	17.0	–	dBm
	MCS7: HT40 @ 28 dB EVM, SISO + CDD		–	17.0	–	dBm
Phase noise	37.4 MHz crystal, integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at chip port TX	Z_o = 50Ω		4	6	–	dB

a. All power targets are measured at the chip output and were measured using revision 6 reference boards.
b. Derate by 1 dB for PA_Vdd supply (direct supply to PA) of 3V.

WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 30 are measured at the chip port input, unless otherwise specified.

Table 30: WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	4900	–	5845	MHz
SISO RX sensitivity (10% PER for 1000 octet PSDU)	6 Mbps OFDM	–	–92.4	–	dBm
	9 Mbps OFDM	–	–91.1	–	dBm
	12 Mbps OFDM	–	–89.7	–	dBm
	18 Mbps OFDM	–	–87.6	–	dBm
	24 Mbps OFDM	–	–83.6	–	dBm
	36 Mbps OFDM	–	–81	–	dBm
	48 Mbps OFDM	–	–76.2	–	dBm
	54 Mbps OFDM	–	–75.1	–	dBm
MIMO RX sensitivity (10% PER for 1000 octet PSDU)	6 Mbps OFDM	–	–93.5	–	dBm/core
	9 Mbps OFDM	–	–88.3	–	dBm/core
	12 Mbps OFDM	–	–86.7	–	dBm/core
	18 Mbps OFDM	–	–84.5	–	dBm/core
	24 Mbps OFDM	–	–80.8	–	dBm/core
	36 Mbps OFDM	–	–78	–	dBm/core
	48 Mbps OFDM	–	–73.4	–	dBm/core
	54 Mbps OFDM	–	–78.0	–	dBm/core
SISO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 7	–	–71.9	–	dBm
	MCS 6	–	–73.6	–	dBm
	MCS 5	–	–75	–	dBm
	MCS 4	–	–79.4	–	dBm
	MCS 3	–	–82.5	–	dBm
	MCS 2	–	–86.3	–	dBm
	MCS 1	–	–88.5	–	dBm
	MCS 0	–	–90.5	–	dBm

Table 30: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
MIMO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 15	–	–69.0	–	dBm (total)
	MCS 8	–	–89.0	–	dBm (total)
	MCS 7	–	–74.9	–	dBm/core
	MCS 6	–	–76.6	–	dBm/core
	MCS 5	–	–78	–	dBm/core
	MCS 4	–	–82.4	–	dBm/core
	MCS 3	–	–85.5	–	dBm/core
	MCS 2	–	–89.3	–	dBm/core
	MCS 1	–	–91.2	–	dBm/core
	MCS 0	–	–92.5	–	dBm/core
SISO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS 7	–	–69.4	–	dBm
	MCS 6	–	–71.1	–	dBm
	MCS 5	–	–72.5	–	dBm
	MCS 4	–	–77	–	dBm
	MCS 3	–	–80	–	dBm
	MCS 2	–	–83.8	–	dBm
	MCS 1	–	–86	–	dBm
	MCS 0	–	–88.1	–	dBm
MIMO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS 15	–	–67.0	–	dBm (total)
	MCS 8	–	–86.5	–	dBm (total)
	MCS 7	–	–71.9	–	dBm/core
	MCS 6	–	–73.7	–	dBm/core
	MCS 5	–	–75.1	–	dBm/core
	MCS 4	–	–79.6	–	dBm/core
	MCS 3	–	–82.7	–	dBm/core
	MCS 2	–	–86.5	–	dBm/core
	MCS 1	–	–88.6	–	dBm/core
	MCS 0	–	–90.4	–	dBm/core
Input In-Band IP3	Maximum LNA gain	–	–15.5	–	dBm
	Minimum LNA gain	–	–1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps	–29.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps	–29.5	–	–	dBm
LPF 3 dB bandwidth	–	9	–	18	MHz

Table 30: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[a] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	100	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[b]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω		6	10	–	dB
Receiver cascaded noise figure	At maximum gain		–	5.0	–	dB

a. For 65 Mbps, the size is 4096.
b. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 31 are measured at the chip port, unless otherwise specified.

Table 31: WLAN 5 GHz Transmitter Performance Specifications[a]

Parameter	Condition/Notes		Min.	Typical	Max.	Unit
Frequency range	–		4900	–	5845	MHz
Harmonic level (at –5 dBm)	9.8–11.570 GHz	2nd harmonic	–	TBD	–	dBm/ MHz
OFDM EVM	OFDM, 64 QAM	0 dBm	–	–30.4	–	dB
OFDM EVM	OFDM, 64 QAM	–3 dBm	–	–32.7	–	dB
OFDM EVM	MCS7	–6 dBm	–	–33.6	–	dB
TX power at chip port for highest power level setting at 25°C, VDD33 = 3.3V, spectral mask and EVM compliance[b]	IEEE 802.11a 6 Mbps, SISO+CDD, low subband,		–	20.0	–	dBm
	IEEE 802.11a 6 Mbps, SISO+CDD, mid subband,		–	19.5	–	dBm
	IEEE 802.11a 6 Mbps, SISO+CDD, high subband,		–	19.0	–	dBm
	IEEE 802.11a 54 Mbps @ 25 dB EVM, SISO+CDD, low subband		–	17.5	–	dBm
	IEEE 802.11a 54 Mbps @ 25 dB EVM, SISO+CDD, mid subband		–	16.5	–	dBm
	IEEE 802.11a 54 Mbps @ 25 dB EVM, SISO+CDD, high subband		–	16.5	–	dBm
	MCS7 HT20 @ 28 dB EVM, SISO+CDD, low subband		–	16.5	–	dBm
	MCS7 HT20 @ 28 dB EVM, SISO+CDD, mid subband		–	15.5	–	dBm
	MCS7 HT20 @ 28 dB EVM, SISO+CDD, high subband		–	15.5	–	dBm
	MCS7 HT40 @ 28 dB EVM, SISO+CDD, low subband		–	16.5	–	dBm
	MCS7 HT40 @ 28 dB EVM, SISO+CDD, mid subband		–	15.5	–	dBm
	MCS7 HT40 @ 28 dB EVM, SISO+CDD, high subband		–	15.5	–	dBm
Phase noise	37.4 MHz crystal, Integrated from 10 kHz to 10 MHz		–	0.7	–	Degrees
TX power control dynamic range	–		20	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Z_o = 50Ω		–	6	–	dB

a. All power targets are measured at the chip output and were measured using revision 6 reference boards.
b. Derate by 1.2 dB for PA_Vdd supply (direct supply to PA) of 3V.

General Spurious Emissions Specifications

Table 32: General Spurious Emissions Specifications

Parameter	*Condition/Notes*		*Min*	*Typ*	*Max*	*Unit*
Frequency range	–		TBD	TBD	TBD	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	TBD	TBD	TBD	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	TBD	TBD	TBD	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm

Section 17: Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside of the specification limits provided in this section.

Core Buck Switching Regulator

Table 33: Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage	DC voltage range inclusive of disturbances (VBAT).	3.0	3.3	5.25	V
PWM mode switching frequency	Forced PWM without FLL enabled	2.8	4	5.2	MHz
	Forced PWM with FLL enabled	3.6	4	4.4	MHz
PWM output current	–	–	–	600	mA
Output current limit	Peak inductor current	1100	1400	–	mA
Output voltage range	Programmable, 30 mV steps Default = 1.35V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max ripple based on VBAT = 3.3V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap+Board total-ESR < 20 mohms, Cout > 1.9 µF, ESL < 200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load Vout = 1.35V, VBAT = 3.3V at 25°C, Fsw = 4 MHz 2.2 µH inductor 0806 with DCR = 0.11 Ohm +/-25% and ACR <1 Ohm at 4 MHz	78	84	–	%
PFM mode efficiency	10 mA load current Vout = 1.35V, VBAT = 3.3V at 25°C, Cap+Board total-ESR < 20 mohms, Cout = 4.7 µF, ESL < 200 pH FLL = OFF 0603-size, L = 2.2 µH, DCR = 240 mohm +/-25%, ACR < 2 Ohm	67	77	–	%

Table 33: Core Buck Switching Regulator (CBUCK) Specifications (Cont.)

Specification	*Notes*	*Min*	*Typ*	*Max*	*Units*
LPOM efficiency	1 mA load current, Vout = 1.35V, VBAT = 3.3V at 25°C, Cap+Board total-ESR < 20 mohms, Cout = 4.7 µF, ESL < 200 pH FLL = OFF L = 2.2 µH, DCR = 240 mohms +/-25%, ACR < 2 Ohm	55	65	–	%
Start-up time from power down	VDDIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	674	850	µs
External inductor	0806 with DCR = 0.11 Ohm ± 25% and ACR <1 Ohm	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30mΩ at 4 MHz, ± 20%, 6.3V	2[a]	4.7	–	µF
External input capacitor	For SR_VDDBATP5V pin, Ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V, 4.7 µF	0.67[a]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

CLDO

Table 34: CLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, V_{in}	Min V_{in} = V_o + 0.15V = 1.35V (for Vo = 1.2V) dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Output current	–	0.2	–	300	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent Current	No load	–	20		µA
	Max load	–	2100	–	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA; V_{in} ≥ (V_o + 0.15V)	–	0.025	0.045	mV/mA
PSRR	@1 kHz, Vin ≥ V_o + 0.15V, C_o = 4.7 µF	20	–		dB
Start-up time of PMU	VDDIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 99% of V_o	–	550	850	µs
LDO turn-on time	LDO turn-on time when rest of the chip is up	–	–	180	µs
External output capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.32[a]	4.7	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO2

Table 35: LNLDO2 Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, Vin	Min Vin = V_o + 0.15V = 1.35V (for V_o = 1.2V) dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Output current	–	–	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	includes Line/Load regulation	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
	Max load	–	970	990	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, max load	–	–	5.5	mV/V
Load regulation	Load from 1 mA to 150 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Output noise	@30 kHz, 60-150 mA load C_o = 2.2 µF @100 kHz, 60-150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[a]	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO1

Table 36: LNLDO1 Specifications

Specification	*Notes*	*Min*	*Typ*	*Max*	*Units*
Input supply voltage , Vin	Min V_{in} = V_o +0.15V = 1.35V (for V_o = 1.2V) dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Output current	–	0.2	–	325	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	includes Line/Load regulation	–4	–	+4	%
Quiescent current	No load	–	88	–	µA
	Max load	–	2100	–	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, 300 mA load	–	–	+5	mV/V
Load regulation	Load from 1 mA to 300 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Output noise	@30 kHz, 60-325 mA load C_o = 4.7 µF @100 kHz, 60-325 mA load C_o = 4.7 µF	–	–	60 30	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 4.7 µF, V_o = 1.2V	20	–	–	dB
Start-up time of PMU	VDDIO up and steady. Time from REG_ON rise edge to LNLDO1 reaching 99% of V_o	–	550	850	µs
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	1.32[a]	4.7	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

Section 18: System Power Consumption

Note:

- Values in this data sheet are design goals and are subject to change based on the results of device characterization.
- Unless otherwise stated, these values apply for the conditions specified in Table 22: “Recommended Operating Conditions and DC Characteristics,” on page 84.

WLAN Current Consumption

WLAN current consumption measurements are shown in Table 37 and Table 38 on page 108.

Table 37: 2.4 GHz WLAN Current Consumption

Parameter	*VDD33 = 3.3V*	*VDDIO = 3.3V*	*Unit*
Current PM1 DTIM1	20	23.6	mA
Current PM1 DTIM3	17.8	23.6	mA
Off current	0.13	0.02	mA
Sleep (interbeacon sleep)	16.2	23.6	mA
Listen Current	100	23.7	mA
Continuous RX Mode @ 54 Mbps	102	23.7	mA
Continuous RX Mode @ MCS7 HT20	102	23.8	mA
Continuous RX Mode @ MCS8 HT20	103	23.8	mA
Continuous RX Mode @ MCS15 HT20	109	23.8	mA
802.11b 1 Mbps @ 19.0 dBm	354	23.7	mA
802.11g 6 Mbps @ 22.5 dBm	464	23.7	mA
802.11g 54 Mbps, SISO, EVM = –25 dBc @ 18.5 dBm	348	23.7	mA
802.11g 54 Mbps, CDD, EVM = –25 dBc @ 18.5 dBm	677	23.7	mA
MCS7 HT20, SISO, EVM = –28 dBc @ +17.0 dBm	325	23.7	mA
MCS7 HT20, CDD, EVM = –28 dBc @ +17.0 dBm	615	23.7	mA
MCS7 HT40, SISO, EVM = –28 dBc @ +17.0 dBm	362	23.7	mA
MCS7 HT40, CDD, EVM = –28 dBc @ +17.0 dBm	670	23.7	mA
MCS15 HT20, EVM = –28 dBc @ +17.0 dBm/core	625	23.7	mA
MCS15 HT40, EVM = –28 dBc @ +17.0 dBm/core	674	23.7	mA

Table 38: 5 GHz WLAN Current Consumption

Parameter	*VDD33 = 3.3V*	*VDDIO = 3.3V*	*Unit*
Current PM1 DTIM1	20.1	23.6	mA
Current PM1 DTIM1	17.4	23.6	mA
Off current	0.13	0.02	mA
Sleep (interbeacon sleep)	16.1	23.6	mA
Continuous RX mode 6 Mbps	110	23.8	mA
Continuous RX mode 54 Mbps	109	23.8	mA
Continuous RX mode MCS7 HT20	110	23.8	mA
Continuous RX mode MCS7 HT40	152	23.8	mA
Continuous RX mode MCS8 HT20	123	23.8	mA
Continuous RX mode MCS8 HT40	154	23.8	mA
Continuous RX mode MCS15 HT20	116	23.8	mA
Continuous RX mode MCS15 HT40	171	23.8	mA
802.11a 6 Mbps, SISO @ +19.5 dBm	367	23.8	mA
802.11a 6 Mbps, CDD, @ +19.5 dBm	710	23.8	mA
802.11a 54 Mbps, SISO @ +16.5 dBm	326	23.8	mA
802.11a 54 Mbps, CDD @ +16.5 dBm	610	23.8	mA
MCS7 HT20 @ –28 dBc EVM, SISO @ +15.5 dBm	312	23.8	mA
MCS7 HT20 @ –28 dBc EVM, CDD,@ +15.5 dBm	580	23.8	mA
MCS7 HT40 @ –28 dBc EVM, SISO @ +15.5 dBm	346	23.8	mA
MCS7 HT40 @ –28 dBc EVM, CDD @ +15.5 dBm	632	23.8	mA
MCS15 HT20, –28 dBc EVM @ +15.5 dBm/core	585	23.8	mA
MCS15 HT40, –28 dBc EVM @ +15.5 dBm/core	630	23.8	mA

Bluetooth Current Consumption

The Bluetooth current consumption measurements are shown in Table 39.

Note:

- The WLAN core is in reset (WL_REG_ON = low) for all measurements provided in Table 39.
- The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm.

Table 39: BT Power Consumption (Referenced at 3.3V VDD33)

Operating Mode	*Typical*	*Units*
Radio off	40	µA
Sleep mode	40	µA
Continuous RX power	15	mA
Sniff mode with page and inquiry scan	450	µA
SCO HV3 Master	7	mA
DM1/DH1	19	mA
DM3/DH3	23	mA
DM5/DH5	25	mA

Section 19: Interface Timing and AC Characteristics

JTAG Timing

Table 40: JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

Section 20: Power-Up Sequence and Timing

Sequencing of Reset and Regulator Control Signals

The BCM43242 has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 28, Figure 29 on page 112, and Figure 30 and Figure 31 on page 113). The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- The WL_REG_ON and BT_REG_ON signals are ORed in the BCM43242. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the BCM43242 regulators.
- The BCM43242 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the 0.6V threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

Description of Control Signals

- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM43242 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal BCM43242 regulators. When this pin is high, the regulators are enabled and the BT section is out of reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Control Signal Timing Diagrams

Figure 28: WLAN = ON, Bluetooth = ON

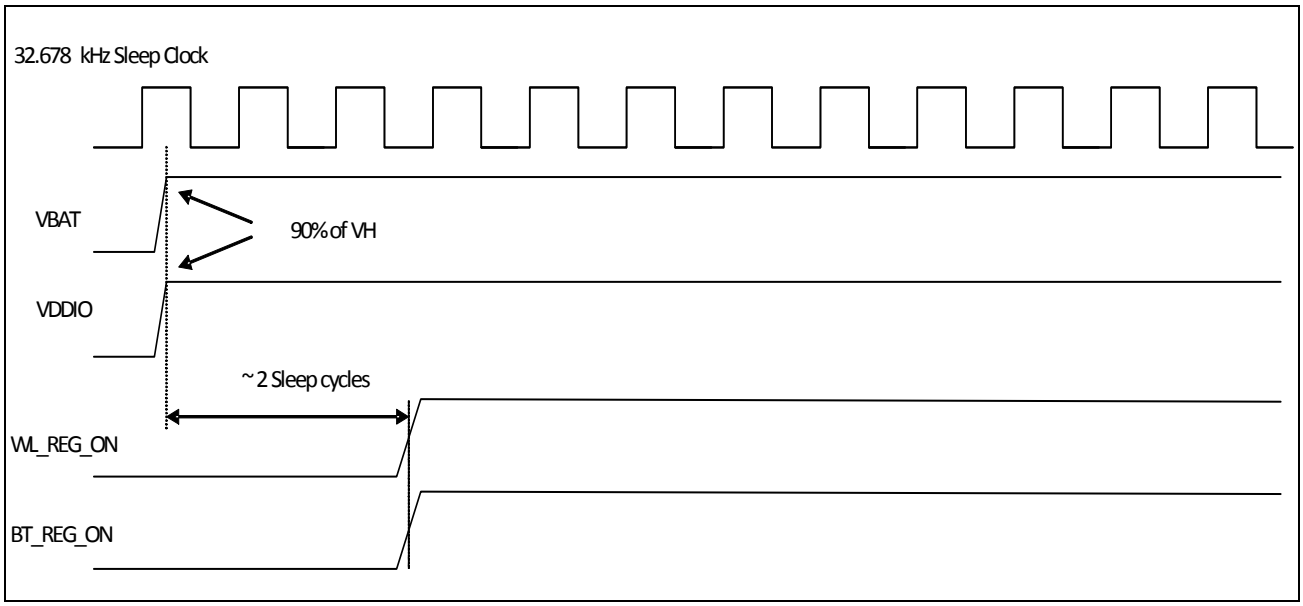


Figure 29: WLAN = OFF, Bluetooth = OFF

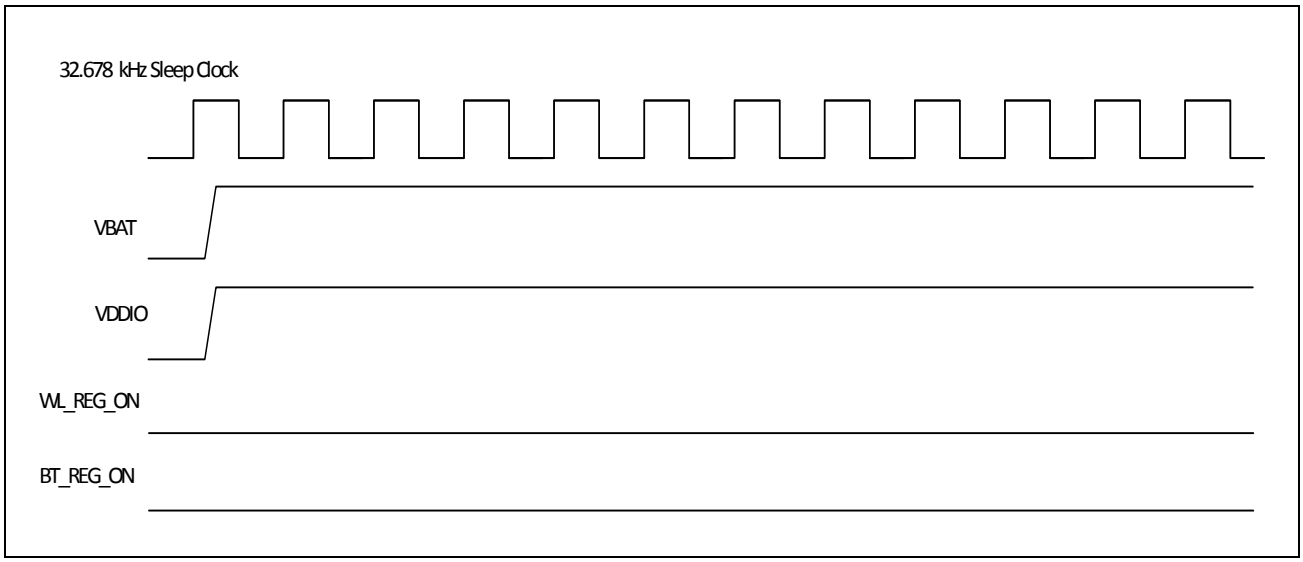


Figure 30: WLAN = ON, Bluetooth = OFF

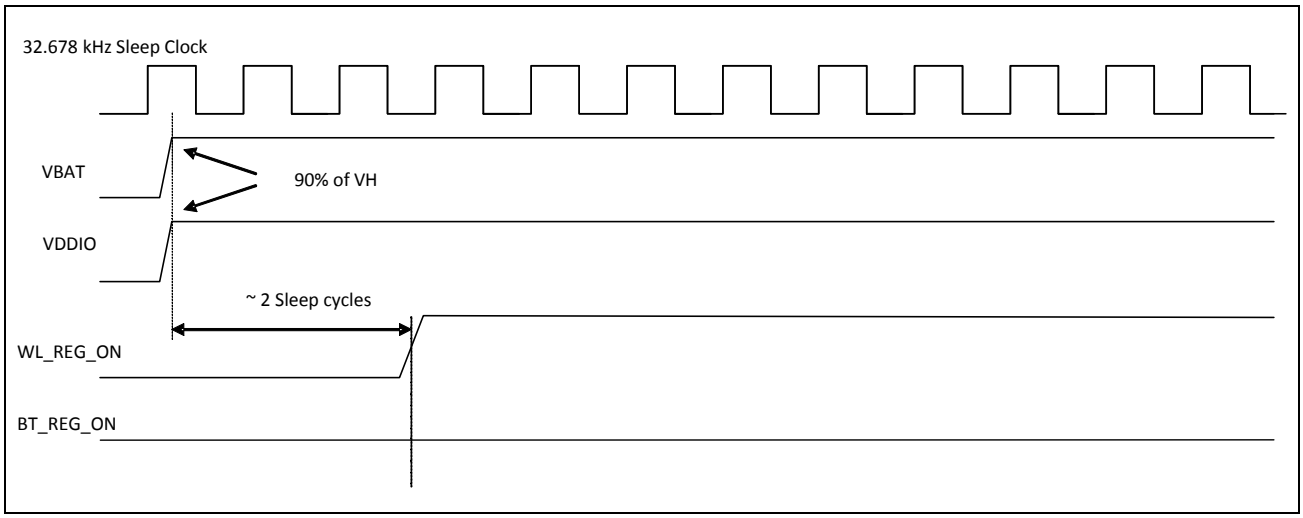
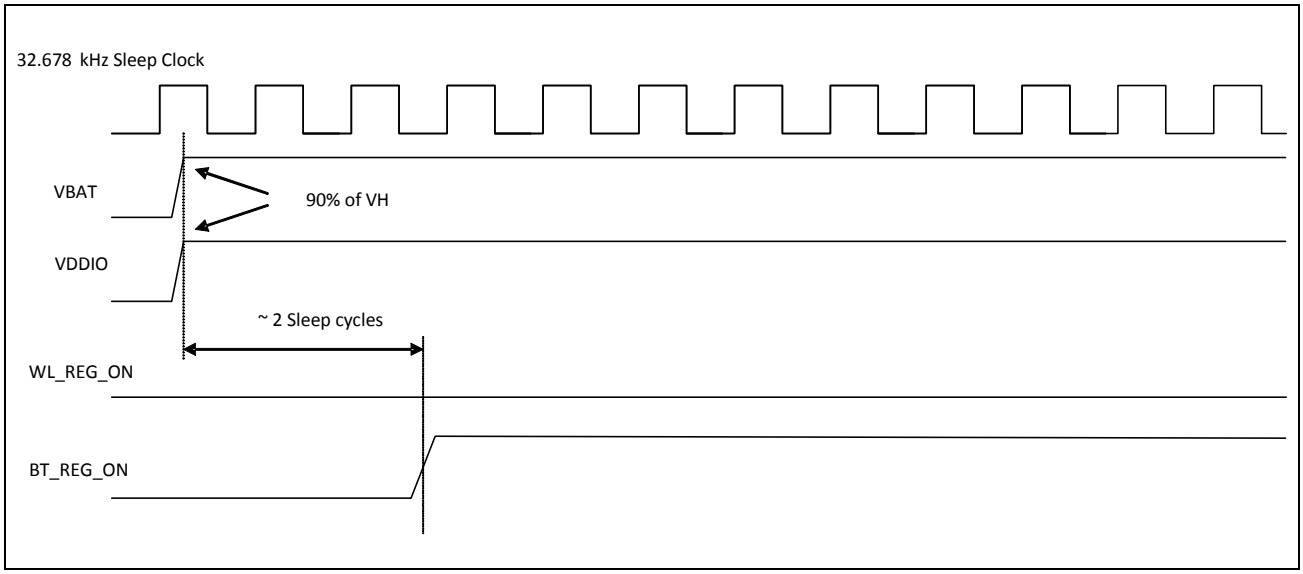


Figure 31: WLAN = OFF, Bluetooth = ON



Section 21: Package Information

Package Thermal Characteristics

Table 41: Package JEDEC Thermal Characteristics

Characteristic	*FCFBGA*
θ_{JA} (°C/W) (value in still air)	33.65
θ_{JB} (°C/W)	11.38
θ_{JC} (°C/W)	15.52
Ψ_{JT} (°C/W)	8.82
Ψ_{JB} (°C/W)	13.93
Maximum junction temperature T_j[a] (°C)	125
Maximum power dissipation (W)	2.1

a. Absolute junction temperature limits are maintained through active thermal monitoring and dynamic TX duty cycle limiting.

Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

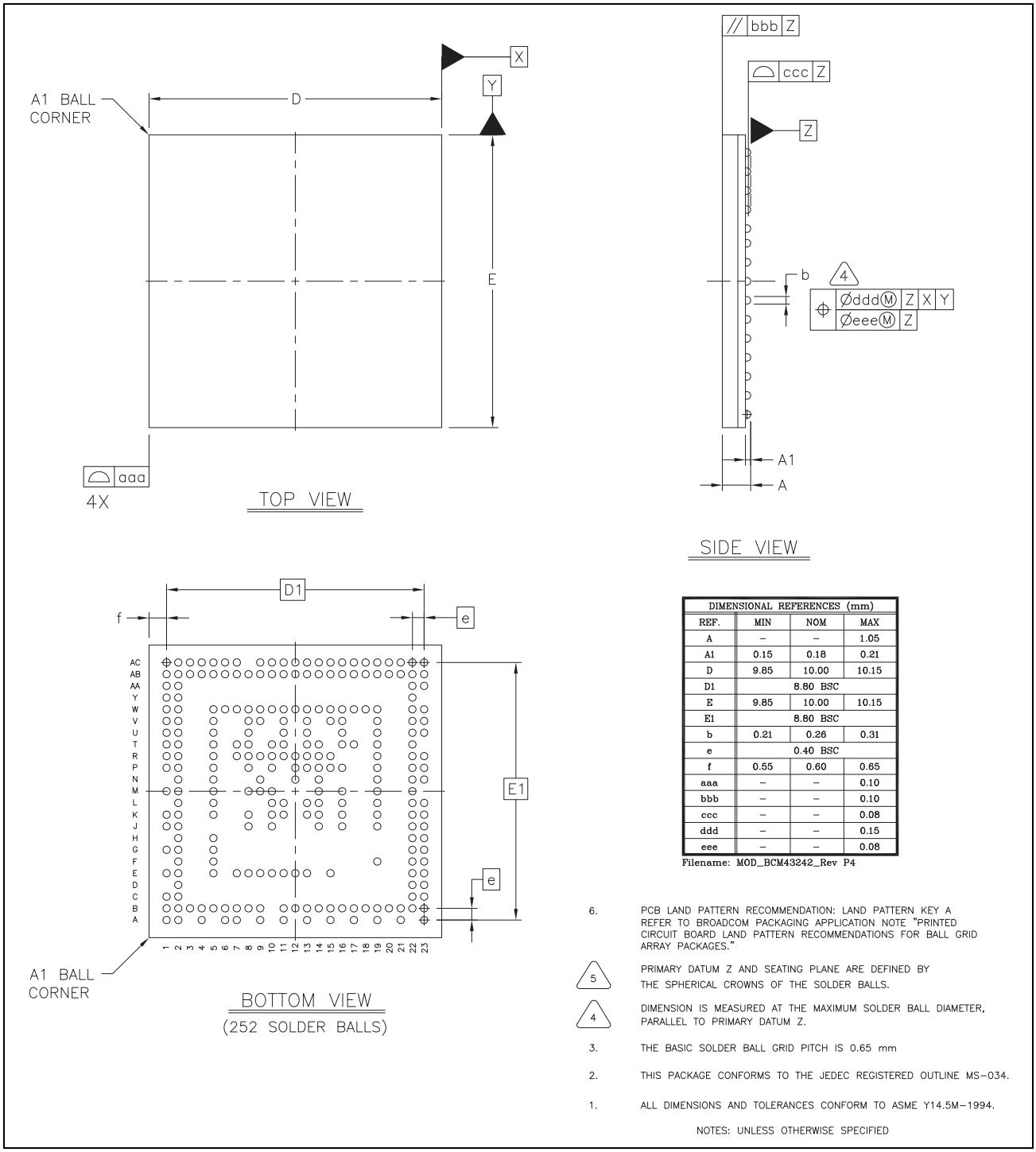
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

Environmental Characteristics

For environmental characteristics data, see Table 20: “Environmental Ratings,” on page 83.

Section 22: Mechanical Information

Figure 32: FCFBGA Package Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.05
A1	0.15	0.18	0.21
D	9.85	10.00	10.15
D1		8.80 BSC	
E	9.85	10.00	10.15
E1		8.80 BSC	
b	0.21	0.26	0.31
e		0.40 BSC	
f	0.55	0.60	0.65
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD_BCM43242_Rev P4

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.65 mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MS-034.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 23: Ordering Information

Part Number	*Package*	*Operating Ambient Temperature*
BCM43242KFFBG	FCFBGA (10.00 mm x 10.00 mm, 0.4 mm pitch)	–10°C to +70°C[a]

a. Absolute junction temperature limits are maintained through active thermal monitoring and dynamic TX duty cycle limiting.

Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

Phone: 949-926-5000
Fax: 949-926-5203
E-mail: info@broadcom.com
Web: www.broadcom.com

43242-DS103-R May 18, 2015