LX2273

Four Channel High Brightness LED Driver

PRODUCT DATASHEET

DESCRIPTION

The LX2273 is a high brightness multi-channel Boost LED driver designed for Solid State Lighting applications. It offers the designer a high degree of flexibility to accommodate different LED configurations (white or RGB), drive currents and output voltages while providing a high degree of control, protection and fault management of the system.

The LX2273 driver supports up to four independent LED strings and can be integrated in a system that supports up to 60V per channel. The drive current of each string can be programmed up to 500mA, with a typical channel-to-channel matching accuracy within +/- 1.5 percent. The FETs of the boost converter and each LED current sink are external to provide the flexibility and scalability to accommodate a variety of LED configurations as well as to provide optimal thermal management of the system.

The device includes a 0V to 2V Analog Dimming input to control the LED current: as an example the analog input can be provided via an ambient light sensor, a thermistor sensing the LED temperature, or the very common 0-10V dimming signal with the use of some external circuitry. In addition there are three independent PWM dimming inputs providing either independent control of several white LED strings or color mixing capability for optimal light temperature control. PWM frequency of up to 25kHz is supported to avoid audible noise. Fault conditions can be reported through a digital 2-wire serial bus interface (I2C and SMBus compatible) and include LED short, LED open, and IC over temperature indicators as well as information about the LED string voltage.

The IC also provides externally programmable LED current rise and fall time that can be used to optimize system EMI.

The LX2273 is designed to provide protection of the expensive LED lighting fixture while allowing continued operation in case of a fault (StayLIT™). The device also includes a variety of protection features such as output short circuit protection (without the need for an input fuse that may require cost intensive manual replacement), over-voltage protection, and over-temperature shutdown. In addition, the LED current can be compensated to stay within a given LED temperature profile by the use of an external thermistor.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website:
http://www.microsemi.com

KEY FEATURES

- Four LED Channels with Independent PWM Control
- Up to 500mA LED Current per Channel with External Power Components for Optimal Design and Thermal Management
  - 3% Current Setting Accuracy
  - 1.5% Channel to Channel Current Matching
  - Programmable LED Current Amplitude via SMBus or I2C
- Analog Dimming via Ambient Light Sensor, Thermistor or 0-10V Signal
- Wide Digital Dimming Range 3000:1 via PWM input
- StayLIT™ Feature to Enable Continued Operation in Case of a Fault (Open String or an LED Short)
- Short Circuit, OVP Protection
- SMBus and I2C Compatible Digital Diagnostic Reporting
  - LED Fault Status
  - String V monitoring
  - LED Over Temperature Warning & Protection
- Soft Start to Limit Inrush Current and Protect the LED's
- Programmable LED Current Rise/Fall Time for EMI Control

APPLICATIONS

- White or RGB LEDs for Single or Multiple Strings Solid State Lighting Applications
  - Street/ Parking Lot Lights, Down lights
  - Wall-washers
  - Commercial Spot Light etc.

PACKAGE ORDER INFO

T_A (°C)			THERMAL DATA
	DB	Plastic QSOP 36-pin	θ_{JA} = 70 °C/W
	LQ	Plastic 5 x 7 mm² QFN 38-pin	θ_{JA} = 19.3 °C/W
		RoHS Compliant / Pb-free	THERMAL RESISTANCE-JUNCTION TO AMBIENT
-40°C to 85°C		LX2273IDB LX2273ILQ	Junction Temperature Calculation: TJ = TA + (PD x θjA). The θJA numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX2273IDB-TR)

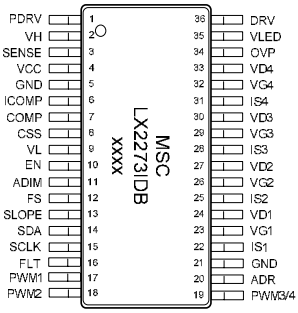
Microsemi
Analog Mixed Signal Group
One Enterprise, Aliso Viejo, CA 92656 USA, Within USA (800)713-4113, Outside USA (949)380-6100, Fax (949) 215-4996

ABSOLUTE MAXIMUM RATINGS

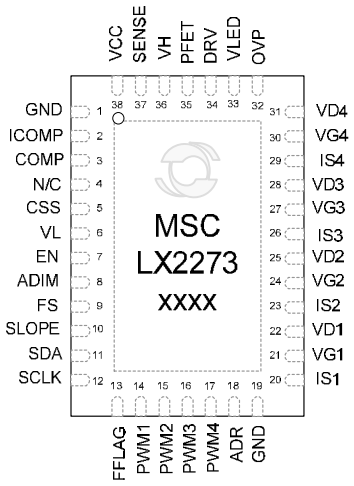
Supply Input Voltage VCC, SENSE, PFET,VH,VD1-4, EN, VLED .....-0.3V to 35V
VH to VCC ..... - 6V
VL to GND .....-0.3V to 6V
SDA, SCLK, PWM1-4, FFLAG .....-0.3V to 6V
All other pins .....-0.3V to VL+0.3V
Maximum Junction Temperature ..... 150°C
Storage Temperature Range .....-65°C to 150°C
Peak Package Solder Reflow Temperature (40 seconds maximum exposure) ..... 260°C

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" are not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

PACKAGE PIN OUT



DB



LQ
(Top View)
RoHS / Pb-free 100% Matte Tin Pin Finish

FUNCTIONAL PIN DESCRIPTION

Pin Name	DB PIN#	LQ Pin #	Description
GND	5	1	GND pin: The external NFET for DC-DC converter should return to this GND
ICOMP	6	2	Power converters current slope compensation. Connect a resistor from this pin to GND to compensate current slope. See "slope compensation section" for detail.
COMP	7	3	Boost Mode Compensation: Connect a series RC to GND.
N/C		4	Not Used
CSS	8	5	Feedback Soft-start: Connect a capacitor 4.7µF typical from this pin and GND.
VL	9	6	5V power supply output – Power Pin – Provides a regulated 5.25V typical to the internal and external 5V circuits.
EN	10	7	Enable Input. Pull low to put the system into sleep mode. If not used must tie to VCC.

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FUNCTIONAL PIN DESCRIPTION

Pin Name	DB PIN#	LQ Pin #	Description
ADIM	11	8	Analog Dimming Input: This input pin has 0V to 2V of control range. Connect ADIM to VL (5V) to force 100% output current when analog dimming is not used.
FS	12	9	Oscillator Frequency Setting pin. Connect a resistor R_{FS} between FS to GND to set the buck/boost frequency using the following formula: Freq [kHz] = 67000/R_{FS} where R is in kΩ.
SLOPE	13	10	LED current rise/fall time programmable pin. Connect a resistor from this pin to GND to program LED current rise/fall time for EMI purpose. If not used, tie this pin to VL.
SDA	14	11	Serial Data In/Output. Read data for fault conditions, LED string status via drain voltage, VLED voltage. SDA also can be used to set the LED peak current amplitude by writing to register 08h. Connect to GND if SDA is not used.
SCLK	15	12	Serial Clock Input. Maximum clock is 100kHz. Connect to GND if not used.
FFLAG	16	13	Fault signal output. Open drain output. This pin goes low when a fault condition is detected.
PWM1-4	17-19	14-17	Pulse Width Modulated dimming signal – Signal input. PWM input can be tied together for a common PWM signal or use for individual PWM control. PWM3 & PWM4 are internally connected together for DB package.
ADR	20	18	Address Setting: connect to VL, GND or leave it open for three different address choices. Refer to SERIAL INTERFACE section.
GND	21	19	GND pin
IS1-4	22,25, 28,31	20,23, 26,29	LED current setting. – Program this pin with an external resistor to set the LED current with 300mV internal reference voltage. I-LED = 300mV/R_{IS}
VG1-4	23,26, 29,32	21,24, 27,30	Gate Drive – CMOS Output Pin: Connect to the gate of the external NFET current sink. Any unused pins must be tied to ground to distinguish between intentionally unused and LED failed open.
VD1-4	24,27, 30,33	22,25, 28,31	Drain – Signal Pin – This connects to Drain pin of the external NFET switch. The boost output voltage regulates based on the lowest VD, and the lowest voltage is kept at 0.9V (typical). Any unused pins can be left open.
OVP	34	32	Over Voltage Protection – Signal input: An external voltage divider sets the maximum LED voltage. System will stop switching when OVP limit hits, and resume when it goes lower than the limit.
VLED	35	33	LED voltage. Connect this pin directly to common anode strings voltage.
DRV	36	34	Low-side NFET gate drive: Connect to the gate of the NFET
PFET	1	35	High-side PMOS gate drive: Connect to gate of a PFET. When the boost output short detected or EN signal low, PFET will open.
VH	2	36	High side power rail. Connect a 1µF 10V capacitor from this pin to VCC.
SENSE	3	37	Converters current sense negative pin. The differential input voltage across R_{SENCE} resistor used to set the peak inductor current. Use Kevin connection directly to the R_{SENCE} output side
VCC	4	38	Power supply input – Provides power to the IC. Must be closely decoupled to ground with ceramic capacitors.

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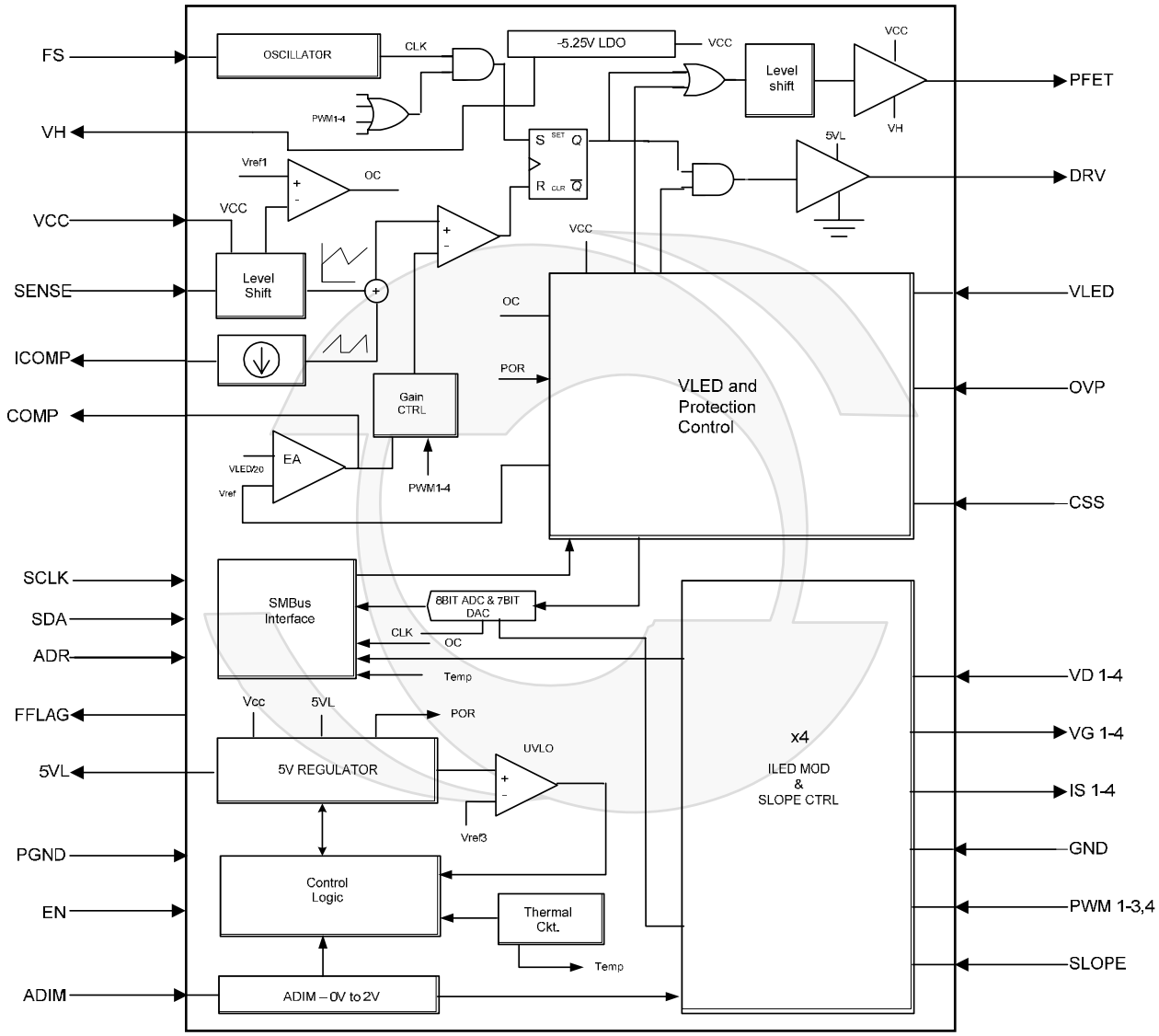
SIMPLIFIED BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature of -40°C ≤ T_A ≤ 85°C and the following test conditions: VCC = 12V; EN = 3V, RFS = 100kΩ (670kHz)

Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
Input Power Supply						
Input Voltage	VCC	Withstand voltage VCC = 35V	8		28	V
Quiescent current	ICC_{ON}	EN > 2 V, No PFET & NFET connected			10	mA
Sleep current	ICC_{SLEEP}	EN < 0.8V , VCC = 28V			25	µA
Control and Logic						
EN Logic High	V_{ENH}		2			V
EN Logic Low	V_{ENL}				0.8	V
EN Current High	I_{ENH}	EN = 3.3V			5	µA
EN Current Low	I_{EN-L}	EN < 0.8V			5	µA
Address High Input	V_{ADRH}		VL-0.8			V
Address Low Input	V_{ADRL}				0.8	V
Address Open	V_{ADRO}		2	VL/2	2.7	V
Address Input Low Current	I_{ADRH}		-20	-7		µA
Address Input High Current	I_{ADRL}			7	20	µA
FFLAG Output Low Voltage	V_{FFLAGH}	I_{LOAD} = 3mA			0.4	V
FFLAG Output High Leakage Current	V_{FFLAGL}	V_{FFLAG} = 5.5V			10	µA
DC/DC PWM Error Amplifier						
Peak Output Current	I_{OUT}			+/-40		µA
Output Resistance	R_{OUT}		2.6	4	8	MΩ
Forward Transconductance	gm	At EA inputs (I_{OUT}/(V_{LED}/20-V_{CSS})		120		µmho
Soft Start/Drain Voltage Sense Error Amplifier						
CSS Source Peak Current	I_{CSS}		-30	-20	-10	µA
CSS Sink Peak Current	I_{CSS}		10	20	30	µA
Forward Transconductance	gm		45	80	100	µmho
Output Resistance			2	5	7	MΩ
Valid Output Voltage Range	V_{CSS}	1/20 of V_{LED}	0.5		2	V
CT Fast Charge-up Current	CT_{CHG}	VD < 700mV	75	120	175	µA
Start Up Time	T_S	C_{CSS} = 0.47µF, R_{ISx} = 2Ω, V_{IS} setting 300mV, 100% PWM, at IS voltage > 90%		5	20	mS
Pulse Width Modulation Input						
PWM Input Low Voltage	V_{PWM_L}				0.8	V

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Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
PWM Input High Voltage	V_{PWM_H}		2			V
PWM Input Frequency	F_{PWM}		0.1		25	kHz
Minimum PWM Input Pulse Width	PW_{MIN}	Digital Dimming ; SLOPE = VL	2			µs
		Adjustable Slope Option to set t_R and t_F	2.5			x t_R or t_F
PWM Input Pull-down Resistor	PWM_R		25	100	200	kΩ
		Applies to PWM3/4 input, DB package only	12.5	50	100	
PWM Input to IS Output Delay		SLOPE = VL (minimum t_R, t_F)	2	6.5	10	µs
		R_{SLOPE} = 82.5kΩ (t_R,t_F~4µS)	5	9	15	µs
Device Protection						
OVP Threshold Voltage	$V_{TH\ OVP}$		1.87	1.97	2.07	V
Over Temperature Shutdown	$T_{OVT-SHDN}$	Rising temperature hysteresis, T_{HYS} = 20°C		150		°C
Shut Down Recovery	$T_{RECOVERY}$			120		°C
Over Temperature Warning	$T_{OVT-WARN}$	Rising temperature hysteresis, T_{HYS} = 15°C		130		°C
Clear Warning				105		°C
LED Current Output						
Sink Current Overshoot	$V_{ISET\ OVERS}$	VS setting at 100% , PWM Dimming			5	%
V-source Pk-Pk Matching Among Strings	$V_{ISET\ 150}$	R_{sense} = 2Ω, 0.8V≤ VD ≤ 3V (note 1) T_{AMB} = 25°C, PWM = 100% duty cycle,	295.5		304.5	mV
		F_{PWM} = 200Hz, PWM = 25% duty cycle	291		309	mV
Maximum IS voltage	V_{ISx}	R_{sense} = 2Ω, Average of the four outputs	291		309	mV
		R_{sense} = 2Ω, Each outputs	286.6		313.6	mV
Minimum VD regulation	V_{Dx}	At the lowest VD pin, I_{DS} = 150mA	800		1000	mV
IS In put Bias Current	I_{IS}	V_{IS} = 300mV			300	nA
DC Gain	A_{OL}			80		dB
Current Source Driver Op Amp						
On State VG Voltage Range	VG_{RANGE}	VG voltage that maintains DC accuracy	1.5		4	V
Off State VG Voltage	VG_{OFF}				0.1	V
VG Sink Current	VG_{SNK}	V_{VG} = 2.5V, V_{IS} = 0.4V, PWM = HIGH		-7		mA
VG Source Current	VG_{SRC}	V_{VG} = 2.5V, V_{IS} = 0.2V, PWM = HIGH		7		mA
VG Load Capacitance	C_{LG}				1500	pF
LED Current On/Off slope						
SLOPE Reference Voltage	V_{SLOPE}			2		V
I-LED Rise Time	$T_{I-LED\ RISE}$	SLOPE = 5VL F_{PWM} = 200Hz, PWM = 50% duty cycle CLG < 500pF	1	1.5	2.5	µs
I-LED Fall Time	$T_{I-LED\ FALL}$		1	1.5	2.5	µs
I-LED Rise Time	$T_{I-LED\ RISE}$	R_{SLOPE} = 82.5kΩ, T_{RISE}//T_{FAL}L = 10% to 90%	3	4.2	5.5	µs

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature of -40°C ≤ T_A ≤ 85°C and the following test conditions: VCC = 12V; EN = 3V, RFS = 100kΩ (670kHz)

Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
I-LED Fall Time	$T_{I\text{-}LED\ FALL}$	F_{PWM} = 200Hz, PWM = 50% duty cycle	3	4.2	5.5	µs
Analog Dimming						
AD Voltage	V_{AD}	I-LED = 95%; PWM1-4 = HIGH; Register 08h = x1111111	1.8	1.9	2.0	V
		I-LED = 6.7%; PWM1-4 = HIGH Register 08h = x1111111	0.05	0.2	0.34	
AD Input Bias Current	AD_{IIB}		-1		1	µA
Analog Control Output Range	V_{IS}	PWM1-4 = High Register 08h = x1111111	5		100	%
SMBus LED Peak Current Adjustment						
Adjustment Range	I_{PADJ}	V_{IS} = 300mV represents maximum current setting	15.4		100	$\%V_{IS}$
Resolution	I_{RES}	2 mV translates out to be 7 bits DAC		2		mV
LED short/open Protection						
LED Short Threshold Voltage (note 1)	VDx_{SHORT}	F_{PWM} = 25kHz, PWM = 10% duty cycle	6.7	7.2	7.7	V
Derated IS Voltage		VD > 7.75	5	10	15	%
LED Open Threshold Voltage	VDx_{OPEN}	F_{PWM} = 25kHz, PWM = 10% duty cycle	0.18	0.24	0.27	V
Inductor Over Current Protection						
Maximum Short Circuit Current	I_{LSHORT}	With 10mΩ current sense resistor, L = 15µH		10		A
Over Current Threshold Voltage	I_{OC}	At current sense inputs		100	130	mV
SENSE Input						
Sense Input Voltage Range	V_{SENSE}	For design reference only, reference to VCC (this is the same parameter as over current threshold. Current sense comparator's input maximum is 150mV that accounts for slope compensation.)			100	mV
Sense Sink Current	I_{SENSE}	For design reference only		1		µA
VL Regulator (5.0V)						
VL Output	5V	8V ≤ VCC ≤ 28V; 0mA ≤ I_{VL} ≤ 15mA	4.75	5.00	5.25	V
VL Source Current	$5V_{CURRENT}$	Not include internal 5V supply. VCC = 8V		10	15	mA
UVLO	VL_{UVLO}	VL rising, V_{HYS} = 0.50V	3.75	4.25	4.65	V
VH (VCC-5.25V) Regulator						
VH Output Voltage	VH	8V ≤ VCC ≤ 28V; 0mA ≤ I_{VH} ≤ 15mA Reference to VCC	-4.75	-5.25	-5.5	V
UVLO	VH_{UVLO}	VH falling, VHYS = 0.50V. Internal POR activates on VH falling UVLO threshold, reference to VCC	-4.65	-4.25	-3.75	V
Oscillator						
FS Reference Voltage	V_{FS}		1.85	2	2.1	V
Oscillator Frequency	F_{SW}	R_{FS} = 100kΩ	600	670	740	kHz

ELECTRICAL CHARACTERISTICS

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Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
Oscillator Frequency Setting Range	F_{RANGE}		400		800	kHz
DC/DC Switching NFET Driver						
DRV Voltage High	V_{DRVH}		4.6	5	5.5	V
DRV Rise Time	T_{RISE}	C_L = 1000pF		25	50	ns
DRV Fall Time	T_{FALL}	C_L = 1000pF		15	50	ns
Off Voltage	V_{DRVOFF}	EN = 0V		0	0.7	V
DC/DC Switching PFET Driver						
PFET High Voltage	V_{PFETH}	EN = 0V, refer to VCC		0	0.5	V
PFET Low Voltage	V_{PPFETL}	Refer to VCC	-5.8	-5.25	-4.5	V
Overall System Efficiency	η	V_{IN} = 12V, VS setting at 100%, PWM = 100%		87		%
SMBus						
SDA, CLK Input Low Voltage	I_{LV}				0.7	V
SDA, CLK Input High Voltage	I_{HV}		2			V
SDA, CLK Input Hysteresis	IH_{YS}			100		mV
SDA,CLK Input Bias Current	I_{IB}		-5		+5	µA
SDA Output Low Sink Current	O_{SNK}	V_{SDA} = 0.4V	4			mA
SMBus Frequency	F_{SMBUS}		10		100	kHz
SMBus Free time	T_{BUF}		4.7			µs
CLK Serial Clock High Period	T_{HIGH}		4			µs
CLK Serial Clock Low Period	T_{LOW}		4.7			µs
Start Condition Set-up Time	$T_{SU:STA}$		4.7			µs
Start Condition Hold-up Time	$T_{HD:STA}$		4			µs
Stop Condition Set-up Time from CLK	$T_{SU:STO}$		4			µs
SDA Valid to CLK Rising Edge Set-up Time, Slave Clocking Data	$T_{SU:DAT}$		250			ns
CLK Falling Edge to SDA Transition	$T_{HD:DAT}$		0			ns
CLK Falling Edge to SDA Valid, Reading Out Data	T_{DV}		200			ns

Note: 1. When the different V_{DRAIN} voltages are more than 2V, then a single LED short may shut off the string that has a highest V_{DRAIN} (VD hits the limit). However V_{SOURCE} pk-pk matching will not be effected in this circumstance.

SERIAL INTERFACE

SMBus INTERFACE

LX2273 is a nine-register device which uses SMBus or I²C protocols to communicate with the host system. All registers are defined as full byte wide. Some registers contain reserved (undefined) bits with a default value of "0", or are read only bits that are status indicators. Two of the nine registers are capable of both read and write, and seven registers are read only. See the LX2273 Register Definitions section for details.

The LX2273 communicates over the SMBus and operates in a "slave" mode receiving commands and sending / receiving data to / from the host or "master". Only standard two-wire SMBus and I²C compatible serial bus and protocols may be used for this device. The LX2273 can be configured for one of the three addresses by connecting the ADR input pin to ground, $V_{DD,}$ or simply leaving it OPEN.

Address Strapping Codes

Option #	ADR	Address
1	GND	0101 100b
2	OPEN	0101 110b
3	V_{DD}	0101 111b

In this document, the SMBUs address occupies high seven bits of an eight bit field on the bus, the low bit is always the R/W bit.

Address = 0101100xb

1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Data Byte**	**A**	**P**
	0 1 0 1 1 0 0	**0**				

Address = 0101110xb

1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Data Byte**	**A**	**P**
	0 1 0 1 1 1 0	**0**				

Address = 0101111xb

1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Data Byte**	**A**	**P**
	0 1 0 1 1 1 1	**0**				

SMBus PROTOCOL

The only required command protocols are SMBus Send Byte, Receive Byte, Read Byte / Word, and the Write Byte / Word protocols.

Writes to registers can be performed by either the SMBus Write Byte / Word protocols and / or by internal IC logic, depending on the register type.

Read can be performed on all registers by issuing the Read Byte / Word protocol. Read Only registers can be written only by internal logics. Their contents will not be affected by SMBus write commands.

When LX2273 is initially powered, it will first test the address selection pin input to determine its own address and then look for its unique address each time it detects a "Start Condition". If the address does not match, the LX2273 ignores all bus activity until it encounters another "Start Condition".

SMBus Packet Protocol Diagram Element Key

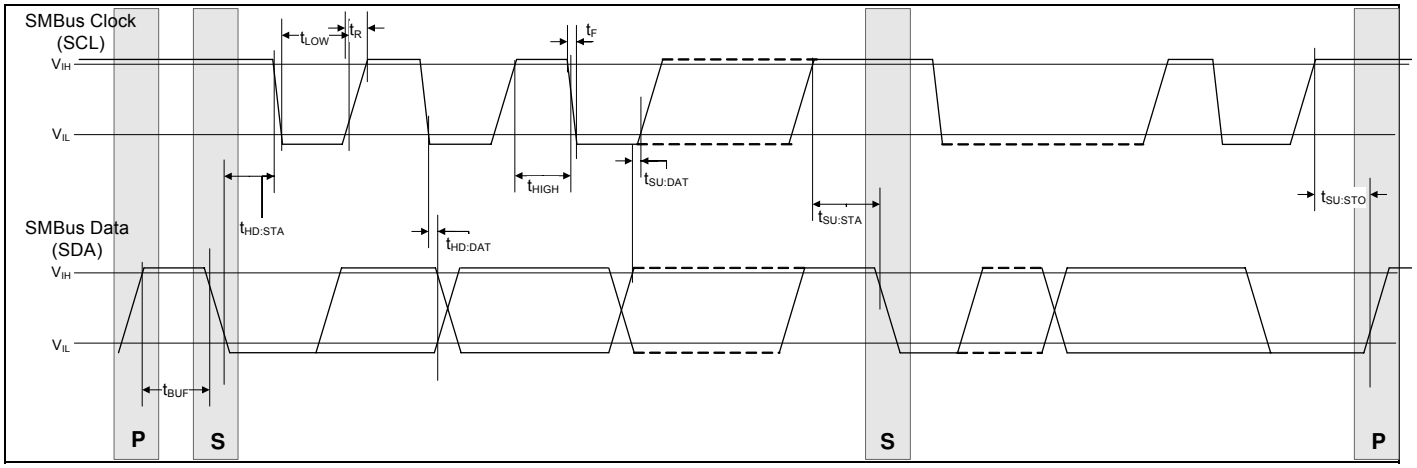
S	Slave Address	Wr	A	Data Byte	A	P
			X		X	

S Start Condition
Rd Read (bit value of 1)
Wr Write (bit value of 0)
A Acknowledge ('0' for an ACK, or '1' for a NACK)
P Stop Condition
Command Code Register Address
☐ Master-to-Slave ▩ Slave-to-Master

Protocols used to communicate with LX2273 must be per standard SMBus specification version 2.0 or higher.

SERIAL INTERFACE

SMBus Timing Measurement



Register Definitions
The LX2273 includes a registers to monitor the fault status. The slave address is set by the ADR signal inputs as follows:

VD Register: Address is 00h to 03h. This register has 8 bits that allows monitoring the drain voltage (VD). This voltage will reveal the string status, i.e., LED short/open. It is suggested that the input PWM duty cycle be reduced when a LED short is detected to avoid LED current sink NFET overheating.
VLED Register: Address is 04h. This register has 8 bits that allow monitoring the Boost output voltage (VLED).
String 1& 2 status Register: Address is 05h. This register has 8 status bits that allows monitoring the string 1 & 2 status.
String 3& 4 status Register: Address is 06h. This register has 8 status bits that allows monitoring the string 3 & 4 status.
Fault/Status Register: Address is 07h. This register has 8 status bits that allows monitoring the backlight controller's operating state.

REGISTER 00h	VD1 (drain voltage monitoring)
REGISTER 01h	VD2 (drain voltage monitoring)
REGISTER 02h	VD3 (drain voltage monitoring)
REGISTER 03h	VD4 (drain voltage monitoring)
REGISTER 04h	VLED (LED Anode voltage monitoring)
REGISTER 05h	String 1 & 2 status
REGISTER 06h	String 3 & 4 status
REGISTER 07h	Faults
REGISTER 08h	LED Peak Current Reference Voltage Adjustment

REGISTER 00h to 03h		**Drain voltage monitoring**			**DEFAULT VALUE 0x00**		
VD	**VD**	**VD**	**VD**	**VD**	**VD**	**VD**	**VD**
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT FIELD	DEFINITION	DESCRIPTION
Bit 0-7 (R)	Drain voltage	8-bit drain voltage monitoring. 256 steps for 8V. (bit 7 is MSB)

SERIAL INTERFACE

REGISTER 04h		LED voltage monitoring			DEFAULT VALUE 0x00		
VLED	VLED	VLED	VLED	VLED	VLED	VLED	VLED
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT FIELD	DEFINITION	DESCRIPTION
Bit 0-7 (R)	LED voltage	8-bit LED voltage monitoring. 256 steps for 67.9V. (bit 7 is MSB)

REGISTER 05h:		String 1&2 Status Register			DEFAULT VALUE 0x00		
String #2 not Used	String #1 not Used	S1_OV	S1_OPEN	S1_ NOTUSE	S2_OV	S2_OPEN	S2_NOTUSE
Bit 7 (W)	Bit 6 (W)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT FIELD	DEFINITION	DESCRIPTION
Bit 7	String #1 not Used	Set 1 when string #1 is not used to mask string faults on the string. Bit 6 and 7 are written to register 05h by the systems via SMBus to let the LX2273 know the unused string so the LX2273 can remove it from the fault detection/reporting. At power up system must disregard fault reporting and FFLAG (software timer) until the systems has finished setting string not used bit (set bit 6 and or 7 to high) and have received acknowledge from LX2273. LX2273 sends an acknowledgement after masking string fault.
Bit 6	String #2 not Used	Set 1 when string #2 in not used to mask sting faults on the string.
Bit 5	S1_OV	String 1 Over Voltage (1 = VD > 6.75V)
Bit 4	S1_OPEN	String 1 Open (1 = string open)
Bit 3	S1_ NOTUSE	String 1 status (1 = string is not used)
Bit 2	S2_OV	String 2 Over Voltage (1 = VD > 6.75V)
Bit 1	S2_OPEN	String 2 Open (1 = string open)
Bit 0	S2_NOTUSE	String 2 status (1 = string is not used)

BIT FIELD	DEFINITION	DESCRIPTION					
REGISTER 06h		String 3&4 Status Register			DEFAULT VALUE 0x00		
String #4 not Used	String #3 not Used	S3_OV	S3_OPEN	S3_ NOTUSE	S4_OV	S4_OPEN	S4_ NOTUSE
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)
Bit 7	String #3 not Used	Set 1 when string #3 in not used to mask sting faults on the string. Bit 6 and 7 are written to register 06h by the systems via SMBus to let the LX2273 know the unused string so the LX2273 can remove it from the fault detection/reporting. At power up system must disregard fault reporting and FFLAG (software timer) until the systems has finished setting string not used bit (set bit 6 and or 7 to high) and have received acknowledge from LX2273. LX2273 send acknowledge after masking string fault					
Bit 6	String #4 not Used	Set 1 when string #4 in not used to mask sting faults on the string.					
Bit 5	S3_OV	String 3 Over Voltage (1 = VD > 6.75V)					
Bit 4	S3_OPEN	String 3 Open (1 = string open)					
Bit 3	S3_ NOTUSE	String 3 status (1 = string is not used)					
Bit 2	S4_OV	String 4 Over Voltage (1 = VD > 6.75V)					
Bit 1	S4_OPEN	String 4 Open (1 = string open)					
Bit 0	S4_ NOTUSE	String 4 status (1 = string is not used)					

SERIAL INTERFACE TIMING

REGISTER 07h			Faults Register		DEFAULT VALUE 0x00		
RESERVED	RESERVED	RESERVED	RESERVED	OC SHDN	OC	OTP	T_Warning
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R/W)	Bit 2 (R)	Bit 1 (R/W)	Bit 0 (R)

BIT FIELD	DEFINITION	DESCRIPTION
Bit 3	OC SHDN	OC shutdown (1 = OCP shut down, 0 = OC SHDN OK). Reset after reading or by En = Low
Bit 2	OC	Input OC (1 = over current condition, 0 = OC OK). Reset after reading or by En = Low
Bit 1	OTP	OTP Shutdown (1 = OTP shut down, 0 = T_{OK}). (note 1)
Bit 0	T WARNING	Temperature warning (1 = $T_{WARNING}$, 0 = T_{OK}). (note 2)

REGISTER 08h			ILED Setting Register		DEFAULT VALUE 0x7F		
ADIM	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT FIELD	DEFINITION	DESCRIPTION
Bit 7	X	don't care
Bit 6:0	ILED bit6:0	To program LED current setting reference voltage, see note below.

Register 08h: LED Peak Current Adjustment (7 bits used for 128 steps)

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	V_{IS} (mV)
0	0	0	0	0	0	0	46
0	0	0	0	0	0	1	48
0	0	0	0	0	1	0	50
0	0	0	0	0	1	1	52
0	0	0	0	1	0	0	54
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	0	298
1	1	1	1	1	1	1	300

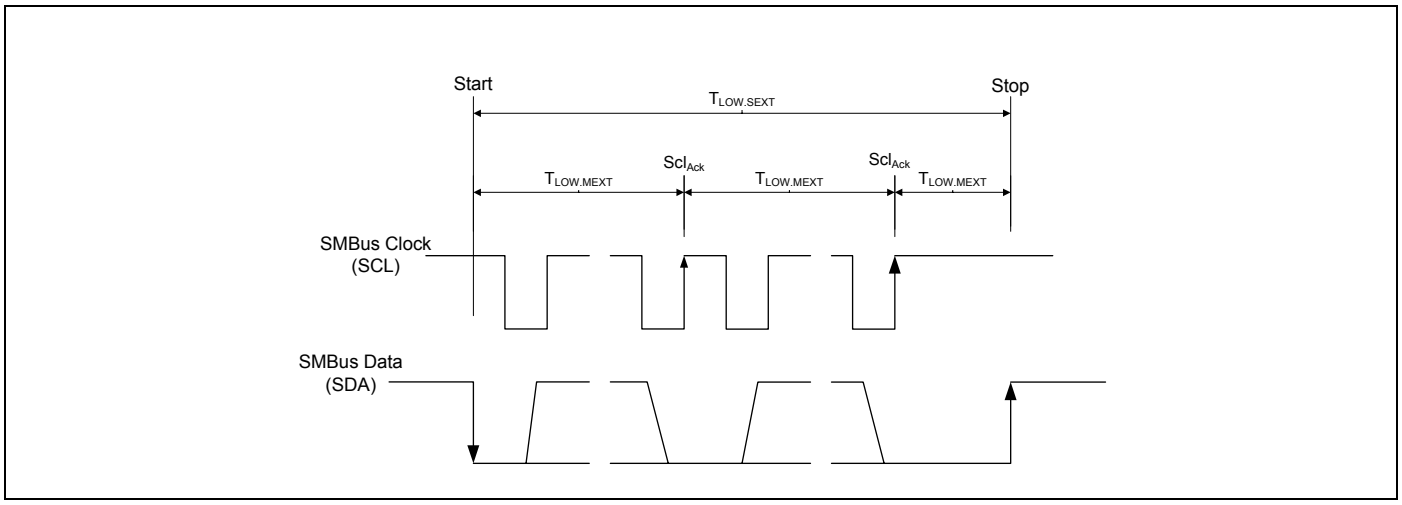
Default LED reference is 300mV regardless SDA/SCLK state at POR.

Note:

1. OTP bit change state from "0" to "1" and latched when the real time OTP changes from "0" to "1".
2. T WARNING bit changes state from "0" to "1" and latched when the real time T WARNING change from "0" to "1".

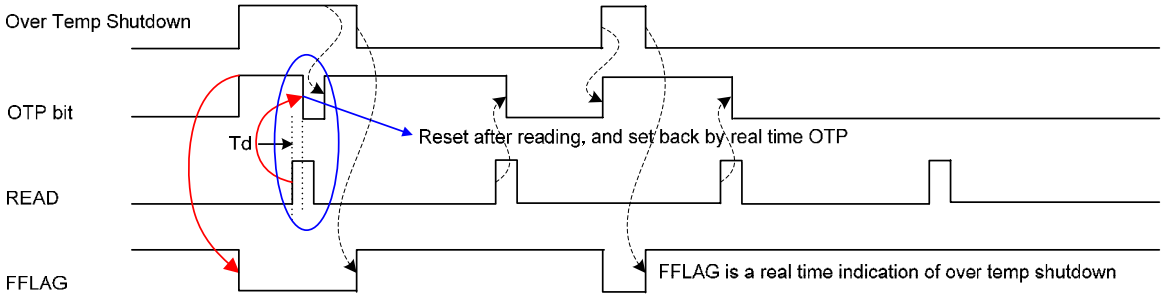
SERIAL INTERFACE TIMING

Timeout Measurement Interval



Faults Timing Diagram

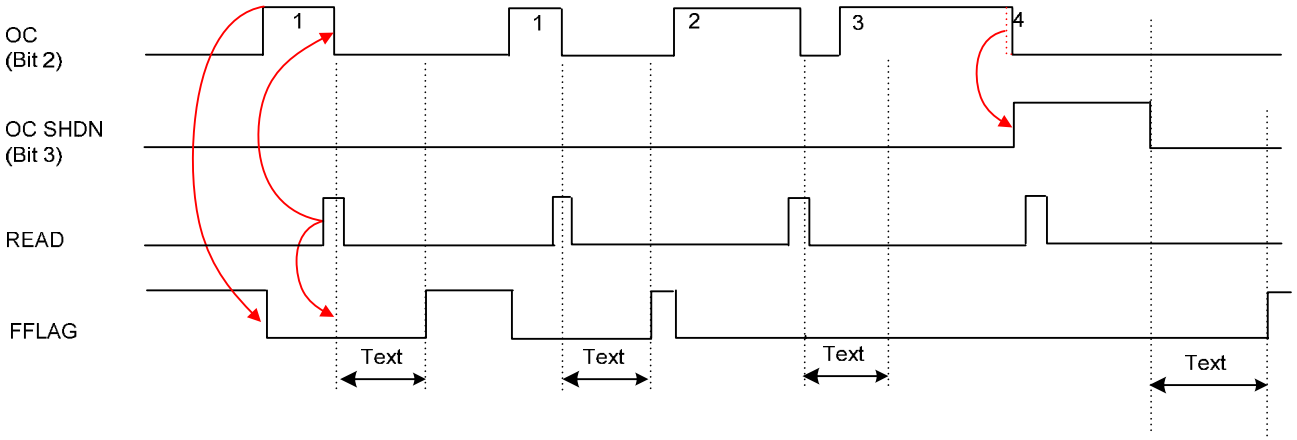
OTP Timing (Bit 1, Reg 07h)



FFLAG stays low when the chip is in over temperature shutdown mode.
OTP bit is latched by over temperature warning signal.
FFLAG and OTP reset after reading and real time OTP is low. (Real time OTP not show)
Td < 1usec.
This timing diagram shows relationship between Over temperature Shutdown output and OTP bit, FFLAG only without any other fault conditions. In an actual application, FFLAG will not represent Over Temp Shutdown from temperature monitor because FFLAG is a NORed output of all faults and over temperature warning is always true when Over Temp Shutdown is true.

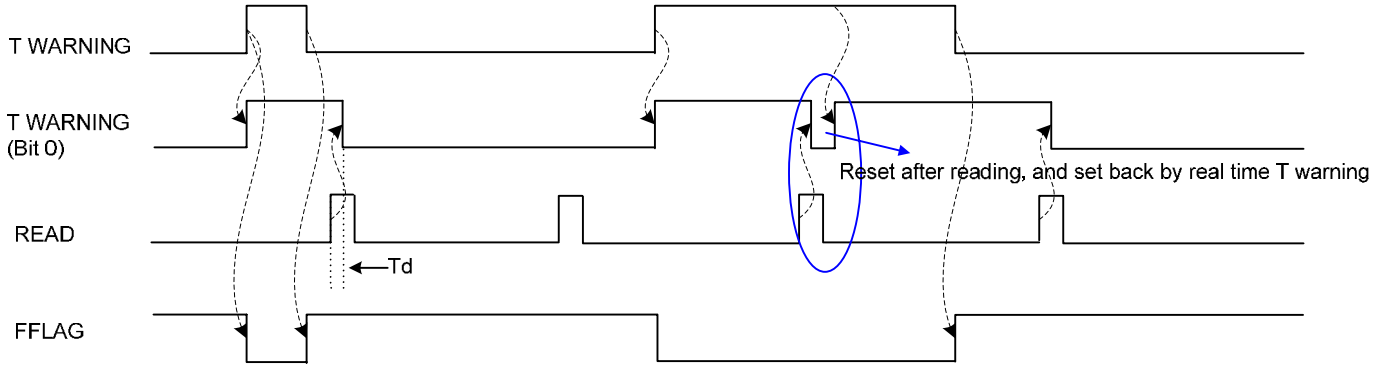
SERIAL INTERFACE TIMING

OC Timing



FFLAG is Low whenever OC or OC SHDN occurs and extended by an internal timer.
OC and FFLAG register bits are reset after reading. (Real time OC not shown)
Fault bits are set back when the fault conditions present.

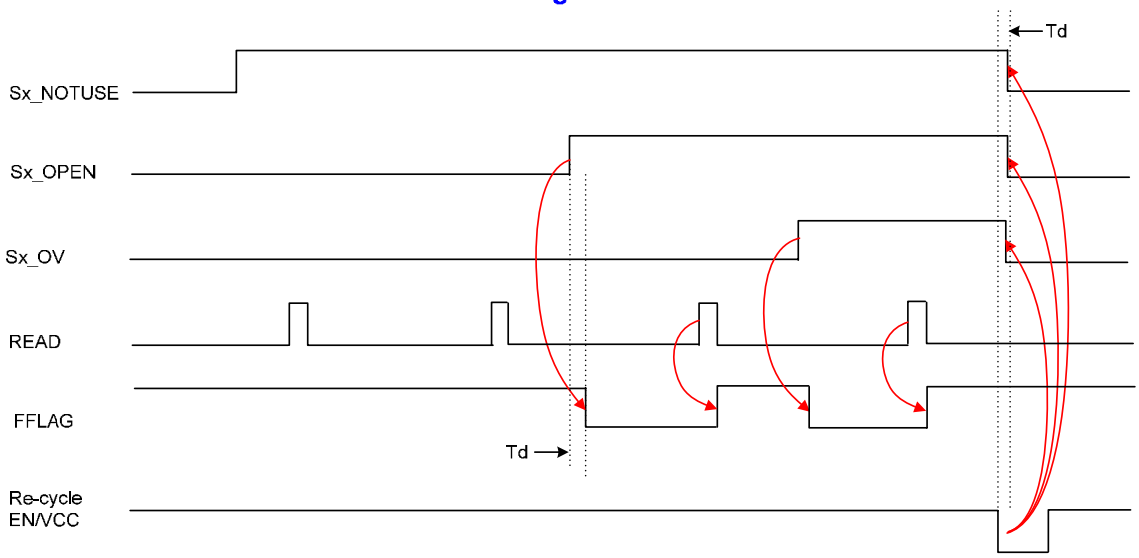
T Warning Timing (bit 0 Reg 07h)



FFLAG is Low whenever T Warning occurs.
T Warning bit is reset after read access and when real time T warning is low.
There are some Tdelay (Td) from real time T WARNING "1" to set T WARNING & FFLAG, as well as from end read
Td < 1usec.

SERIAL INTERFACE TIMING

Strings Status Timing Diagram



FFLAG is Low whenever String OV or String OPEN occurs.
FFLAG reset after reading.
Strings status are latched and be reset by recycling EN signal or Vcc
Td < 1usec.

THEORY OF OPERATION

Operation Theory

The LX2273 operates in fixed frequency boost converter mode PWM controller to regulate the necessary voltage to the LED array. Fixed switching frequency is set by an external resistor, from 400kHz to 800kHz. LX2273 will regulate the lowest drain voltages (typ. 0.9V) to minimize the power loss through the external current sink NFETs. The voltage across an external input current sense resistor (typical 10mΩ) is used for limiting the switching current (coil current) cycle-by-cycle.

Inductor Selection

To keep the circuit in constant current mode (CCM), the maximum ripple current should be less than twice the minimum load current. Due to the effective of RHP zero on Error Amplifier compensation, select the minimum load = IOUT. The following formulae use to calculate the inductor values in boost mode.

Minimum inductor value for boost converter:

Where $f_S \approx 600kHz$

$$L_{BOOST} \geq \frac{V_{IN} \cdot (V_O - V_I)}{(V_O \cdot f_S \cdot I_O \cdot \%\Delta_I)}$$

Where $V_{IN} = V_O/2$, $\%\Delta I = \Delta_I/I_O$

Slope Compensation.

LX2273 operates in fixed frequency CCM mode. Therefore, in some conditions, the duty cycle may extend beyond 50%. This condition will cause sub-harmonic instability. The cure for this is adding an additional ramp current. An external resistor will set the ramp current for the internal current slope compensation circuit.

Use the following equation to set the external resistor for the slope compensation:

Ricomp[kΩ] = 66.7*L[µH]/Rsense[mΩ]

This is a theoretical minimum slope compensation required to avoid subharmonic distortion. User may required to add larger slope compensation in the real application. Amount of slope compensation is inversely proportional to the R_{ICOMP} resistor.

Start-up

The start-up or wake-up is controlled to minimize inrush or to eliminate the starting surge current required from the input power supply. EN pin input is always alive, therefore the LX2273 consumes a minimal amount of current even when the chip is in sleep mode (EN=low). After EN assertion, 5V regulator is turned on first. Once the 5V regulator output (VL) reaches to UVLO limit, VCC-5.25V (VH) regulator turns on. After VH is ready, an internal POR is set then the rest of circuit turns on after POR time-out (100µs typ.).

LX2273's start-up time is set by an external capacitor C_{CSS}. During start-up, C_{CSS} is charged up at 120µA until lowest VD reaches to 700mV. Use the following equation to estimate the start up TSU.

$$Tsu \cong C_{CSS}/120\mu A/20*((V_{LEDtarget}-1V) + (0.7V+dVD)/D_{PWM})$$

To speed up the startup time with low PWM duty cycle, user may try to stagger the PWM inputs so that the DC/DC converter stays active for an extended time. The LX2273's DC/DC converter is active when any of the active string's PWM inputs are high.

Over current (OC) and over current shut down (OC SHDN). (Requires external PFET)

In any mode of operation once over current (OC) is detected, the PDRV turns off for 4 switching clock cycles and then resumes operation. An internal 4 event counter accumulates the number of over current triggers that happen within 128 clock cycles. In other words, the 4 event counter is reset by 1/128 clock. At the 4th over current event (in case there is the 1/128 reset coming before the 4th trigger, total number of over current triggers that cause shutdown became more than 4), the chip shuts off the DC-DC converter and discharges CSS capacitor to 75mV. The chip resumes operation thereafter. If the over current condition is still present, the chip repeats the shut down and recovery cycle. The status of over current (OC) will set Bit 2 of register 07h to "1". Bit 2 will reset after reading. Hiccup cycle during the over current protection depends on dimming PWM duty. The cycle is inversely proportional to the PWM duty.

THEORY OF OPERATION- CONTINUTED

Over Temperature Protection (OTP).

In any mode of operation once over OTP is detected, the LX2273 will shutdown. The status of OTP will set Bit 1 of register 07h to "1". Bit 1 will reset after reading in real time and OTP is low. System will resume operation when temperature drops below OTP threshold voltage.

Temperature Warning (T_Warning).

In any mode of the converter or any test condition, once T_warning is detected, the status of T_warning will set Bit 0 of register 07h to "1". Bit 1 will reset after reading in real time that T_Warning is low.

Fault Flags:

The following faults will set the FFLAG to "Low", and be reset either by after reading via SMBus. The fault output is intended to stay low for an extended period after internal faults are cleared. The timer is 8mS typical with 100kohm on FS pin.

Fault Condition	Register /Bit	Reset By	Notes
String Over Voltage	Register 05h & 06h, bit 2 & 5	Toggle EN or VCC	When VD >6.75V
String Open	Register 05h & 06h, bit 1 & 4	Toggle EN or VCC	When VD <0.2V
T-WARNING	Register 07h bit 0	After reading & real time T WARNING is Low	
OTP	Register 07h bit 1	After reading & real time OTP is Low	
OC	Register 07h bit 2	After reading & real time OC is Low	
OC SHDN	Register 07h bit 3	After reading & chip resumes start up	

5V Regulator

The 5V regulator generates 5V from VCC to the internal low voltage circuit and also provides power for an external light sensor (such as LX1973). Maximum output current is limited to 10mA for the external devices. The 5V output requires at least 0.1µF connected across 5V pin and GND for phase compensation. A 1µF capacitor is recommended and should be placed near the near the 5V and tied to the GND plane. The 5V is shut off while the chip is in sleep mode (EN = low).

VCC-5.25V Regulator

VCC-5.25V (VH) is a floating VSS for the low voltage circuits residing across VCC and VH. During start up, VH is turned on after VL gets ready.

POR

POR is cleared 100µS (typ.) after VH exceeds internal VH UVLO threshold.

PWM Dimming

The LED strings current are individual controlled directly by PWM input. A high on PWM input enables the output current.

DC Dimming

DC dimming can be achieved, but not independently. In this mode, all the PWM inputs must be tied to VL, while the DC control signal goes to ADIM pin. The DC input range from 2V to 0V corresponding from 100% to 5% of LED current setting.

OVP

Two external resistors program the LX2273's OVP level. The threshold is set to 2V (typical) at the OVP pin. When the OVP voltage threshold is reached it will stop the power converter from switching and then resume when the OVP pin voltage drops below the 2V threshold. The OVP function is active whenever the EN signal is high regardless the LED current condition.

THEORY OF OPERATION- CONTINUTED

LED Open/Short Detection

In case an LED fails open or an opened string, the VD pin drops down to 0V. The power converter will try to raise the VLED under this condition. The open string will then latch off when VLED voltage reaches 100% of OVP setting. At latch off this string's VD pin voltage is excluded from the power supply regulation loop. The power converter will stop switching until the highest VD pin voltage drops below 2V and the OVP pin voltage is less than 2V. Any change in the VLED voltage should have minimum impact to the LED output current since they are current source outputs. However, the chip may shut down and recover after successful latch off of the open string depending on input, output voltage and other conditions. LED short protection is temporarily disabled when one or more open strings are detected. This allows VD to go beyond the LED short protection threshold of 7.25V (typ.). After successful latch off of any open string the VD voltage returns to a normal regulation level. The LX2273 reduces the LED current reference voltage to 10% while VD>7.25V to avoid the external FET from overheating. The LED current returns to normal level when VD voltage gets below 7.25V. Cycling power or the EN input will reset any latched off VD pin. User must tie VG pin to GND for any unused string to distinguish between string failed open and strings unused. During this condition, any string that has VD higher than the LED short threshold voltage will not be latched off and not be report with VD is higher than 6.75V. The LED short fault is masked when any of VD is below open LED detection threshold until such string is latched off. Broken PWM input lines will be checked during start and reported as corresponding strings open

In case of the LED short condition, LX2273 output works normally until the VD voltage reaches the LED short threshold voltage, and the corresponding string is turned off. LED short protection works this way when there are more than two active strings and the lowest VD regulation is at normal level (0.24V<VD<2V). This allows the VD voltage to go beyond the LED short threshold in case of an open string or temporary instability on VLED output. When there is only one active string in the system, the last string is latched of when VD voltage reaches to 7.25V. VD of the latched off strings are excluded from the power converter regulation loop. LED short detection is masked for 7µS (typ.) at the beginning of each PWM cycle to avoid false shutdown of LED strings.

Note: The size of NFET current sink must increase to handle LED short or VD voltages in excess of the LED short threshold voltage. Otherwise, the relative PWM input duty cycle must be reduced if smaller NFET is used.

Current Source Driver

This is the current source driver for the external LED current sink NFET. The driver output VGx, and the feedback signal ISx will regulate the LED current through an internal op amp with a 300mV band gap (current source reference), for unused string will tie VG to ground. The lowest drain voltage of any external current sink NFET is used to regulate the boost voltage output. All the drains will report back to host computer through the SMBus to determine the strings status (number of shorted LED, open LED) The LED current matching between strings is 1.5% when matched with an external current sense resistor whose tolerance is 0.1% at room ambient temperature. The IC specifies voltage only at ISx pin and the voltage matching is +/-1.5%.

LED Output Current Rise/Fall Time Control

LX2273's LED output current rise/fall time can be programmed by one external resistor connected between SLOPE and GND.

Rise/Fall time can be calculated by:

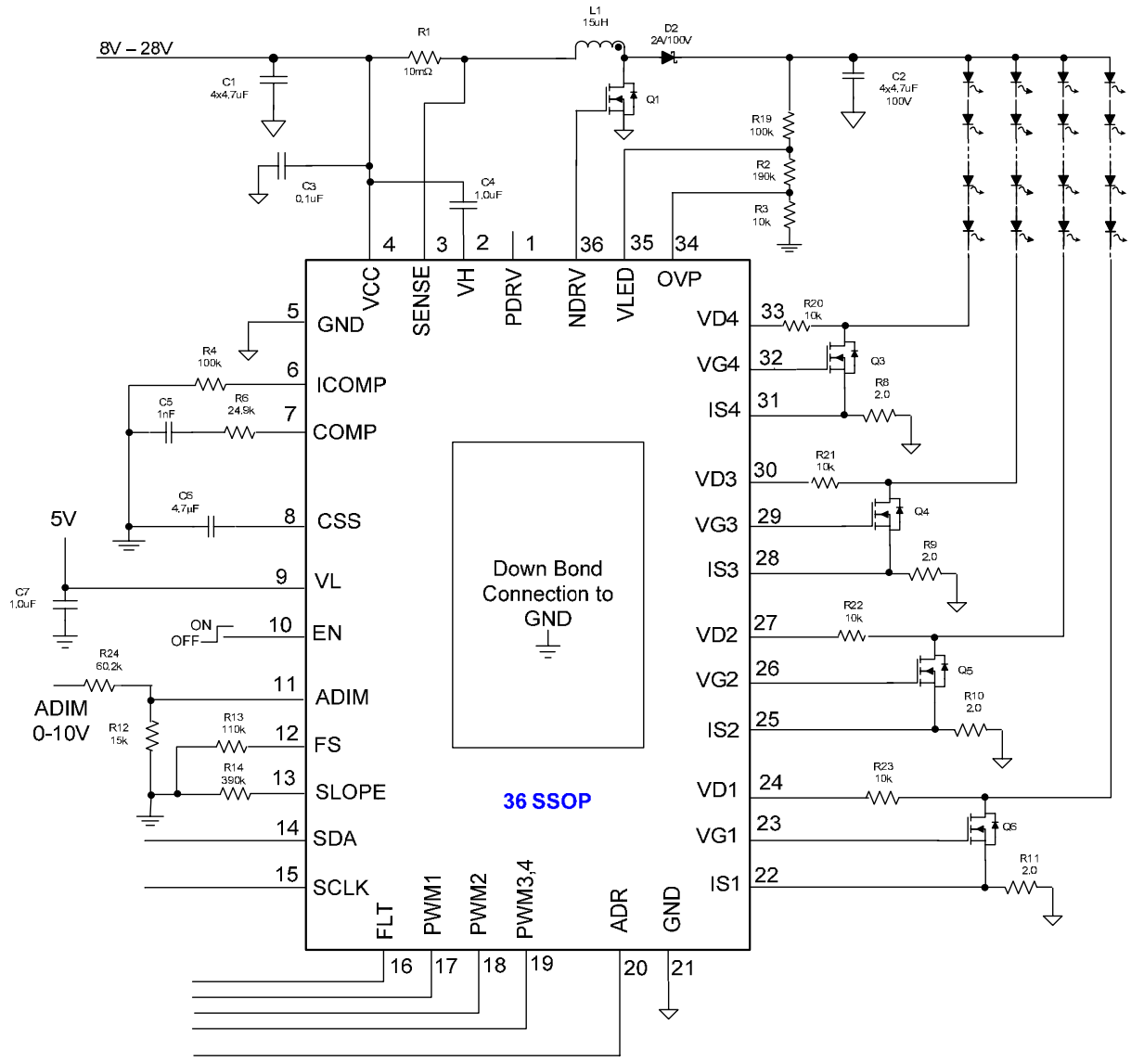
R_{SLOPE} [kΩ] ≅ 20*Tr,Tf [µs]

Use 20k and greater resistor.

Connect SLOPE pin to VL when slope control is not used. 5V on SLOPE pin selects an internal 20kohm.

TYPICAL APPLICATIONS

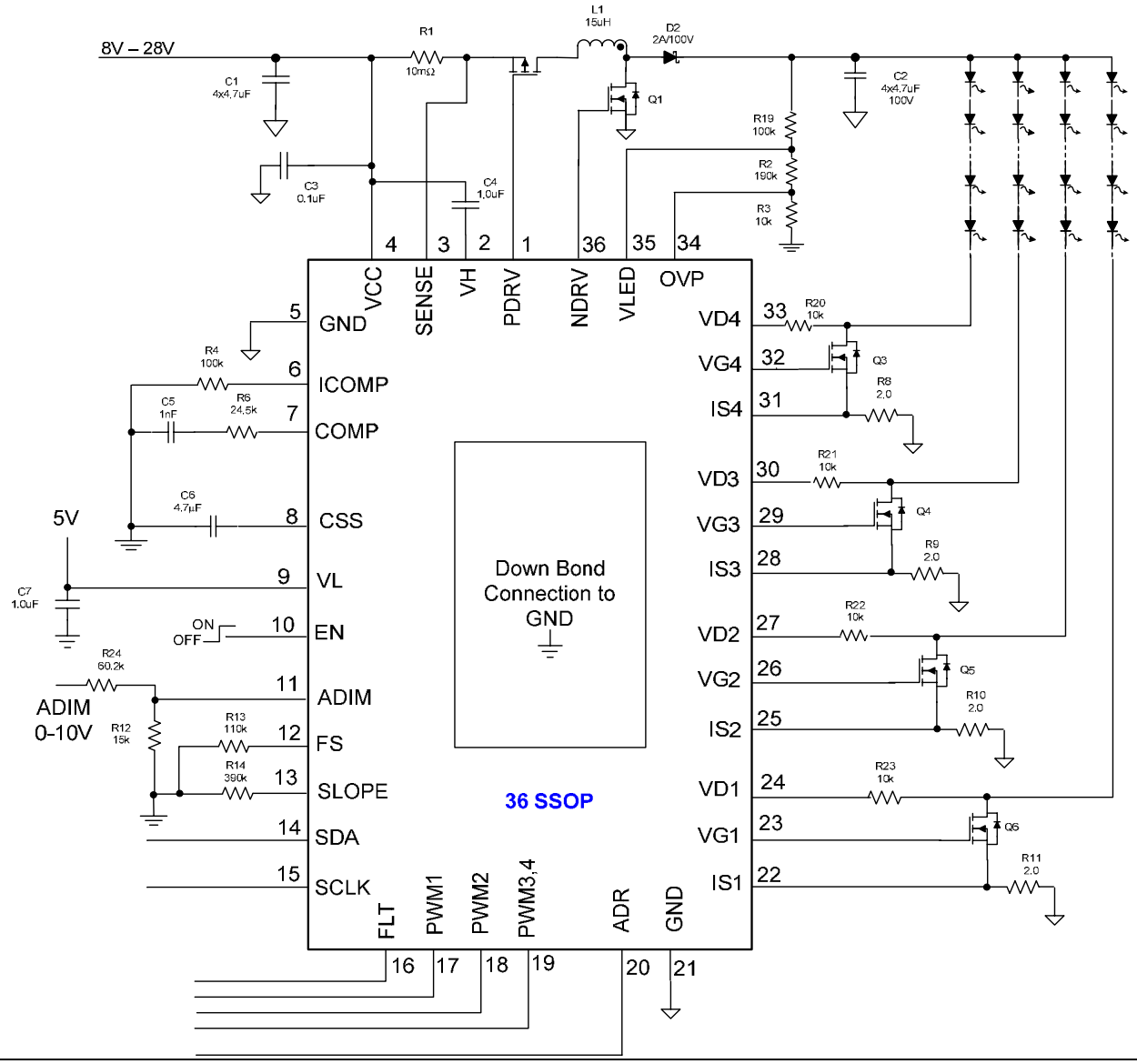
Typical Application Circuit 1: Boost Mode Converter (Vin < Vo<60V



The component values are for reference only

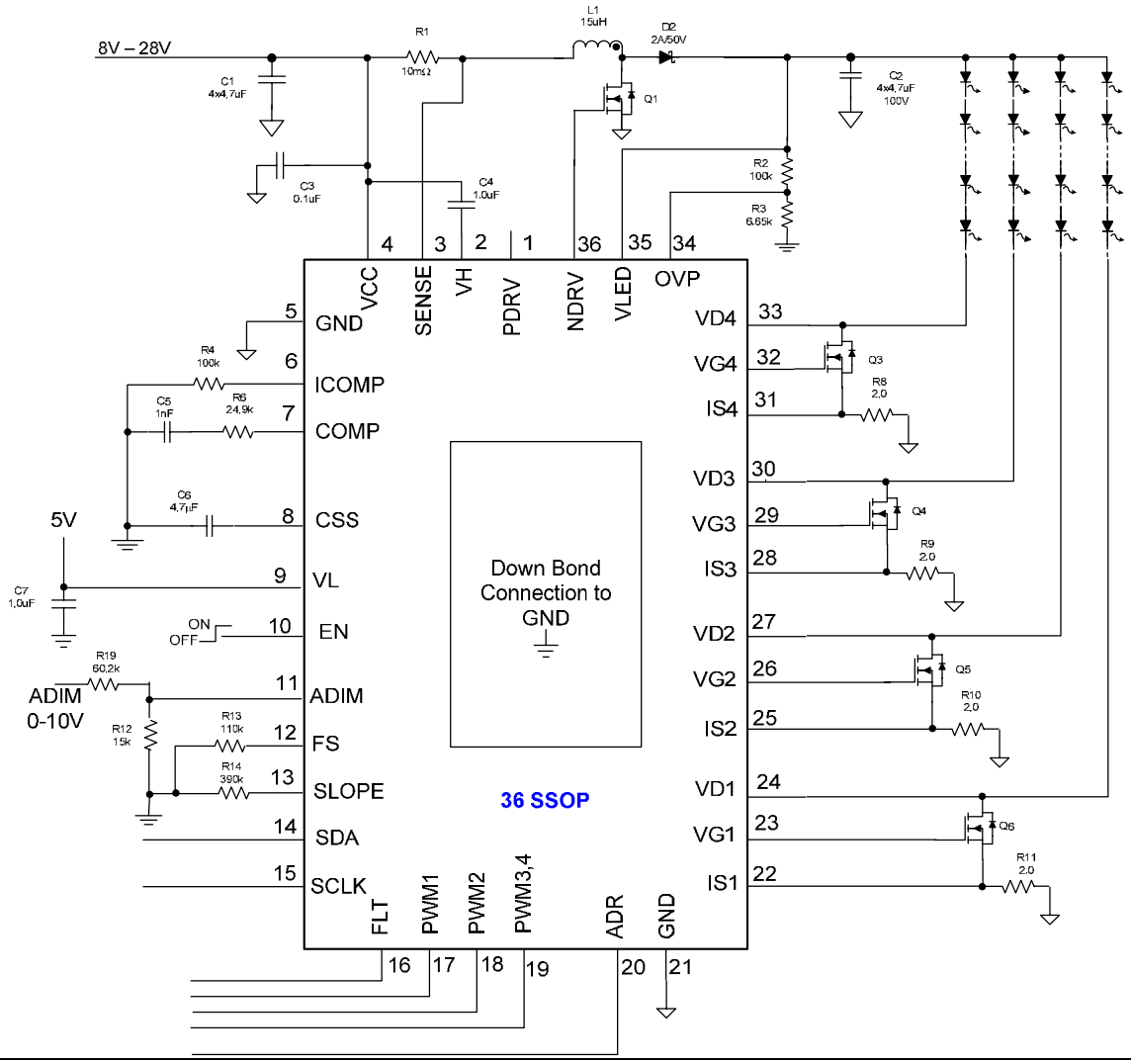
Microsemi
Analog Mixed Signal Group
One Enterprise, Aliso Viejo, CA 92656 USA, Within USA (800)713-4113, Outside USA (949)380-6100, Fax (949) 215-4996

Typical Application Circuit 2: Boost Mode Converter (Vin < Vo<60V)
With short circuit protection using external PFET



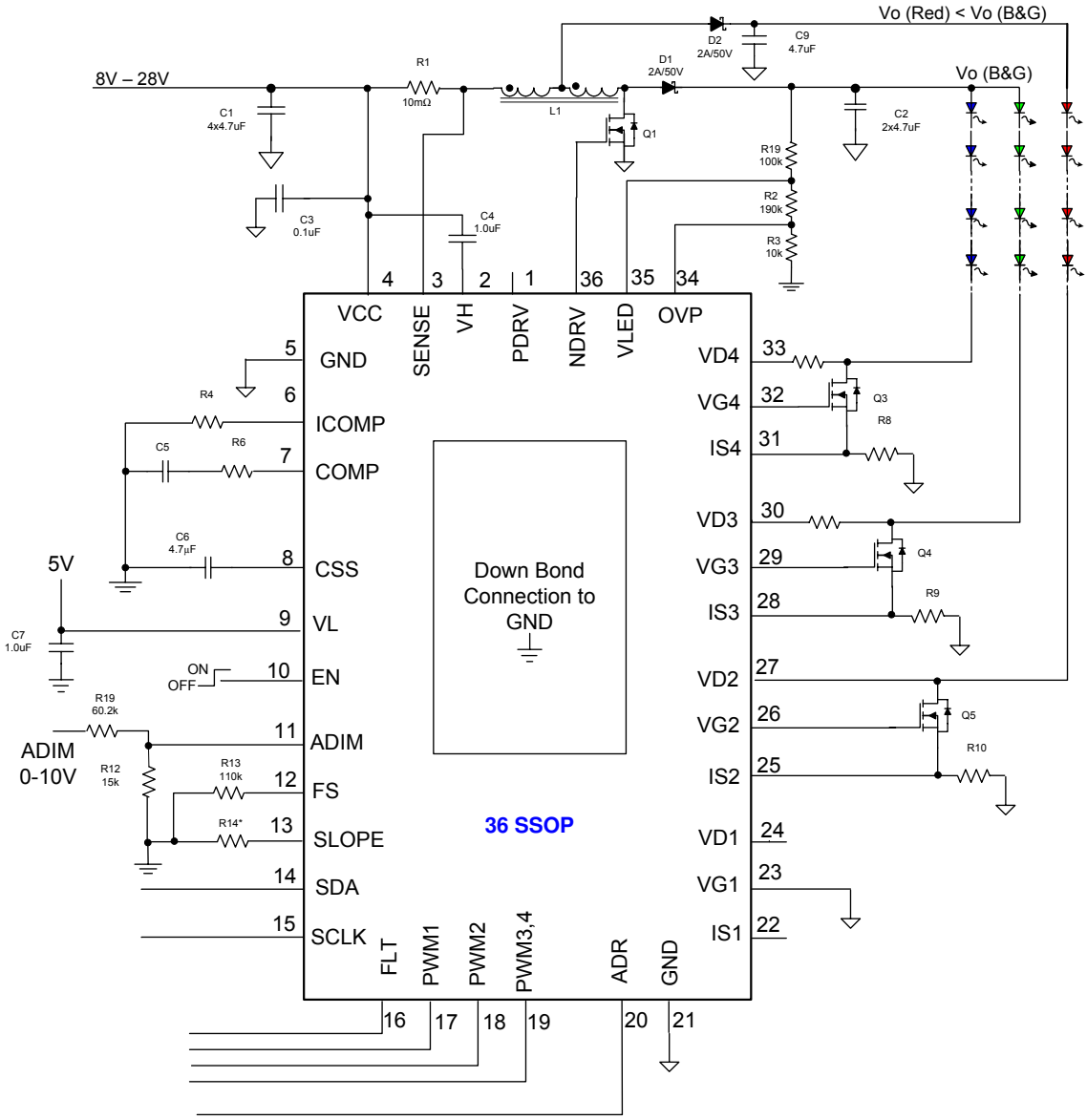
The component values are for reference only

Typical Application Circuit 3: Boost Mode Converter (Vin < Vo<35V)



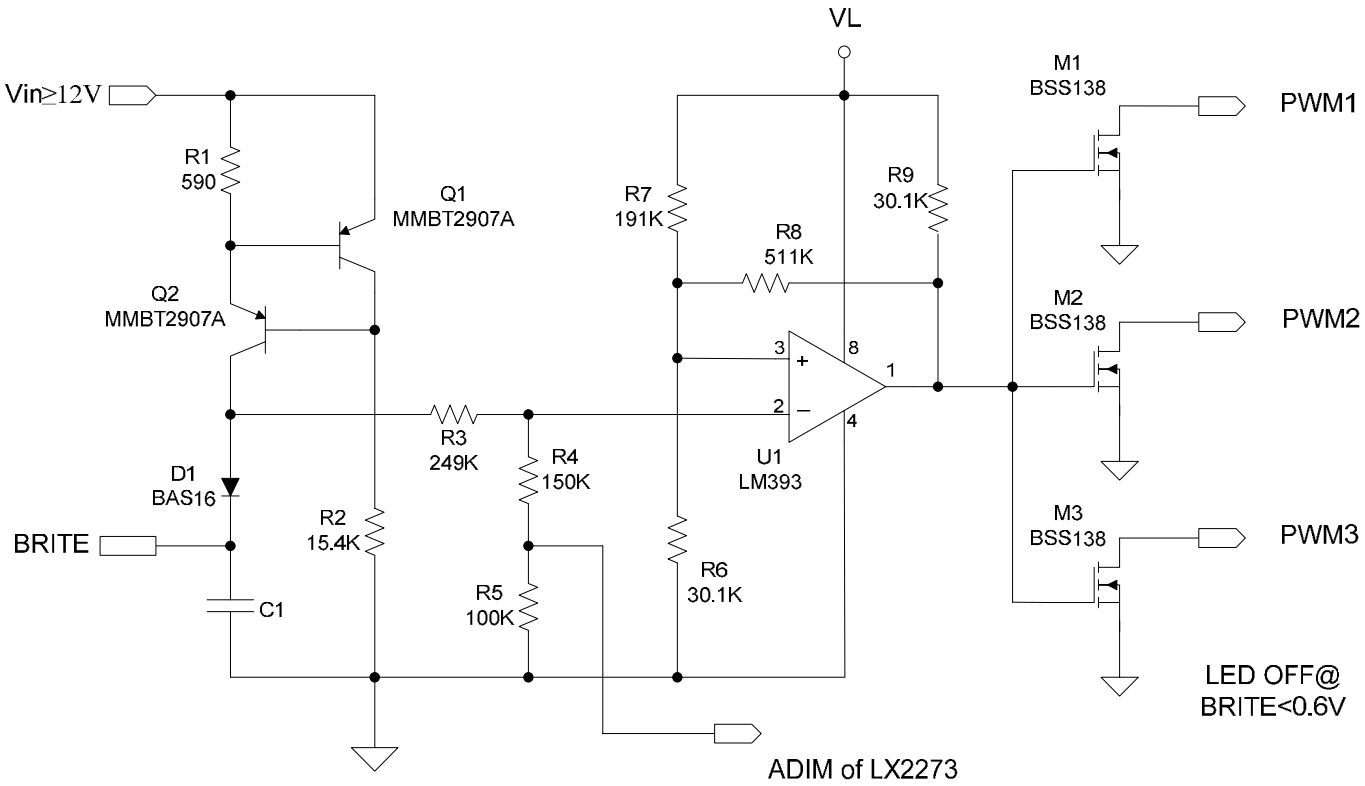
The component values are for reference only

Typical Application 4: Boost Mode Converter (Vin < Vo<60V) for RGB LEDs



The component values are for reference only.

Typical Application 5: SSL 0V to 10V Interface Circuit

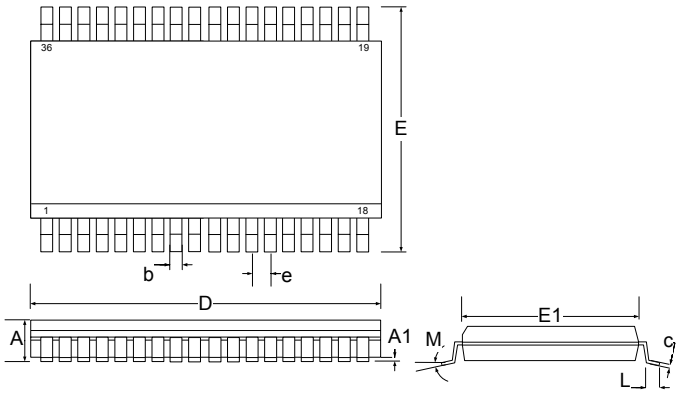


The component values are for reference only.

Typical application 4 provides a circuit to allow the LX2273 to be interfaced with a 0 to 10V SSL dimming control through the node labeled BRITE. Q1 and Q2 along with R1 sets up a current source to drive the dimmer over the 1V to 10V range providing the dimming control signal to the ADIM input of the LX2273. When the BRITE input is less than about 0.6V the comparator U1 will drive the PWMx inputs of the LX2273 low completely shutting of the LED string current.

PACKAGE DIMENSIONS

DB 36-Pin Plastic Quarter Size/Small Shrink Outline Package (SSOP/QSOP)



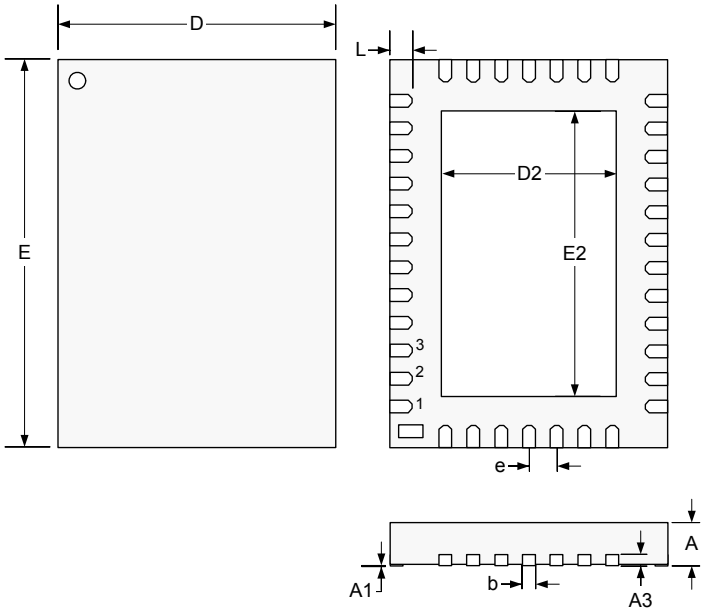
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.44	2.65	0.096	0.104
A1	0.10	0.30	0.004	0.012
b	0.25	0.51	0.010	0.020
c	0.20	0.33	0.009	0.013
D	15.20	15.60	0.598	0.614
E	10.05	10.55	0.396	0.415
E1	7.40	7.60	0.291	0.299
e	0.80 BSC		0.031 BSC	
L	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
*LC	–	0.10	–	0.004

*Lead Coplanarity

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage

PACKAGE DIMENSIONS

LQ 38-Pin Plastic QFN (5x7mm) Exposed Pad



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.011
D	5.00 BSC		0.196 BSC	
D2	3.00	3.25	0.118	0.127
E	7.00 BSC		0.275 BSC	
E2	5.00	5.25	0.196	0.206
e	0.50 BSC		0.019 BSC	
L	0.30	0.50	0.012	0.020

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage

NOTES