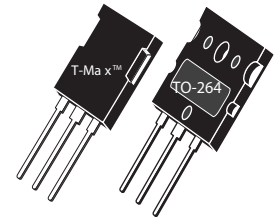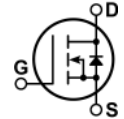## N-Channel FREDFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr}, soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent niose immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.

APT22F120B2   APT22F120L

Single die FREDFET

FEATURES

- **Fast switching with low EMI**
- **Low t_{rr} for high reliability**
- **Ultra low C_{rss} for improved noise immunity**
- **Low gate charge**
- **Avalanche energy rated**
- **RoHS compliant**

TYPICAL APPLICATIONS

- **ZVS phase shifted and other full full bridge**
- **Half bridge**
- **PFC and other boost converter**
- **Buck converter**
- **Single and two switch forward**
- **Flyback**

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ T_C = 25°C	23	A
	Continuous Drain Current @ T_C = 100°C	15	
I_{DM}	Pulsed Drain Current [1]	90	
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy [2]	1875	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	12	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ T_C = 25°C			1040	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.12	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	°C
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			6.2		g
Torque	Mounting Torque (TO-264 Package), 4-40 or M3 screw			10	in·lbf
				1.1	N·m

Static Characteristics $T_J = 25°C$ unless otherwise specified APT22F120B2_L

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V$, $I_D = 250\mu A$		1200			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, $I_D = 250\mu A$			1.41		V/°C
$R_{DS(on)}$	Drain-Source On Resistance③	$V_{GS} = 10V$, $I_D = 12A$			0.53	0.70	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 2.5mA$		2.5	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient				-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 1200V$	$T_J = 25°C$			250	μA
		$V_{GS} = 0V$	$T_J = 125°C$			1000	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm30V$				±100	nA

Dynamic Characteristics $T_J = 25°C$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	$V_{DS} = 50V$, $I_D = 12A$		27		S
C_{iss}	Input Capacitance	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1MHz$		8370		pF
C_{rss}	Reverse Transfer Capacitance			100		
C_{oss}	Output Capacitance			615		
$C_{o(cr)}$ ④	Effective Output Capacitance, Charge Related	$V_{GS} = 0V$, $V_{DS} = 0V$ to $800V$		240		
$C_{o(er)}$ ⑤	Effective Output Capacitance, Energy Related			125		
Q_g	Total Gate Charge	$V_{GS} = 0$ to $10V$, $I_D = 12A$, $V_{DS} = 600V$		260		nC
Q_{gs}	Gate-Source Charge			42		
Q_{gd}	Gate-Drain Charge			120		
$t_{d(on)}$	Turn-On Delay Time	**Resistive Switching** $V_{DD} = 800V$, $I_D = 12A$ $R_G = 2.2\Omega$⑥, $V_{GG} = 15V$		45		ns
t_r	Current Rise Time			27		
$t_{d(off)}$	Turn-Off Delay Time			145		
t_f	Current Fall Time			42		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)				23	A
I_{SM}	Pulsed Source Current (Body Diode)①					90	
V_{SD}	Diode Forward Voltage	$I_{SD} = 12A$, $T_J = 25°C$, $V_{GS} = 0V$				1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 12A$③ $di_{SD}/dt = 100A/\mu s$	$T_J = 25°C$		375	425	ns
			$T_J = 125°C$		720	850	
Q_{rr}	Reverse Recovery Charge		$T_J = 25°C$		2.2		μC
			$T_J = 125°C$		5.8		
I_{rrm}	Reverse Recovery Current		$T_J = 25°C$		12.3		A
			$T_J = 125°C$		16.5		
dv/dt	Peak Recovery dv/dt	$I_{SD} \le 12A$, di/dt $\le 1000A/\mu s$, $V_{DD} = 800V$, $T_J = 125°C$				25	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at $T_J = 25°C$, L = 26.04mH, $R_G = 25\Omega$, $I_{AS} = 12A$.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$. To calculate $C_{o(cr)}$ for any value of V_{DS} less than $V_{(BR)DSS}$, use this equation: $C_{o(er)} = -3.80E\text{-}7/V_{DS}{}^2 + 4.62E\text{-}8/V_{DS} + 6.57E\text{-}11$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.
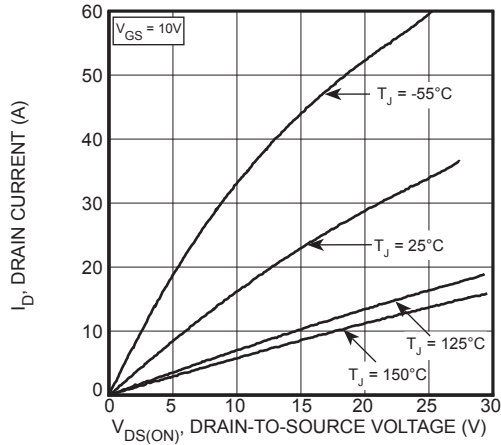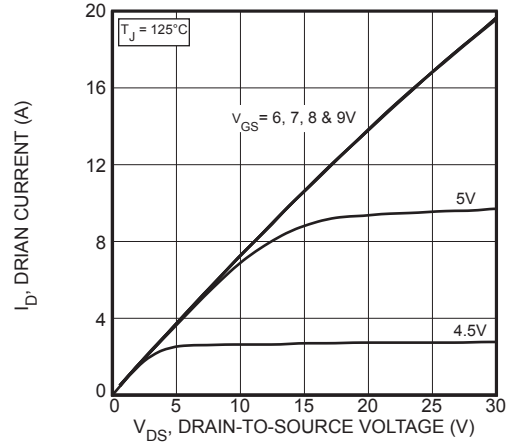
Figure 1, Output Characteristics
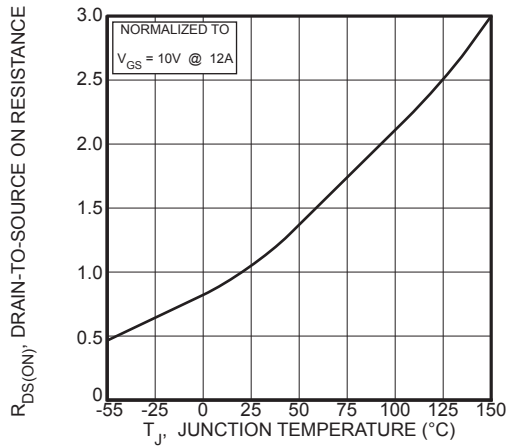

Figure 2, Output Characteristics

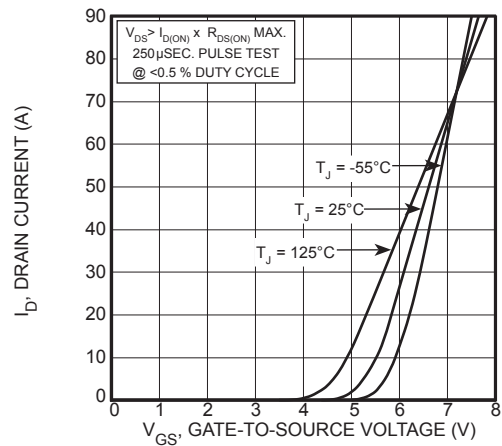Figure 3, R$_{DS(ON)}$ vs Junction Temperature
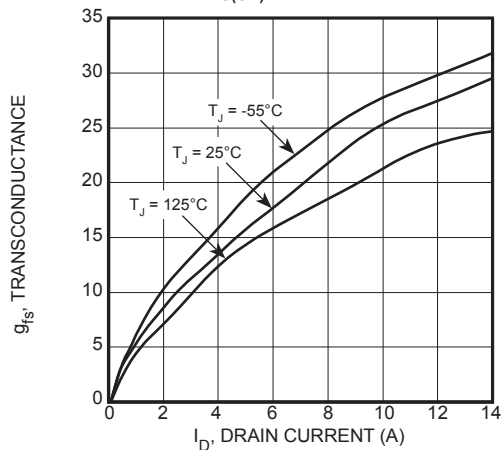

Figure 4, Transfer Characteristics
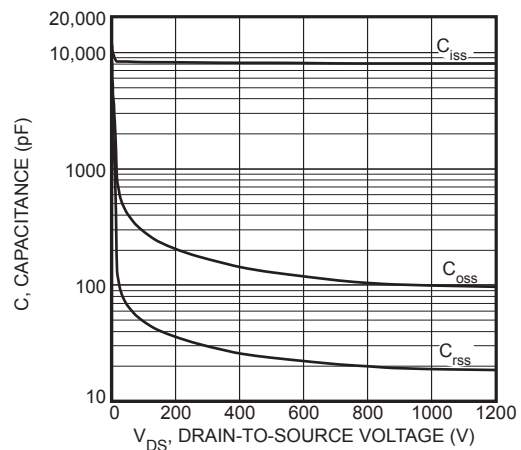

Figure 5, Gain vs Drain Current

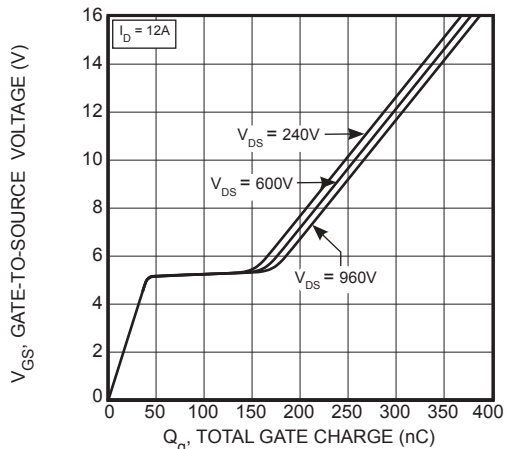Figure 6, Capacitance vs Drain-to-Source Voltage

Figure 7, Gate Charge vs Gate-to-Source Voltage

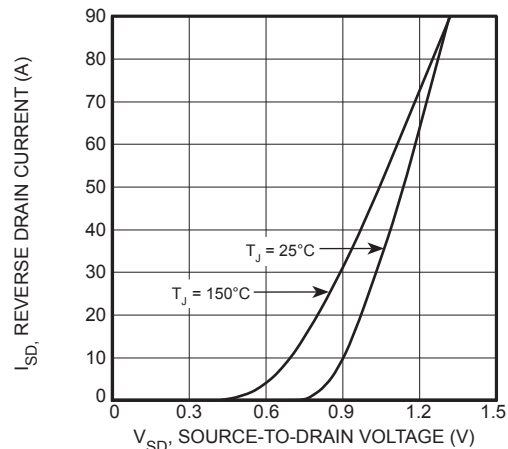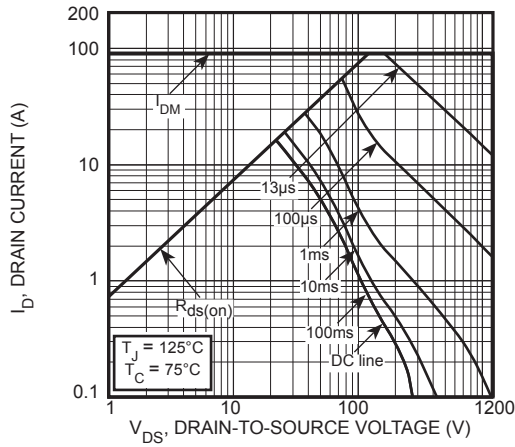Figure 8, Reverse Drain Current vs Source-to-Drain Voltage
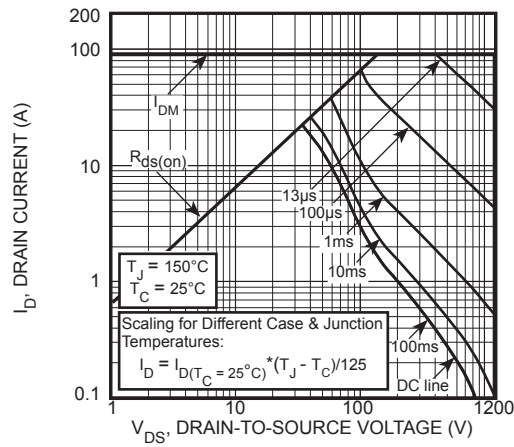
Figure 9, Forward Safe Operating Area

I_D, DRAIN CURRENT (A)

I_DM

R_ds(on)

13µs
100µs
1ms
10ms
100ms
DC line

$T_J = 125°C$
$T_C = 75°C$

V_DS, DRAIN-TO-SOURCE VOLTAGE (V)

Figure 10, Maximum Forward Safe Operating Area

I_D, DRAIN CURRENT (A)

I_DM

R_ds(on)

13µs
100µs
1ms
10ms
100ms
DC line

$T_J = 150°C$
$T_C = 25°C$

Scaling for Different Case & Junction Temperatures:

$$I_D = I_{D(T_C = 25°C)} * (T_J - T_C)/125$$

V_DS, DRAIN-TO-SOURCE VOLTAGE (V)

Z_θJC, THERMAL IMPEDANCE (°C/W)

D = 0.9
0.7
0.5
0.3
0.1
0.05

SINGLE PULSE

Note:

P_{DM}

t_1
t_2

t_1 = Pulse Duration

Duty Factor D = t_1/t_2

Peak $T_J = P_{DM} \times Z_{\theta JC} + T_C$

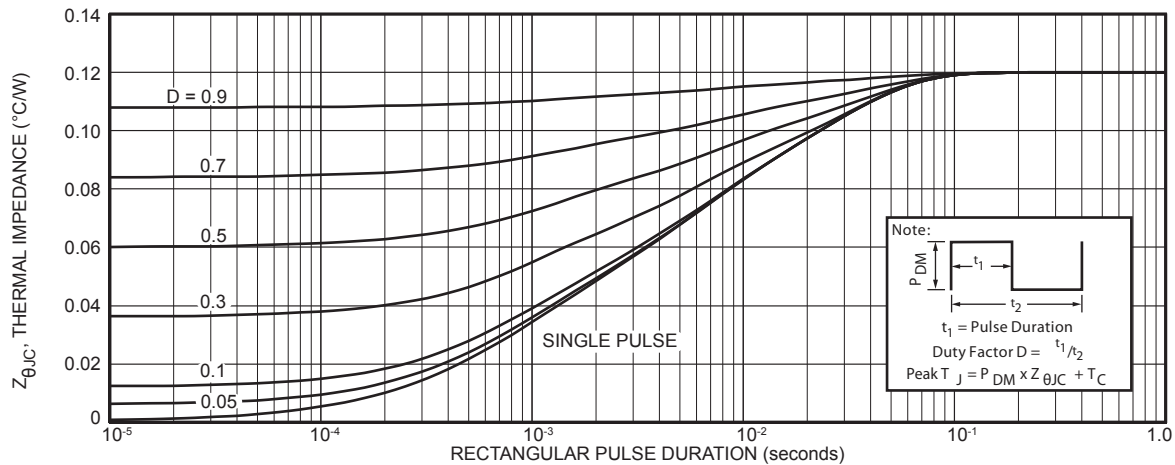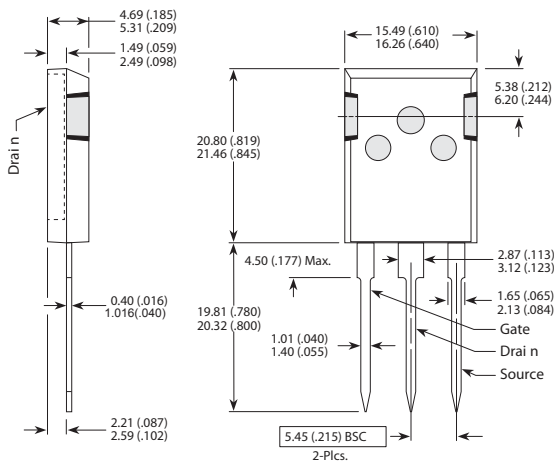RECTANGULAR PULSE DURATION (seconds)

Figure 11. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

T-MAX® (B2) Package Outline

TO-264 (L) Package Outline

e3 100% Sn Plated

Drain

4.69 (.185)
5.31 (.209)
1.49 (.059)
2.49 (.098)

15.49 (.610)
16.26 (.640)

5.38 (.212)
6.20 (.244)

20.80 (.819)
21.46 (.845)

4.50 (.177) Max.

2.87 (.113)
3.12 (.123)

1.65 (.065)
2.13 (.084)

0.40 (.016)
1.016 (.040)

19.81 (.780)
20.32 (.800)

1.01 (.040)
1.40 (.055)

Gate
Drain
Source

2.21 (.087)
2.59 (.102)

5.45 (.215) BSC
2-Plcs.

These dimensions are equal to the TO-247 without the mounting hole.
Dimensions in Millimeters and (Inches)

Drain

4.60 (.181)
5.21 (.205)
1.80 (.071)
2.01 (.079)

19.51 (.768)
20.50 (.807)

3.10 (.122)
3.48 (.137)

5.79 (.228)
6.20 (.244)

25.48 (1.003)
26.49 (1.043)

2.29 (.090)
2.69 (.106)

2.29 (.090)
2.69 (.106)

19.81 (.780)
21.39 (.842)

0.48 (.019)
0.84 (.033)
2.59 (.102)
3.00 (.118)

0.76 (.030)
1.30 (.051)
2.79 (.110)
3.18 (.125)

Gate
Drain
Source

5.45 (.215) BSC
2-Plcs.

Dimensions in Millimeters and (Inches)