Click here to ask an associate for production status of specific part numbers.

SMBUS Dual Channel High Dynamic Range Power Accumulator

MAX34427

General Description

The MAX34427 is a specialized current, voltage, and power monitor used to determine power consumption of systems. The device has a very wide dynamic range (20,000:1) that allows for the accurate measurement of power in such systems. The device is configured and monitored with a standard I²C/SMBus serial interface. The unidirectional current sensor offers precision high-side operation with a low full-scale sense voltage. The device automatically collects the current-sense and voltage samples and then multiplies those values to obtain a power value it then accumulates. Upon a command from the host, the device transfers the accumulated power samples, as well as the accumulation count, to a set of registers accessible by the host. This transfer occurs without missing a sample and allows the host to retrieve the data not only in real-time, but at any time interval.

Applications

- Tablets
- Ultra Notebooks
- Workstations
- Servers
- VR/AR Headsets

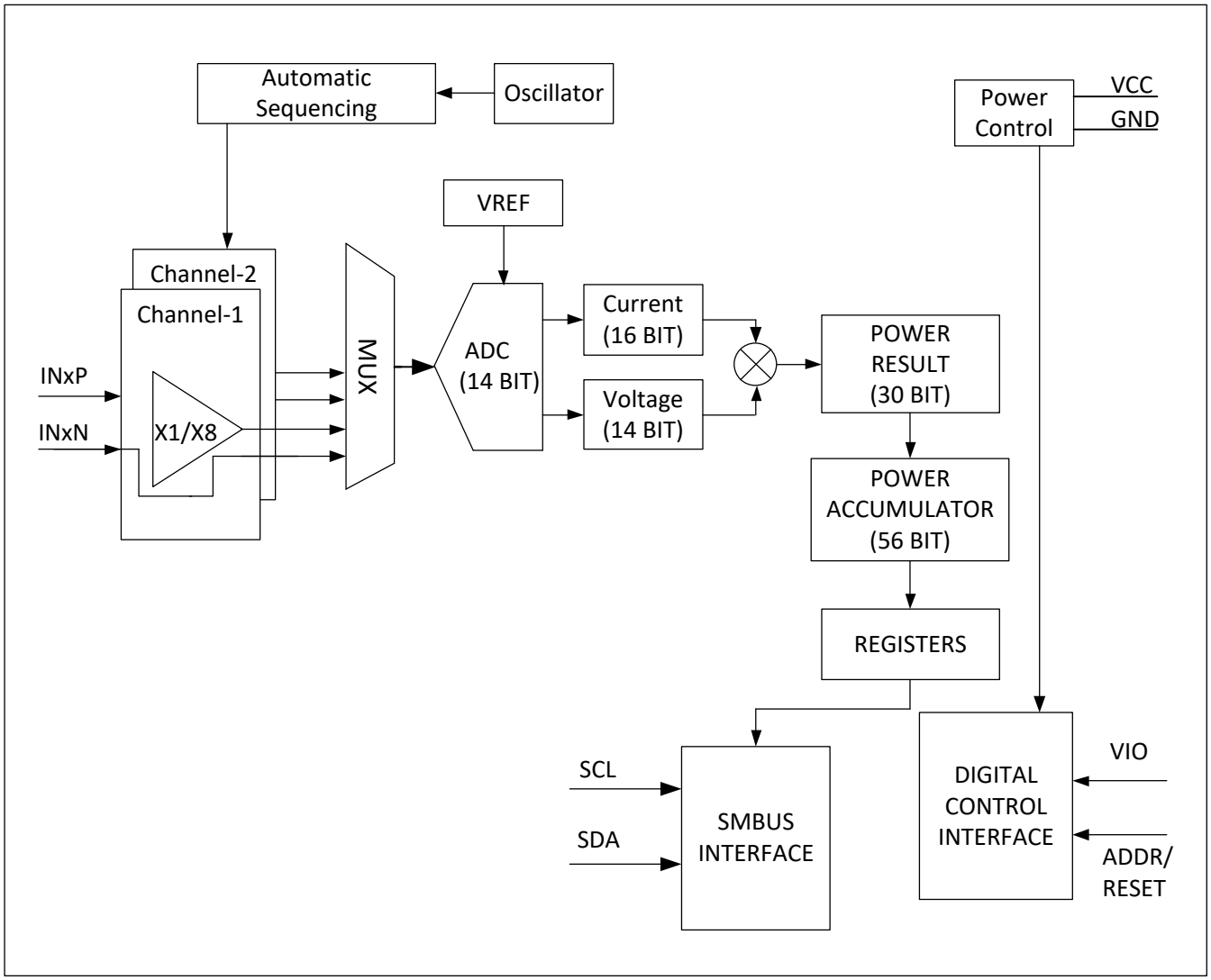
Benefits and Features

- Enables Code Optimization to Minimize Power Consumption
- Two Power Monitors with Wide 86dB Dynamic Range
- Measures Both Current and Voltage
- Ability to Measure Only Accumulated Current or Accumulated Power
- Reduced Power Consumption in Slow Accumulation Mode
- Power-Down Mode
- Minimizes Processor Overhead with Autonomous Operation
  - Per Channel 56-Bit Power Accumulators Capture 2.27 Hours of Data at 2048 Samples per Second
  - Per Channel 14-Bit Voltage Registers
- High-Integration Solution Minimizes Part Count, PCB Space, and BOM Cost
  - 5µV to 100mV Current-Sense Voltage with Current Common-Mode Range of 0.5V to 24V
  - 16 Programmable I²C Addresses
  - I²C/SMBus Interface with Bus Timeout
  - Temperature Range: -40°C to +85°C
  - Small, 2.24mm x 1.91mm Footprint WLP with 12 Bumps at 0.5mm Pitch and 3mm x 3mm Footprint TDFN 12-pin package
- Ease of Development
  - Evaluation Kit with Advanced GUI

***Ordering Information* appears at end of data sheet.**

19-101544; Rev 0; 5/22

Simplified Block Diagram



Absolute Maximum Ratings

IN+ and IN- to GND ..... -0.3V to 28V
Differential Input Voltage, IN+ to IN- ..... ±0.5V
VDD or VIO to GND ..... -0.3V to 4V
SDA or SCL to GND ..... -0.3V to 4V
ADDR/RESET Pin ..... -0.3V to VDD + 0.3 (not to exceed +4) V

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Temperature See the IPC/JEDEC J-STD-020A Specification °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 WLP

Package Code	121C2+1
Outline Number	*21-0009*
Land Pattern Number	See *Application note 1891*
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	N/A
Junction-to-Case Thermal Resistance (θ_{JC})	N/A
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	62°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

12 TDFN

Package Code	TD1233+1C
Outline Number	21-0664
Land Pattern Number	90-0397
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	63°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages . Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial .

Electrical Characteristics

(V_{DD} = 3.3V, V_{IO} = 3.3V, Normal Mode (SLOW bit not set, CAM bit not set, Power-Up Default Values of CONTROL Register (0x01) and RATE Register (0x20)), T_A = +25°C Unless Otherwise Noted. = Limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_{DD} Operating Range			2.7		3.6	V
V_{DD} Average Supply Current (*Note 1*, *Note 5*)	IDD	Per channel Sample rate = 2048 samples/s		740		µA
V_{DD} Average Supply Current (*Note 1*)	IDD	SLOW bit is set		4		µA
		PDNB bit is set		1.5		µA
V_{IO} Operating Range			1.6		3.6	V
V_{IO} Average Supply Current	IIO			0.1		µA
SENSE INPUT/OUTPUT						
Minimum Input Common-Mode Voltage				0.5		V
Maximum Input Common-Mode Voltage				24		V
IN+ Input Bias Current				1		µA
IN- Average Input Bias Current (*Note 2*)		SLOW bit is set or PDNB bit is set		1		µA
				5		
DYNAMIC CHARACTERISTICS						
Per Channel Current and Power Sample Rate				1875		SPS
Per Channel Current and Power Sample Rate		CAM bit is set		3468		SPS
		SLOW bit is set		2		
Power and Current Measurement Accumulation Accuracy (1 Sigma Error Range with > 5000 Accumulations) (*Note 3*, *Note 4*)		V_{SENSE} = 5µV		±25		%
Input Bandwidth				400		kHz
Power-Up Time		Measured from V_{DD} > 2.6V and V_{IO} > 1.5V to SMBus port active		2		ms
ACCURACY						
Current Sample Resolution		V_{SENSE} < 12.5mV		16		bits
		V_{SENSE} > 12.5mV		13		
Voltage Sample Resolution				14		bits
Current-Sense Full Scale Voltage				100		mV
Voltage-Sense Full Scale				24		V
Power and Current Measurement		V_{SENSE} = 95mV		±0.8		%
		V_{SENSE} = 10mV		±1		

(V_{DD} = 3.3V, V_{IO} = 3.3V, Normal Mode (SLOW bit not set, CAM bit not set, Power-Up Default Values of CONTROL Register (0x01) and RATE Register (0x20)), T_A = +25°C Unless Otherwise Noted. = Limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Accumulation Accuracy (1 Sigma Error Range with > 1000 Accumulations) (*Note 3*, *Note 4*)		V_{SENSE} = 1mV		±1.5		
		V_{SENSE} = 100µV		±2.2		
		V_{SENSE} = 50µV		±3.5		
LOGIC INPUT/OUTPUT						
Input Logic-High (SCL/SDA)	V_{IH}		0.75 x V_{IO}			V
Input Logic-High (RESET)	V_{IH}		0.6 x V_{DD}			V
Input Logic-Low (SCL/SDA)	V_{IL}				0.3 x V_{IO}	V
Input Logic-Low (RESET)	V_{IL}				0.2 x V_{lave}	V
SDA Output Logic-Low	V_{OL}	IOL = 4mA			0.4	V
SCL, SDA Leakage					±5	µA
I^2C/SMBUS INTERFACE (V_{IO} = 3.3V)						
SCL Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		500			ns
Hold Time (Repeated) START Condition	$t_{HD:STA}$		260			ns
Low Period of SCL	t_{LOW}		500			ns
High Period of SCL			260			ns
Data Hold Time			0			ns
			0		150	
Data Setup Time			50			ns
Start Setup Time			260			ns
SDA and SCL Rise Time					120	ns
SDA and SCL Fall Time			3		120	ns
Stop Setup Time			260			ns
Noise Spike Reject				25		ns

Note 1: SMBus not active.

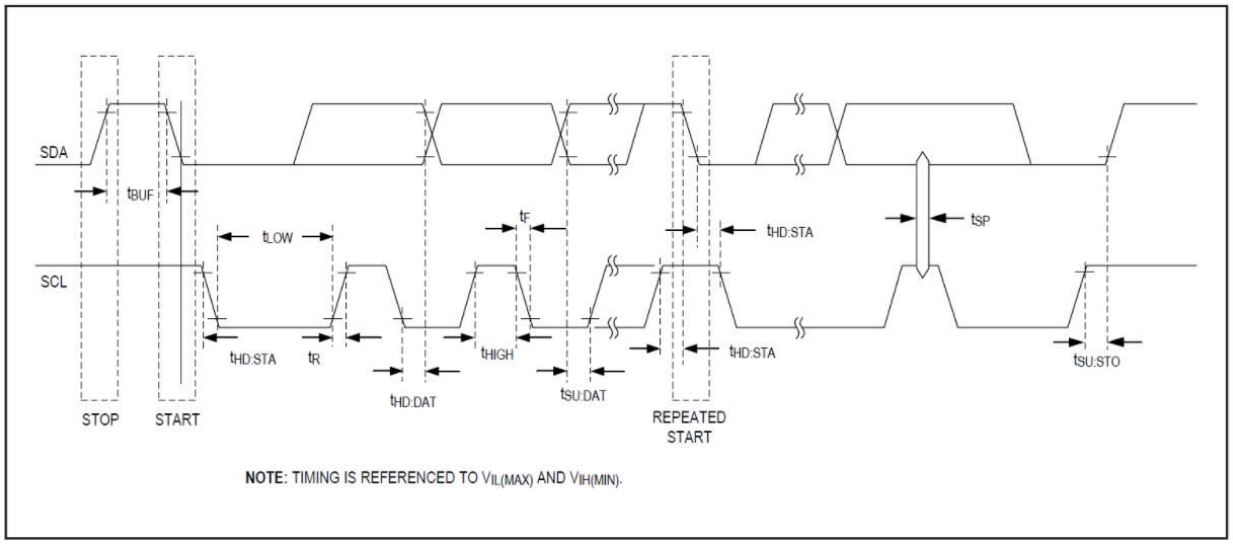
Note 2: Input bias current varies with VSENSE (IN+ - IN-) voltage.

Note 3: Estimated from characterization, not production tested.

Note 4: Includes gain error, offset error, and quantization error.

Note 5: VDD average supply current at sampling rate 1024 samples/sec is 356µA. This current consumption is half of the MAX34417's supply current. The MAX34417's sampling rate is 1024 samples/s.

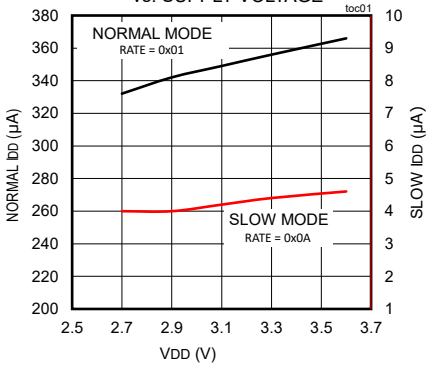
Timing Diagrams



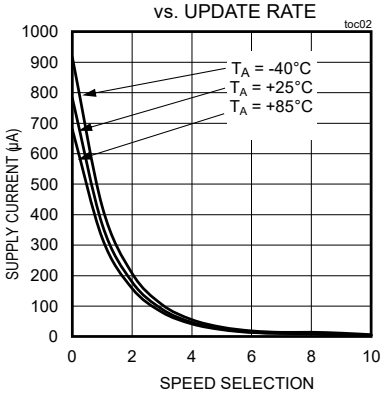
Typical Operating Characteristics

V_{DD} = V_{IO} = 3.3V, T_A = +25°C, V_{CM} = 3.8V, V_{SENSE} = 1mV.

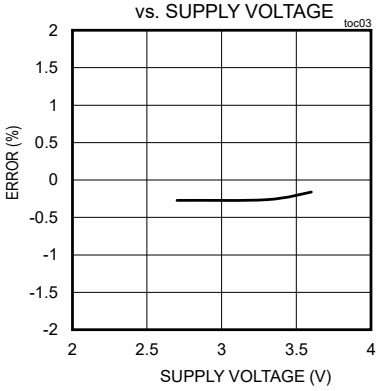
SUPPLY CURRENT vs. SUPPLY VOLTAGE



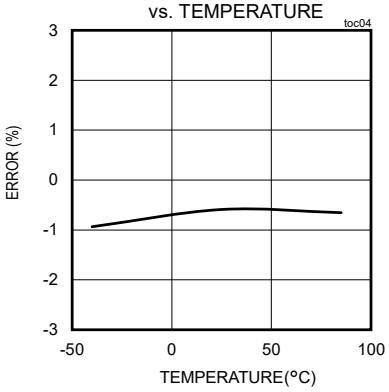
VDD SUPPLY CURRENT vs. UPDATE RATE



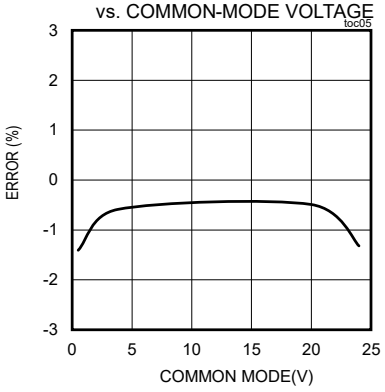
POWER MEASUREMENT ERROR vs. SUPPLY VOLTAGE



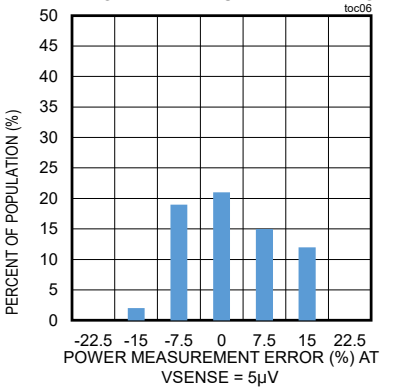
POWER MEASUREMENT ERROR vs. TEMPERATURE



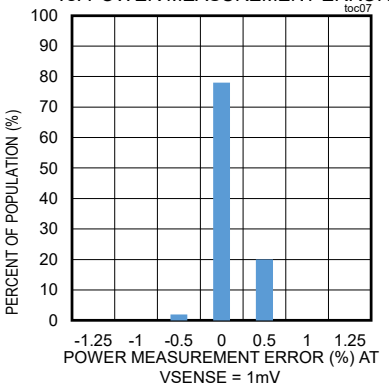
POWER MEASUREMENT ERROR vs. COMMON-MODE VOLTAGE



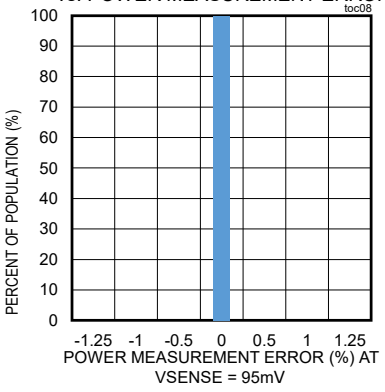
PERCENT OF POPULATION vs. POWER MEASUREMENT ERROR



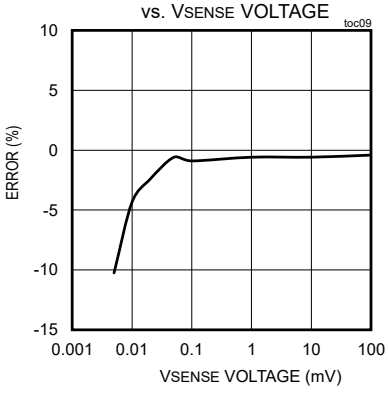
PERCENT OF POPULATION vs. POWER MEASUREMENT ERROR



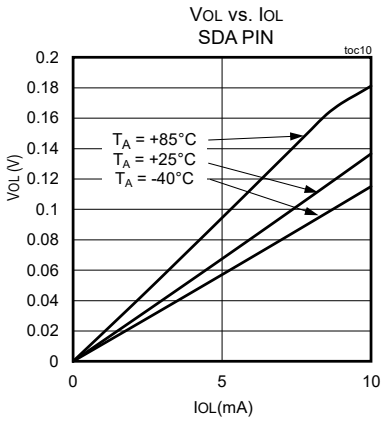
PERCENT OF POPULATION vs. POWER MEASUREMENT ERROR



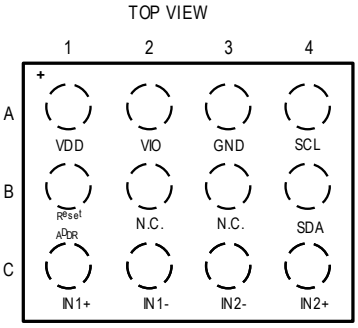
POWER MEASUREMENT ERROR vs. VSENSE VOLTAGE



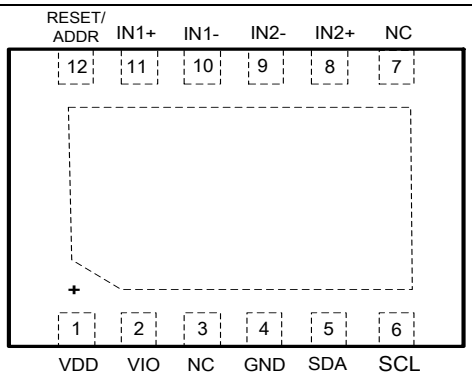
V_{DD} = V_{IO} = 3.3V, T_A = +25°C, V_{CM} = 3.8V, V_{SENSE} = 1mV.



Pin Configurations



12 WLP



12-TDFN

Pin Descriptions

PIN		NAME	FUNCTION
WLP	TDFN		
11	C1	IN1+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 1. Voltages can be applied to these pins in the absence of power being applied to VDD or VIO. Unused current-sense inputs should be tied together.
10	C2	IN1-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 1. Voltages can be applied to these pins in the absence of power being applied to VDD or VIO. Unused current-sense inputs should be tied together.
8	C4	IN2+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 2. Voltages can be applied to these pins in the absence of power being applied to VDD or VIO. Unused current-sense inputs should be tied together.
9	C3	IN2-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 2. Voltages can be applied to these pins in the absence of power being applied to VDD or VIO. Unused current-sense inputs should be tied together.
4	A3	GND	Ground
3	B2	NC	No Connect
7	B3		
1	A1	VDD	Supply Voltage for Current-Sense Amplifiers. +2.7V to +3.6V supply. This pin should be decoupled to GND by 0.1uF capacitor.
2	A2	VIO	Supply Voltage for Digital Interface. +1.6V to +3.6V supply. This pin should be decoupled to GND with 100nF capacitor. Power can be applied to VDD either before or after or in absence of VIO.
12	B1	RESET/ADDR	I^2C/SMBus-Compatible Address Select Input. A resistor tied to GND from this pin selects the SMBus target address during power up of IC. See the *Target Address Setting* section for more details. After power-up, a low to high pulse on this pin resets IC.
6	A4	SCL	I^2C/SMBus-Compatible Clock Input. SCL does not load the SMBus when either VDD or VIO is not present.
5	B4	SDA	I^2C/SMBus-Compatible Data Input/Output. SDA does not load the SMBus when either VDD or VIO is not present
13		EP	Connect Expose Pad to GND

Detailed Description

The MAX34427 automatically sequences through the channels to collect samples from the common-mode voltage and the current-sense amplifiers. The 16-bit current value and the 14-bit voltage value are then multiplied to create a 30-bit power value that is then written to the power accumulator. The MAX34427 contains a 56-bit power accumulator for each channel. This accumulator is updated at a programmable rate between 4 to 4096 times per second. When the host is ready to pull the latest accumulation data, it first sends the update command. This update command cross loads the accumulation count and accumulation data of both channels into the registers that the host can read at any time. This type of operation allows the host to control the accumulation period. The only constraint is that the host should access the data before the accumulators can overflow. If the accumulators overflow, they do not roll over. The MAX34427 contains a 14-bit ADC for voltage and a 13-bit ADC for current. During each sample time, a 14-bit voltage sample and a 16-bit current sample are resolved. To create a 16-bit current value from the 13-bit ADC, the device takes two current samples: one with the current sense amplifier in a high-gain mode and another with the amplifier in a low-gain mode. The high gain setting is eight times the low-gain setting. Based on the two current-sense ADC results, the device determines which result provides the best accuracy and fills the 16-bit current sample accordingly.

SMBus Operation

The MAX34427 uses the SMBus command/response format as described in the System Management Bus Specification Version 2.0. The structure of the data flow between the host and the target is shown as follows for several different types of transactions. Data is sent MSB first. The fixed target address of the MAX34427 is determined on device power-up by sampling the resistor tied to the ADDR pin. See the *Target Address Setting* section for details. On device power-up, the device defaults to the control command code (01h). If the host attempts to read the device with an invalid command code, all ones (FFh) are returned in the data byte.

Table 1. Read Byte Format

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Target Address	W	A	Command Code	A	SR	Target Address	R	A	Data Byte	NA	P

Table 2. Write Byte Format

1	7	1	1	8	1	8	1	1
S	Target Address	W	A	Command Code	A	Data Byte	A	P

Table 3. Send Byte Format

1	7	1	1	8	1	1
S	Target Address	W	A	Command Code	A	P

Table 4. Block Read Format

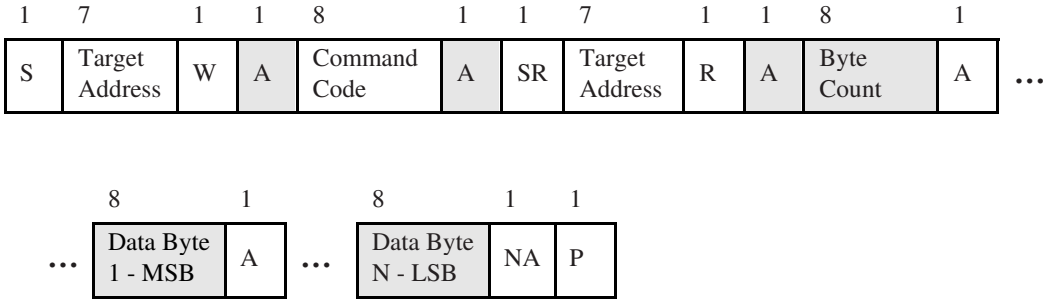
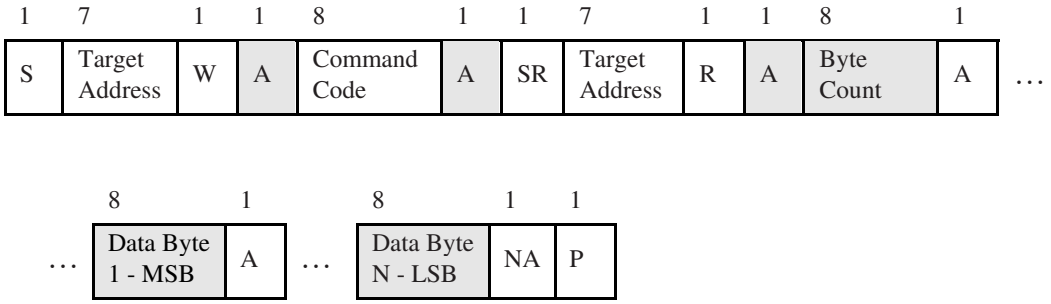


Table 5. Bulk Read Format



Note: in multi-byte reads, the Most Significant Byte is the first data byte read.

Key:
S = Start
SR = Repeated-Start
P = Stop
W = Write-Bit(0)
R = Read-Bit(1)
A = Acknowledge(0)
NA = Not-Acknowledge(1)
Shaded-Block = Target-Transaction

Target Address Setting

The MAX34427 responds to receiving its fixed target address by asserting an ACK on the bus. The fixed target address of the MAX34427 is determined on device power up by sampling the voltage across a resistor tied to the ADDR pin after VDD rises to a valid value. See *Table 6* for more details. The device does not respond to a general call address. It is activated only when receiving its fixed target address or the broadcasting address, 2Ch, for Global Update. Upon sending "00" to target address 2Ch, all MAX34427 ICs that connect to the I2C are updated.

On power up or after a reset sequence, a current of 640µA is applied to the RADDR and the voltage is measured. The binary slicing value is compared to the ADC result. An ADC value that is below the slicing value but not below the adjacent lower slicing value selects the 7-bit Target-Address. For resistance values greater than 1960Ω, ADC result is obtained using 20µA current. The selected values tolerate a total error of ±15% in the measurement to account for errors in the current value and resistor value. E96 1% resistor is recommended.

Table 6. SMBUS Target Address Select

Mode	7 BIT I2C ADDRESS (Hex)	E96 1% RESISTOR VALUE (Ω)
16	0x36	118000
15	0x34	61900
14	0x32	43200
13	0x30	30100
12	0x26	20000
11	0x24	12700
10	0x22	7150
9	0x20	3240
8	0x1E	1960
7	0x1C	1370
6	0x1A	931
5	0x18	619
4	0x16	392
3	0x14	226
2	0x12	105
1	0x10	0

Command Codes

Table 7. Command Codes

COMMAND CODE	NAME	DETAILED DESCRIPTION	TYPE	NO OF BYTES	POR
00h	UPDATE	Request Accumulator Update	Send Byte	0	-
01h	CONTROL	Device Configuration and Status	R/W Byte	1	00h
02h	ACC_CNT	Accumulator Counter	Block Read	3	*Note 7*
03h	PWR_ACC_1	Power or Current Accumulator for Channel 1	Block Read	7	*Note 7*, *Note 12*
04h	PWR_ACC_2	Power or Current Accumulator for Channel 2	Block Read	7	*Note 7*, *Note 12*
07h	VOLT_CH1	Voltage for Channel 1	Block Read	2	*Note 7*
08h	VOLT_CH2	Voltage for Channel 2	Block Read	2	*Note 7*
0Fh	DID	Device ID and Revision	Read Byte	1	*Note 8*
00h	BULK_UPDATE	Target address = 2Ch followed by command code = 00H	Send Byte	0	*Note 9*
10h	BULK_POWER	Read all accumulators in bulk mode starting with channel 1	Bulk Read	28	*Note 10*
11h	BULK_VOLTAGE	Read all voltages in bulk mode starting with channel 1	Bulk Read	8	*Note 7*
20h	RATE	Sampling Rate Selection	R/W Byte	1	*Note 7*
21h	PWRDN	Power Down Mode Control	Write Byte	1	*Note 7* and *Note 11*

Note 6: Power-On Reset (POR) is the default value when power is applied to the device.

Note 7: These registers are set to all zeros upon POR.

Note 8: The Device ID is factory set and varies based on the die revision.

Note 9: Target Address 2Ch is a broadcast address for Global Update to all MAX34427.

Note 10: 28 bytes if Control[7] = 1, else, 24

Note 11: To exit Power Down, reset sequence should be executed.

Note 12: Bit 7 in Control register determines power or current accumulation.

Command Code Bit Description

Update (00h) – Send Byte

The update send byte command does not contain any data. The UPDATE command must be sent to the device before reading any of the other commands, and it must be sent after writing to the CONTROL command. After sending the UPDATE command, the host should wait at least 1ms before reading any command. Each time the device receives this command, it completes an accumulation cycle for the active channels (if not already complete) and then it transfers all of the accumulation data in the power accumulators and the accumulator counter to a set of registers that can be read with the SMBus interface. This command resets all of the counters/accumulation registers. An update command does not clear the OVF bit.

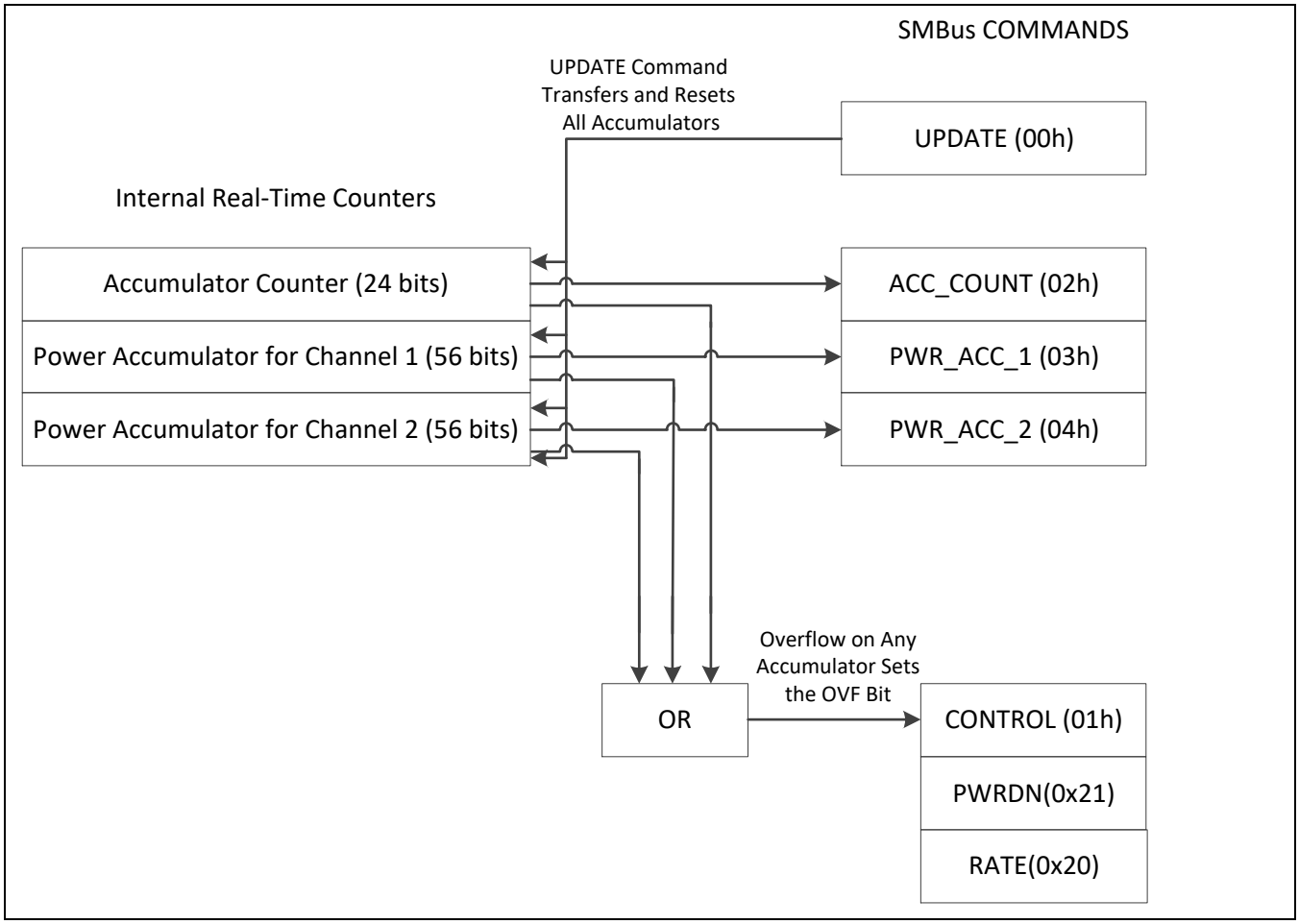


Figure 1. MAX34417 SMBus Register Structure

CONTROL (0x01)

BIT	7	6	5	4	3	2	1	0
Field	MODE	CAM	SMM	PARK_EN	PARK[1:0]		SLOW	OVF
Reset	**0x0**	**0x0**	**0x0**	**0x0**	**0x0**		**0x0**	**0x0**
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7	When this bit is at 0, current accumulation is enabled. 16-bit current value is accumulated over time and can be readout in 56-bit wide power accumulator registers. When this bit is set to 1, the power accumulation gets enabled. The accumulators are 56-bit wide and the power readout is a 30-bit value.	0 = Enable Current Accumulation 1 = Enable Power Accumulation
CAM	6	Continuous Accumulate Mode. When this bit is set, the inputs are measured and accumulated continuously without idle periods. After setting this bit, an UPDATE command must be issued to start the accumulation cycles. The subsequent UPDATE command moves the data to the SMBus registers, resets the accumulators, and starts the continuous accumulation cycle process. SMM and CAM modes should not be enabled at the same time. Note that changing any Control byte settings while CAM bit is enabled is disallowed. If CAM mode must be set, the Control byte must be set to desired values with CAM = 0, then followed by an UPDATE. After this, the CAM mode bit can be set and another UPDATE must be sent	0 = CAM mode not active 1 = CAM Mode enabled
SMM	5	Single Measure Mode. When this bit is set, the device performs two measure and accumulation cycles for the active channels (normal scan mode) or four samples of one channel in Park mode in response to an UPDATE command. The data can be read by issuing another UPDATE command which moves the previous UPDATE data into the SMBus read registers and starts another measurement cycle. Data should be read between UPDATE commands. UPDATE commands should be no less than 1ms apart for reliable measurements. The power accumulators remain at 56-bits even though the single calculated power is a 30-bit value. After the SMM bit is changed, the UPDATE command should be sent to reset the accumulators and perform the selected scan operation. SMM and CAM modes should not be enabled at the same time.	0 = Normal scan and accumulate operation. 1 = SMM Mode enabled
PARK_EN	4	This bit enables the channel park feature. If this bit is set, only one channel is enabled and the device samples the selected channel two times faster than the normal round-robin rate. The channel to monitor is selected with the PARK bit. After the PARK_EN bit is changed, the UPDATE command should be sent to clear out the accumulators and start a new accumulation period. When the channel park feature is enabled, the minimum time before the power accumulators can overflow is reduced by a factor of two since the selected channel is being updated two times faster. Also, the power accumulators for the disabled channels do not contain any meaningful data.	0 = Round Robin Sampling of Two Channels. 1 = One Channel Selected (with the PARK0/1 bits)

BITFIELD	BITS	DESCRIPTION	DECODE
PARK	3:2	If the PARK_EN (Park Enable) bit is set, then these bits select which channel is to be monitored at the exclusion of the other channels	0x0: Channel 1 enabled 0x1: Channel 2 enabled 0x2: Reserved 0x3: Reserved
SLOW	1	If this bit is set, then the power accumulation calculation rate is slowed in order to lower the power consumption of the device. See the Rate register for further details.	0x0: Normal Mode 0x1:Slow Mode
OVF	0	This status bit is set to a one if any of the power accumulators or the accumulator counter reach overflow. When the accumulators or counter overflow, they do not rollover. Any active sequencing or accumulation mode stops and the device halts in the idle state. A UPDATE command clears the accumulators and the accumulation counter, thus clearing the overflow condition, as well as resuming the selected accumulation mode sequence. The OVF bit in the control register is not cleared by an UPDATE command. This status bit must be cleared by writing a 0.	

ACC_CNT (0x02)

BIT	23	22	21	20	19	18	17	16
Field	CNT23:16							
Reset	0							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	CNT15:8							
Reset	0							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	CNT7:0							
Reset	0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CNT	23:0	These bits report the number of accumulations since the last UPDATE command. The UPDATE command copies the count into this SMBus data register. By dividing the total accumulated power reported in each power accumulator by this count, the average power can be determined. The accumulator counter does not roll over.

PWR_ACC_1 (0x03)

This same register is used for current accumulation as well. Bit 7 in Control register determines power or current accumulation.

BIT	55	54	53	52	51	50	49	48
Field	PWR_CH1[55:48]							
Reset	0							
Access Type	Read Only							
BIT	47	46	45	44	43	42	41	40
Field	PWR_CH1[47:40]							
Reset	0							
Access Type	Read Only							
BIT	39	38	37	36	35	34	33	32
Field	PWR_CH1[39:32]							
Reset	0							
Access Type	Read Only							
BIT	31	30	29	28	27	26	25	24
Field	PWR_CH1[31:24]							
Reset	0							
Access Type	Read Only							
BIT	23	22	21	20	19	18	17	16
Field	PWR_CH1[23:16]							

Reset	0							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	PWR_CH1[15:8]							
Reset	0							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	PWR_CH1[7:0]							
Reset	0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PWR_CH1	55:0	Power accumulation for Channel 1. These bits report the total power accumulated by channel 1. The UPDATE command moves the data in the accumulators into these registers in the SMBus logic from where they are read. The power accumulators do not rollover. This is an unsigned, binary number.

PWR_ACC_2 (0x04)

This same register is used for current accumulation as well. Bit 7 in the Control register determines power or current accumulation.

BIT	55	54	53	52	51	50	49	48
Field	PWR_CH2[55:48]							
Reset	0							
Access Type	Read Only							
BIT	47	46	45	44	43	42	41	40
Field	PWR_CH2[47:40]							
Reset	0							

Access Type	Read Only							
BIT	39	38	37	36	35	34	33	32
Field	PWR_CH2[39:32]							
Reset	0							
Access Type	Read Only							
BIT	31	30	29	28	27	26	25	24
Field	PWR_CH2[31:24]							
Reset	0							
Access Type	Read Only							
BIT	23	22	21	20	19	18	17	16
Field	PWR_CH2[23:16]							
Reset	0							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	PWR_CH2[15:8]							
Reset	0							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	PWR_CH2[7:0]							
Reset	0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PWR_CH2	55:0	Power Accumulation for Channel 2. These bits report the total power accumulated by each Channel 2. The UPDATE command moves the data in the accumulators into these registers in the SMBus logic from where they are read. The power accumulators do not rollover. This is an unsigned, binary number.

VOLT_CH1 (0x07)

BIT	15	14	13	12	11	10	9	8
Field	VOLT_CH1[13:6]							
Reset	0							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	VOLT_CH1[5:0]						0	0
Reset	0							
Access Type	Read Only						Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
VOLT_CH1	15:2	These bits report the voltage on the IN- pin of channel 1 at the approximate time of the last UPDATE command. It is a single sample and is not accumulated over time. It is an unsigned, binary value. The 14-bit value is in bits 15:2.

VOLT_CH2 (0x08)

BIT	15	14	13	12	11	10	9	8
Field	VOLT_CH2[13:6]							
Reset	0							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	VOLT_CH2[5:0]						0	0

Reset	0	0x0	0x0
Access Type	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
VOLT_CH2	15:2	These bits report the voltage on the IN- pin of channel 2 at the approximate time of the last UPDATE command. It is a single sample and is not accumulated over time. It is an unsigned, binary value. The 14-bit value is in bits 15:2

DID (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	ID[4:0]					DIE_REV[2:0]		
Reset	0x09							
Access Type	Read Only					Read Only		

BITFIELD	BITS	DESCRIPTION
ID	7:3	These bits report the device identification (ID). The ID is fixed at 09h.
DIE_REV	2:0	These bits report the device revision. The device revision is factory set.

RATE (0x20)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CONV_RATE[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CONV_RATE	3:0	Sets the ADC conversion rate. Decode table shows the raw number of ADC samples per second. This number is divided by two if both channels are active. Setting Slow bit in control register is equivalent to setting CONV_Rate to 0xA.	0x0: 4096 sps 0x1: 2048 sps 0x2: 1024 sps 0x3: 512 sps 0x4: 256 sps 0x5: 128 sps 0x6: 64 sps 0x7: 32 sps

BITFIELD	BITS	DESCRIPTION	DECODE
			0x8: 16 sps 0x9: 8 sps 0xA: 4 sps 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

PWRDN (0x21)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PDN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write 1 to set

BITFIELD	BITS	DESCRIPTION
PDN	0	Write 1 to power down the part, suspending all conversions and placing the part in its lowest power state. To exit power down, issue a reset sequence as described in Reset sequence.

BULK UPDATE (00H)

When sending 00 to target address 2Ch, all devices on the SMbus are updated.

BULK POWER READOUT (10H)

Read accumulated power data for both channels. Returned data is 28 bytes packet with 7bytes for each channel with channel 1 MSB first and channel 2 LSB last, total 14 bytes. Ignore last 14 bytes as they are returned 0.

BULK VOLTAGE READOUT (11H)

Read all voltage data for both channels. Returned data is 8 bytes packet with 2 bytes each for each channel with channel 1 MSB first and channel 2 LSB last, total 4 bytes. Ignore last 4 bytes as they are returned 0.

Reset Sequence

The MAX34427 features a system RESET functionality, which can be asserted at the ADDR/RESET pin during its normal operation. On the RESET condition, the MAX34427 performs a complete power up and a new post power-up sequence is executed to sense the ADDR resistor again and to determine the new SMbus target address.

After the initial powerup, the ADDR/RESET multiplexed pin acts as a digital input pin for RESET. The RESET can be asserted by using both the RESET pin and a request in the SMBus module by using SCL and SDA (START and STOP detection). As shown in *Figure 2*, the following sequence asserts RESET in MAX34427:

1. Pulling RESET pin from low to high before a START condition of SMBus, triggers a RESET sequence. The “setup” and “hold” time to hold Reset “high” is around 40µs as shown in *Figure 2*. It ensures the correct sampling of Reset pin’s “high” state. Before forcing the “high” state, make sure to leave RESET pin free by defaulting the controller I/O drive on the pin to “high impedance”.
2. Finally, RESET gets asserted when RESET pin is again pulled to “low” from “high” before a STOP condition of SMBus. Step 2 should happen within 1.280ms after performing Step 1.

If the RESET pin is high during a STOP condition, then the RESET is not asserted and the host needs to restart the process (from Step 1) to trigger the RESET.

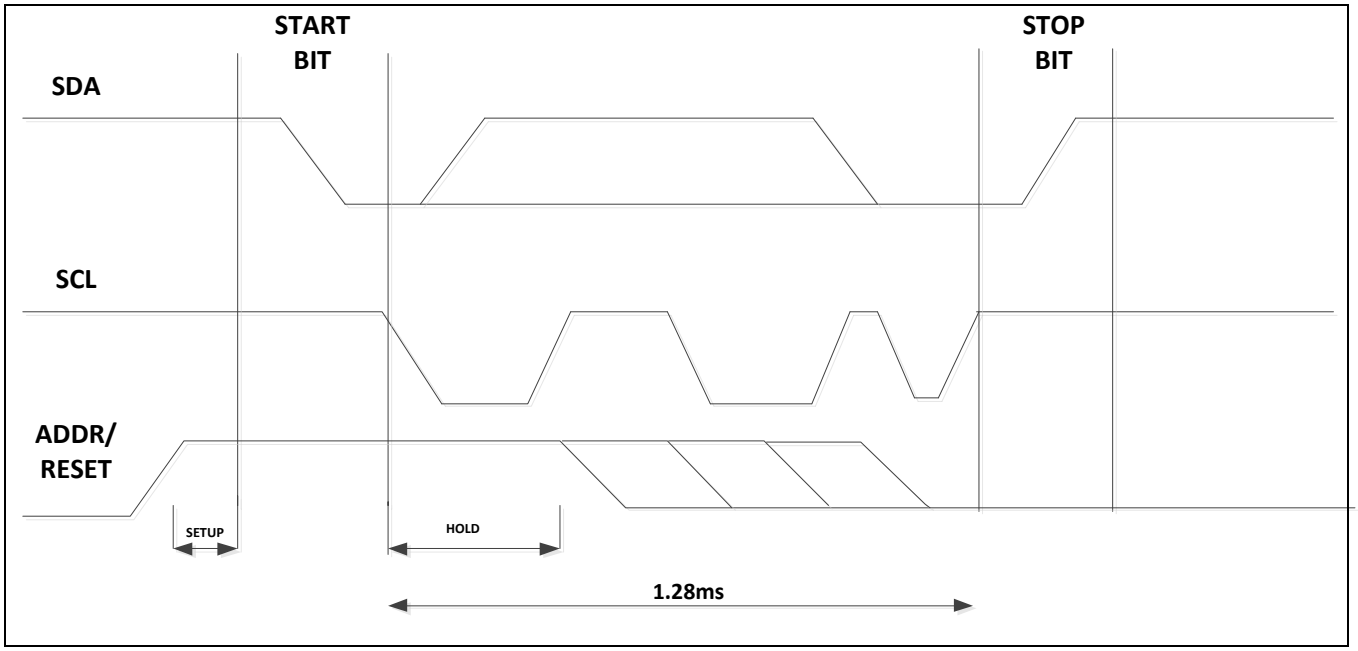


Figure 2. Reset Assert and Deassert Timing Sequence

Applications Information

Average Power and Current Calculation Example

AVERAGE POWER CALCULATION EXAMPLE

The average power can be derived in an external calculation using the steps as follows if the current sense resistor value is known, where: Power accumulator (56 bit) = 000001CEFBD314h, (7767577364 decimal), Accumulator counter (24 bit) = 0005DEh, and (1502 decimal), and Current-sense resistor = 10mΩ.

1. Calculate the unscaled average power by dividing the power accumulator value with the accumulator count value: 000001CEFBD314h/0005DEh = 4EE921h (5171489 decimal)
2. Calculate the ratio of the Step 1 result to the calculated power full-scale value which is a 30-bit value: $5171489/2^{30}$ = 0.004816324
3. Multiply the result from Step 2 by the correction factor listed in *Table 8* that matches the current-sense resistor value: 0.004816324 x 240 = 1.156W

Table 8. Power Correction Factors for Various Current-Sense Resistor Values

CURRENT-SENSE RESISTOR VALUE (mΩ)	FULL-SCALECURRENT(A	FULL-SCALEVOLTAGE(V)	POWER SCALE CORRECTION CALCULATION	POWER SCALE CORRECTION FACTOR (W)
100	1	24	1 x 24	24
50	2	24	2 x 24	48
40	2.5	24	2.5 x 24	60
25	4	24	4 x 24	96
20	5	24	5 x 24	120
15	6.6667	24	6.6667 x 24	160
10	10	24	10 x 24	240
5	20	24	20 x 24	480
4	25	24	25 x 24	600
2	50	24	50 x 24	1200
1	100	24	100 x 24	2400

AVERAGE CURRENT CALCULATION EXAMPLE

The average power can be derived in an external calculation using the steps as follows if the current sense resistor value is known, where: Current accumulator (56 bit) = 00000000FBD314h (16503572 decimal), Accumulator counter (24 bit) = 0005DEh (1502 decimal), and Current-sense resistor = 10mΩ.

4. Calculate the unscaled average current by dividing the power accumulator value with the accumulator count value: 00000000FBD314h/0005DEh = 2AEBh (10987 decimal)
5. Calculate the ratio of the Step 1 result to the calculated current full-scale value which is a 16-bit value: $10987/2^{16}$ = 0.1676
6. Multiply the result from Step 2 by the correction factor listed in *Table 9* that matches the current-sense resistor value: 0.1676 x 1 = 0.1676A

Table 9. Current Correction Factors for Various Current-Sense Resistor Values

CURRENT-SENSE RESISTOR VALUE (mΩ)	FULL-SCALE CURRENT(A)	CURRENT SCALE CORRECTION FACTOR (W)
100	1	1
50	2	2
40	2.5	2.5
25	4	4
20	5	5
15	6.6667	6.6667
10	10	10
5	20	20
4	25	25
2	50	50
1	100	100

Kelvin Sense

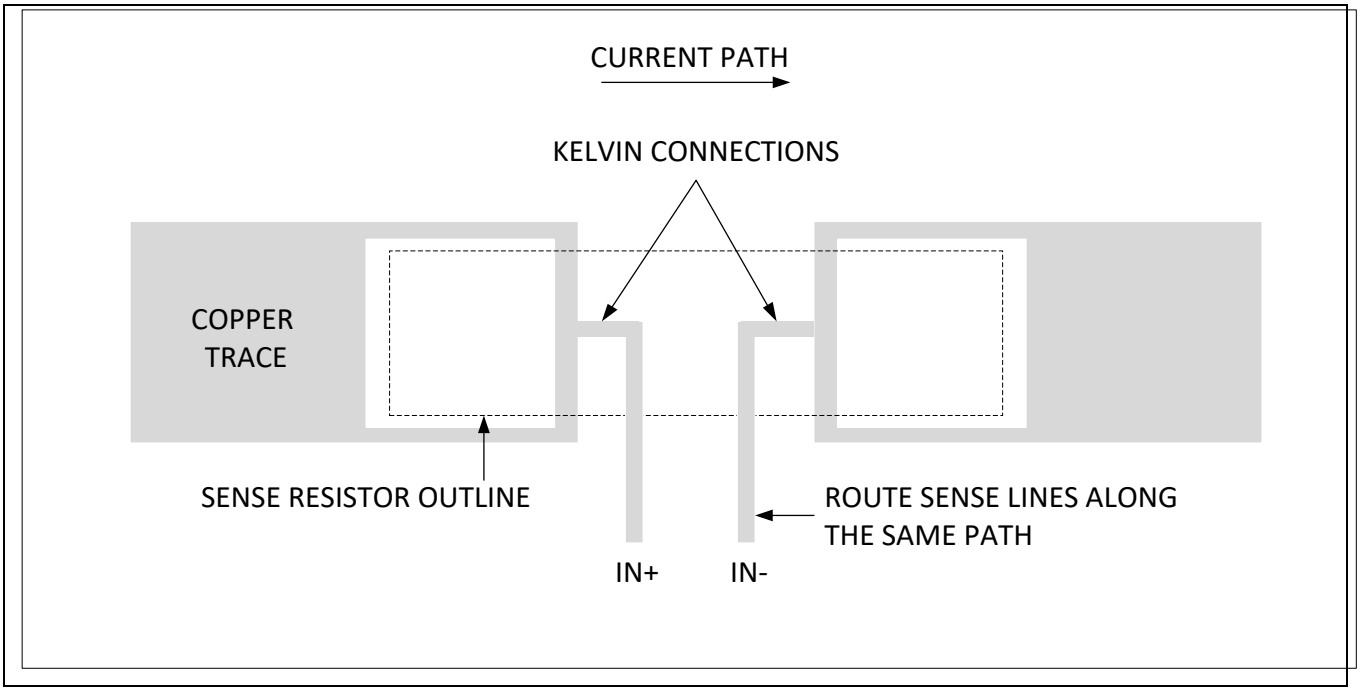


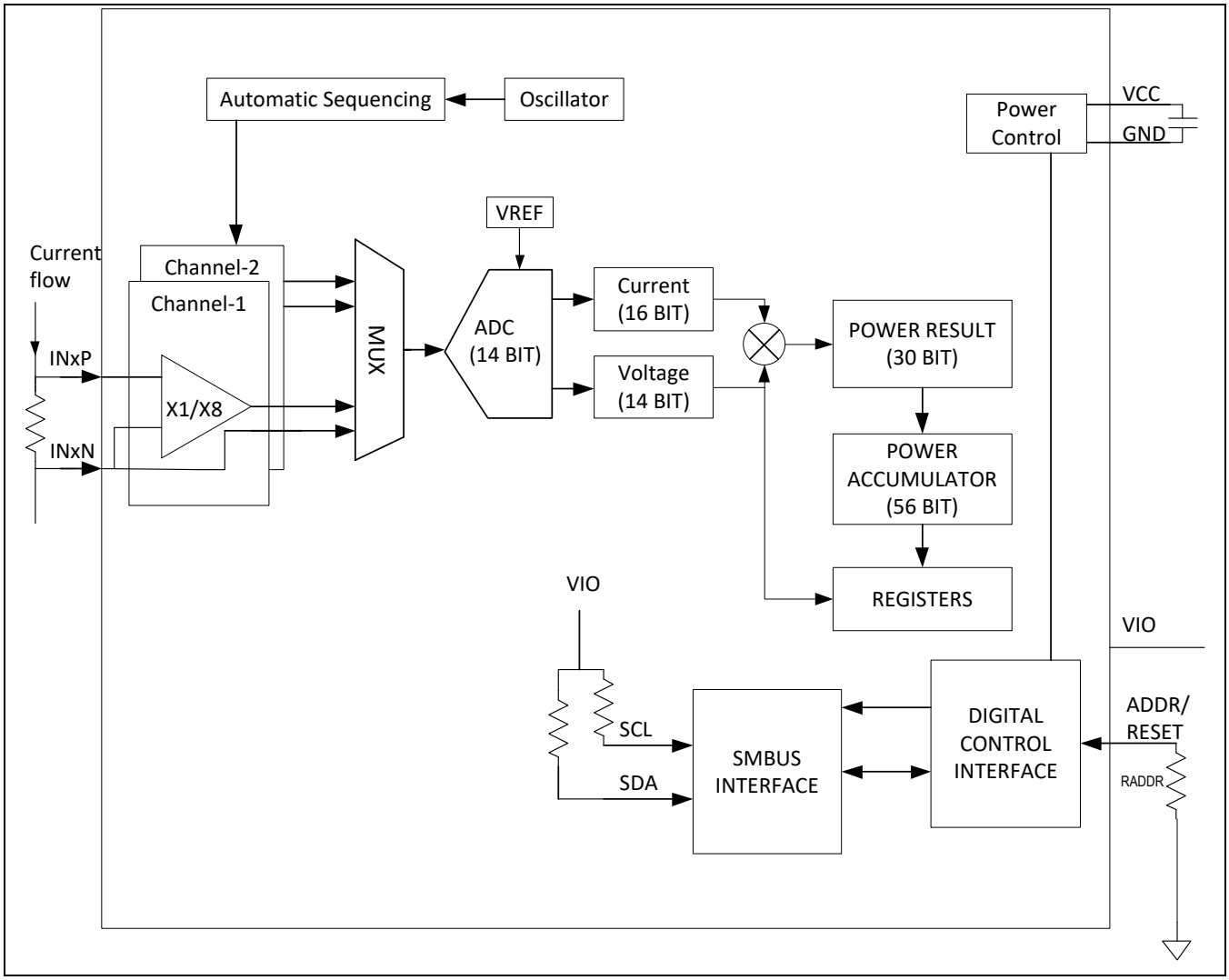
Figure 3. Kelvin Sense Connection Layout Example

For best performance, a Kelvin sense arrangement is recommended (see *Figure 3*). In a Kelvin sense arrangement, the voltage-sensing nodes across the sense element are placed so that they measure the true voltage drop across the sense element and not any additional excess voltage drop that can occur in the copper PCB traces or the solder mounting of the sense element. Routing the differential sense lines along the same path to the MAX34427 and keeping the path short also improve the system performance.

Minimizing Trace Resistance

PCB trace resistance from the sense resistor (RSENSE) to the IN- inputs can affect the MAX34427 power measurement accuracy. Every 1Ω of PCB trace resistance in the IN- path adds about 25μV of offset error. It is recommended to place the sense resistors as close as possible to the MAX34427 and not to use minimum width PCB traces. When placing an RC filter at the input, the resistor must be placed in the IN+ input path to reduce DC errors from the trace resistance.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX34427EWC+T	-40°C to +85°C	12WLP
MAX34427ETC+T*	-40°C to +85°C	12TDFN

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/22	Release for Market Intro	—