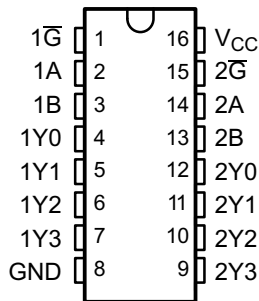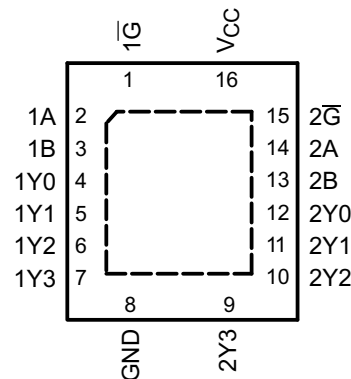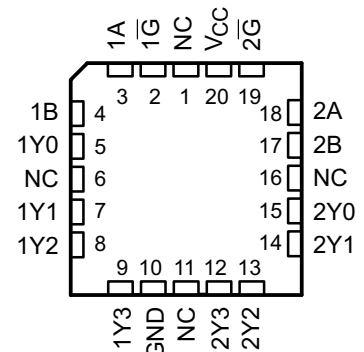# DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

Check for Samples: SN74AHC139, SN54AHC139

FEATURES

- **Operating Range 2-V to 5.5-V**
- **Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54AHC139 . . . J or W PACKAGE
SN74AHC139 . . . D,DB,DGV,N,NS
OR PW PACKAGE
(TOP VIEW)

1$\overline{G}$	1	16	V$_{CC}$
1A	2	15	2$\overline{G}$
1B	3	14	2A
1Y0	4	13	2B
1Y1	5	12	2Y0
1Y2	6	11	2Y1
1Y3	7	10	2Y2
GND	8	9	2Y3

SN74AHC139 . . . RGY PACKAGE
(TOP VIEW)

Top: 1$\overline{G}$ (1), V$_{CC}$ (16)

1A	2	15	2$\overline{G}$
1B	3	14	2A
1Y0	4	13	2B
1Y1	5	12	2Y0
1Y2	6	11	2Y1
1Y3	7	10	2Y2

Bottom: GND (8), 2Y3 (9)

SN54AHC139 . . . FKP ACKAGE
(TOP VIEW)

Top: 1A, 1$\overline{G}$, NC, V$_{CC}$, 2$\overline{G}$ (pins 3 2 1 20 19)

1B	4	18	2A
1Y0	5	17	2B
NC	6	16	NC
1Y1	7	15	2Y0
1Y2	8	14	2Y1

Bottom: 1Y3, GND, NC, 2Y3, 2Y2 (pins 9 10 11 12 13)

NC − No internal connection

DESCRIPTION

The 'AHC139 devices are dual 2-line to 4-line decoders/demultiplexers designed for 2-V to 5.5-V V$_{CC}$ operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.
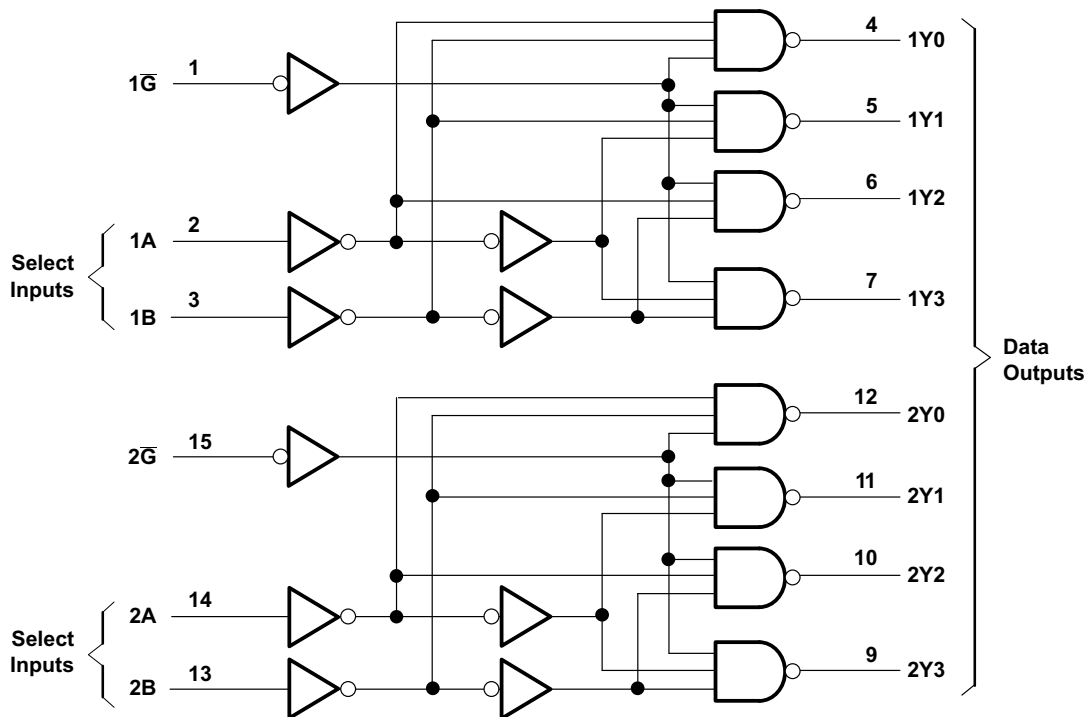
FUNCTION TABLE
(EACH GATE)

INPUTS			OUTPUT			
$\overline{G}$	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)

Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUE	UNIT
Supply voltage range, V_{CC}		−0.5 to 7	V
Input voltage range, V_I[2]		−0.5 to 7	V
Output voltage range, V_O[2]		−0.5 to V_{CC} + 0.5	V
Input clamp current, I_{IK} (V_I < 0)		−20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})		±20	mA
Continuous output current, I_O (V_O = 0 to V_{CC})		±25	mA
Continuous current through V_{CC} or GND		±75	mA
Package thermal impedance, θ_{JA}	D package[3]	73	°C/W
	DB package[3]	82	
	DGV package[3]	120	
	N package[3]	67	
	NS package[3]	64	
	PW package[3]	108	
	RGY package[4]	39	
Storage temperature range, T_{stg}		−65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) The package thermal impedance is calculated in accordance with JESD 51-5

Product Folder Links: *SN74AHC139 SN54AHC139*

RECOMMENDED OPERATING CONDITIONS[(1)]

			SN54AHC139		SN74AHC139		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC}= 2 V	1.5		1.5		V
		V_{CC}= 3V	2.1		2.1		
		V_{CC}= 5.5 V	3.85		3.85		
V_{IL}	Low-level Input voltage	V_{CC}= 2 V		0.5		0.5	V
		V_{CC}= 3 V		0.9		0.9	
		V_{CC}= 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC}= 2 V		−50		−50	mA
		V_{CC}= 3.3 V ± 0.3 V		−4		−4	
		V_{CC}= 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC}= 2 V		50		50	mA
		V_{CC}= 3.3 V ± 0.3 V		4		4	
		V_{CC}= 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	V_{CC}= 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC}= 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C SN54AHC139		T_A = −40°C TO 85°C SN74AHC139		T_A = −40°C TO 125°C Recommended SN74AHC139		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	2 V	1.9	2		1.9		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		2.48		
	I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	I_{OH} = 4 mA	3 V			0.36		0.5		0.44		0.5	
	I_{OH} = 8 mA	4.5 V			0.36		0.5		0.44		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1[(1)]		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
						SN54AHC139		SN74AHC139		Recommended SN74AHC139		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF	7.2[1]	11[1]	1[1]	13[1]	1	13	1	13	ns
t_{PHL}				7.2[1]	11[1]	1[1]	13[1]	1	13	1	13	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF	6.4[1]	9.2[1]	1[1]	11[1]	1	11	1	11	ns
t_{PHL}				6.4[1]	9.2[1]	1[1]	11[1]	1	11	1	11	
t_{PLH}	A or B	Y	C_L = 50 pF	9.7	14.5	1	16.5	1	16.5	1	16.5	ns
t_{PHL}				9.7	14.5	1	16.5	1	16.5	1	16.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF	8.9	12.7	1	14.5	1	14.5	1	14.5	ns
t_{PHL}				8.9	12.7	1	14.5	1	14.5	1	14.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

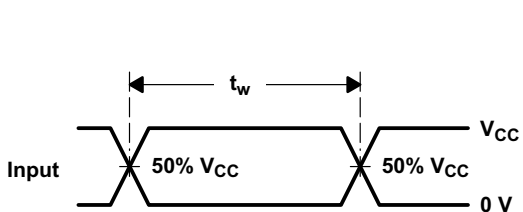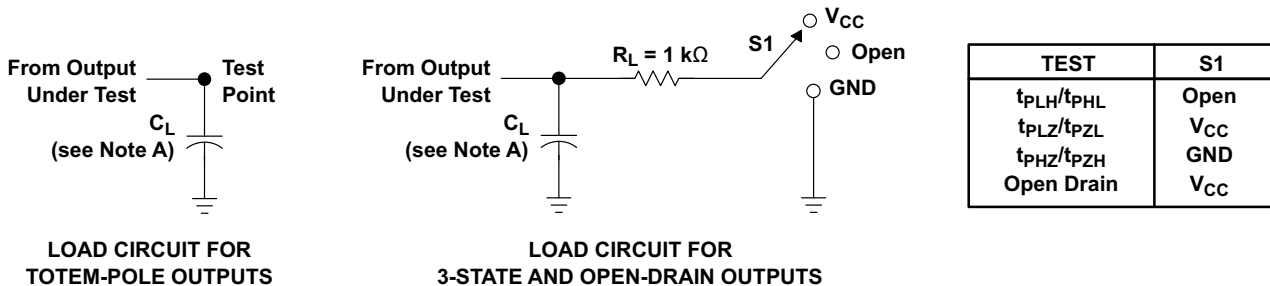| PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
						SN54AHC139		SN74AHC139		Recommended SN74AHC139		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF	5[1]	7.2[1]	1[1]	8.5[1]	1	8.5	1	8.5	ns
t_{PHL}				5[1]	7.2[1]	1[1]	8.5[1]	1	8.5	1	8.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF	4.4[1]	6.3[1]	1[1]	7.5[1]	1	7.5	1	7.5	ns
t_{PHL}				4.4[1]	6.3[1]	1[1]	7.5[1]	1	7.5	1	7.5	
t_{PLH}	A or B	Y	C_L = 50 pF	6.5	9.5	1	10.5	1	10.5	1	10.5	ns
t_{PHL}				6.5	9.5	1	10.5	1	10.5	1	10.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF	5.9	8.3	1	9.5	1	9.5	1	9.5	ns
t_{PHL}				5.9	8.3	1	9.5	1	9.5	1	9.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
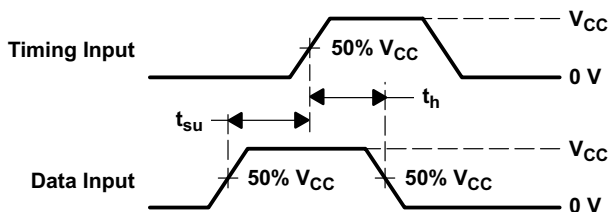
OPERATING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	13	pF

PARAMETER MEASUREMENT INFORMATION

From Output Under Test — **Test Point**
C_L (see Note A)

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

From Output Under Test — $R_L = 1 \text{ k}\Omega$ — S1 — V_{CC} / Open / GND
C_L (see Note A)

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

Input — t_w — 50% V_{CC} — 50% V_{CC} — V_{CC} / 0 V

VOLTAGE WAVEFORMS PULSE DURATION

Timing Input — 50% V_{CC} — V_{CC} / 0 V
t_{su} — t_h
Data Input — 50% V_{CC} — 50% V_{CC} — V_{CC} / 0 V

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

Input — 50% V_{CC} — 50% V_{CC} — V_{CC} / 0 V
t_{PLH} — t_{PHL}
In-Phase Output — 50% V_{CC} — 50% V_{CC} — V_{OH} / V_{OL}
t_{PHL} — t_{PLH}
Out-of-Phase Output — 50% V_{CC} — 50% V_{CC} — V_{OH} / V_{OL}
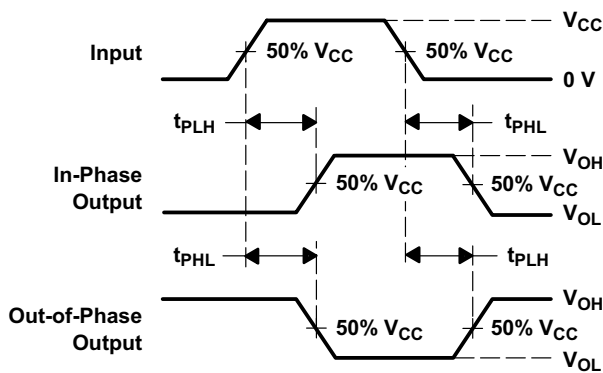
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

Output Control — 50% V_{CC} — 50% V_{CC} — V_{CC} / 0 V
t_{PZL} — t_{PLZ}
Output Waveform 1 S1 at V_{CC} (see Note B) — 50% V_{CC} — $\approx V_{CC}$ / $V_{OL} + 0.3$ V / V_{OL}
t_{PZH} — t_{PHZ}
Output Waveform 2 S1 at GND (see Note B) — 50% V_{CC} — $V_{OH} - 0.3$ V / V_{OH} / ≈ 0 V
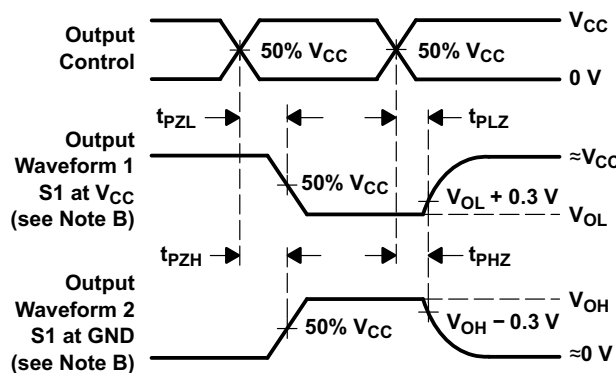
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \ \Omega$, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74AHC139 SN54AHC139*

REVISION HISTORY

Changes from Revision K (December 1995) to Revision L

Page

Product Folder Links: *SN74AHC139 SN54AHC139*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC139D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC139	
SN74AHC139DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA139	Samples
SN74AHC139DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA139	Samples
SN74AHC139DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC139	Samples
SN74AHC139N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC139N	Samples
SN74AHC139NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC139	Samples
SN74AHC139PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA139	Samples
SN74AHC139RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA139	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC139DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC139DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC139DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC139NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC139PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC139RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC139DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHC139DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74AHC139DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC139NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74AHC139PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC139RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
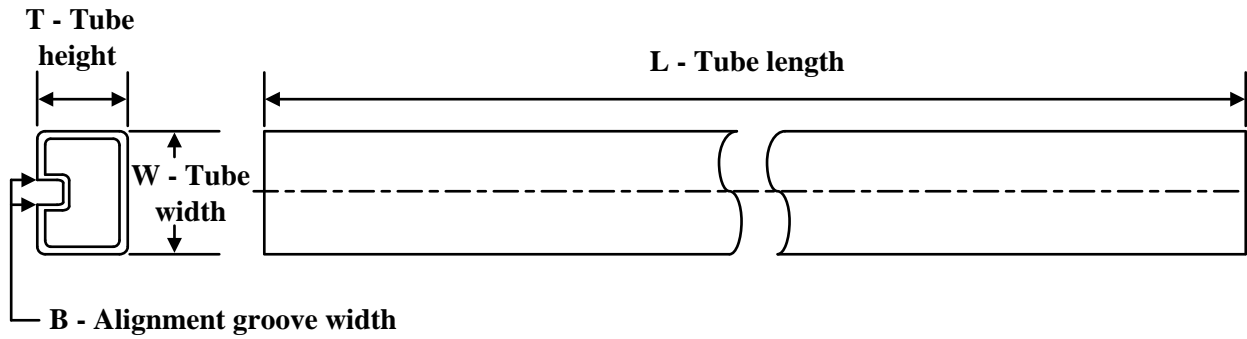
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC139D	D	SOIC	16	40	507	8	3940	4.32
SN74AHC139N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC139N	N	PDIP	16	25	506	13.97	11230	4.32

8.2
7.4 TYP

A

PIN 1 ID
AREA

1

16

14X | 1.27 |

10.4
10.0
NOTE 3

2X
| 8.89 |

8

9

B

5.4
5.2
NOTE 4

16X 0.51
0.35

| ⊕ | 0.25Ⓜ | C | A | B |

C

SEATING PLANE

| ⌒ | 0.1 | C |

2.00 MAX

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0° - 10°

1.05
0.55

(1.25)

0.3
0.1

DETAIL A
TYPICAL
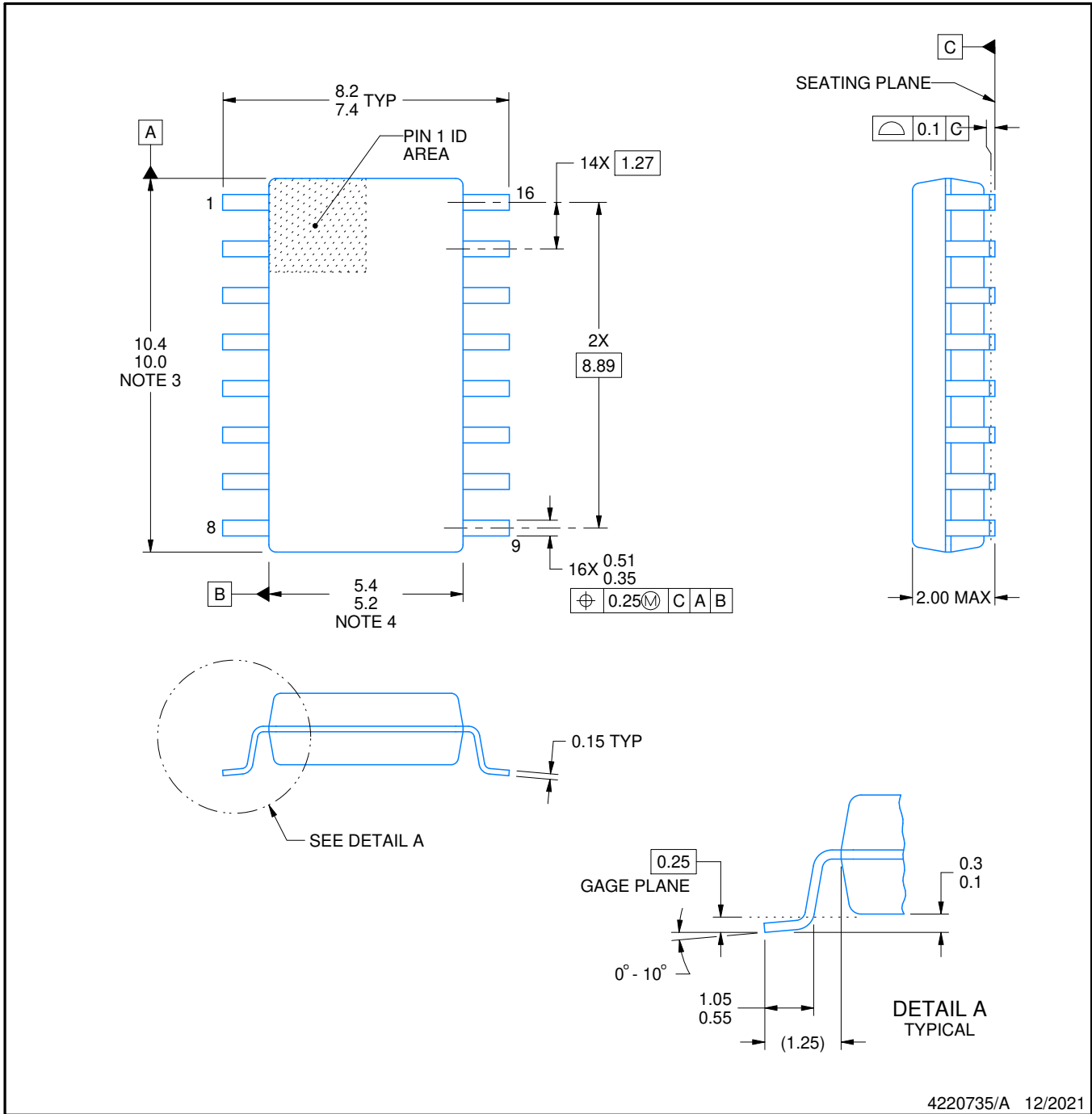
4220735/A   12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
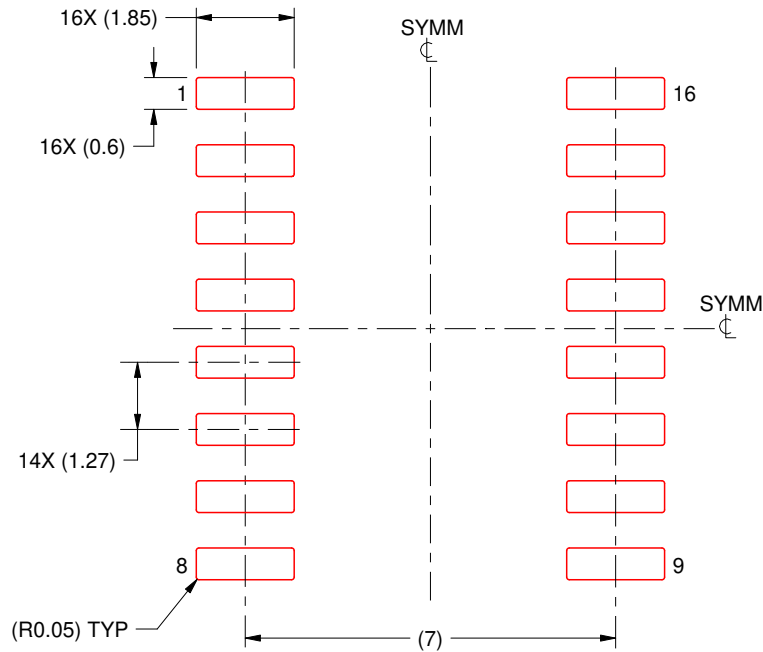4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

Texas
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16X (1.85)

SYMM

SEE
DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM

1

16X (0.6)

16

14X (1.27)

SYMM

8

9

(R0.05) TYP

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
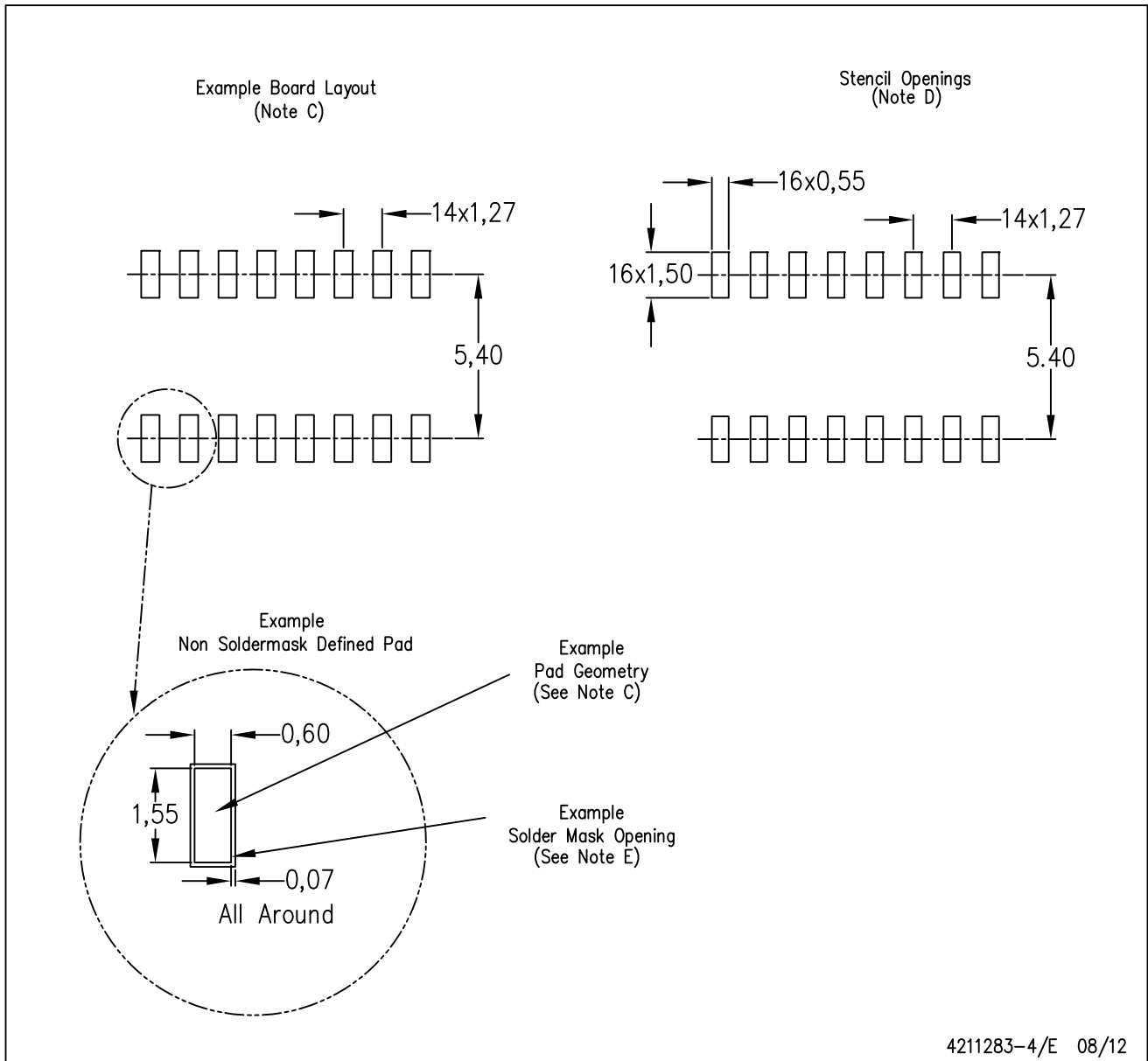SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
8. Board assembly site may have different recommendations for stencil design.
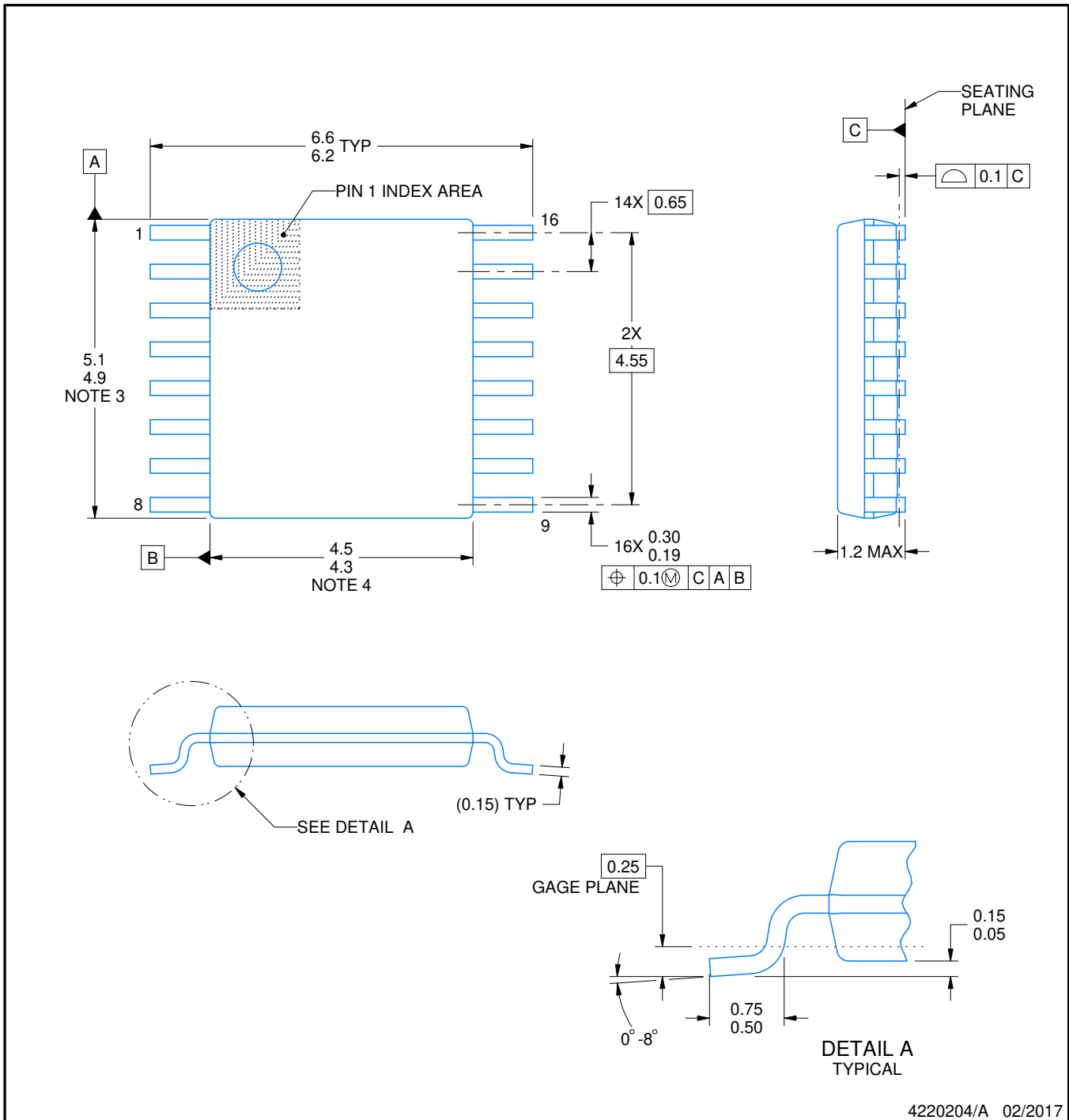
D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
―――――――――
0.386 (9,80)
△C

16   9

0.244 (6,20)
―――――――――
0.228 (5,80)

0.157 (4,00)
――――――――― △D
0.150 (3,80)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
―――――――――
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
―――――――――
0.004 (0,10)

0.010 (0,25)
―――――――――
0.005 (0,13)

△ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
―――――――――
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      △C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
      △D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

TEXAS
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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←14x1,27

16x0,55

14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

16

14X [0.65]

2X
[4.55]

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.19

⊕ [0.1Ⓜ] C A B

SEATING
PLANE

C

◁ [0.1] C

1.2 MAX

SEE DETAIL A

(0.15) TYP

GAGE PLANE

[0.25]

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND
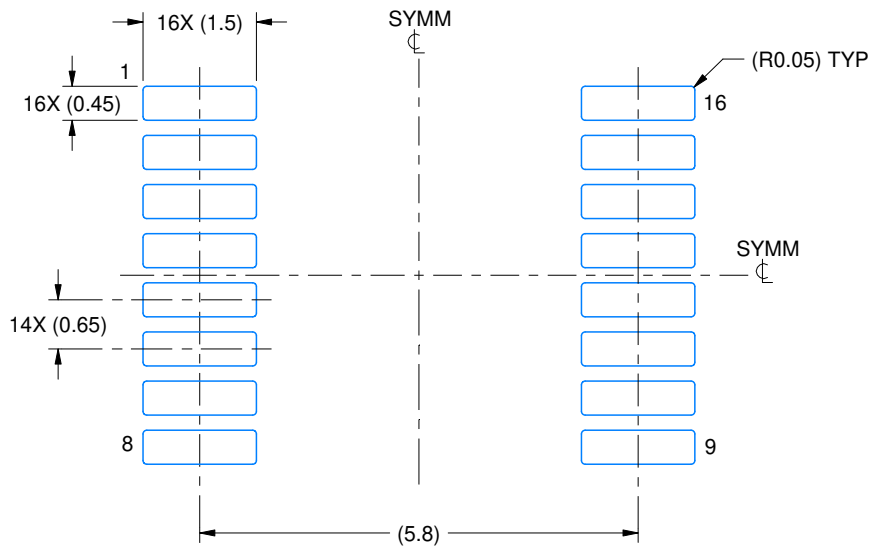
SOLDER MASK
DEFINED
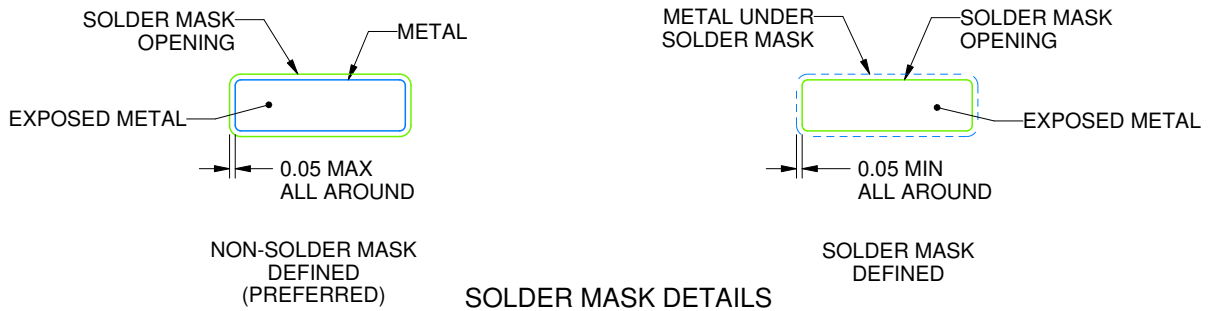
SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
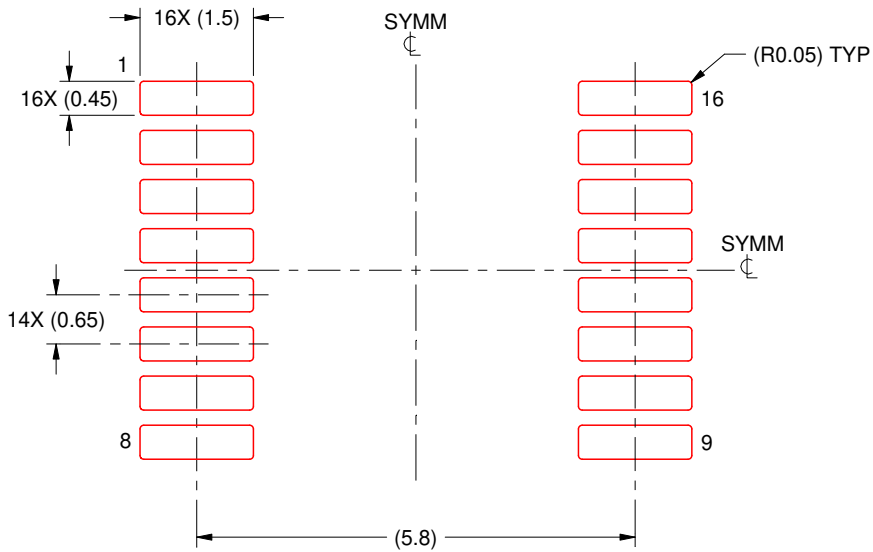
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

8.2
7.4 TYP

A

PIN 1 INDEX AREA

1

16

14X 0.65

2X
4.55

6.5
5.9
NOTE 3

8

9

16X 0.38
0.22

B

5.6
5.0
NOTE 4

⊕ 0.1 Ⓜ C A B

C

⌒ 0.1 C

SEATING
PLANE

0.25
0.09

SEE DETAIL A

GAGE PLANE

0.25

0° -8°

0.95
0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4220763/A   05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

16X (1.85)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220763/A   05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

1

16X (0.45)

SYMM

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(7)
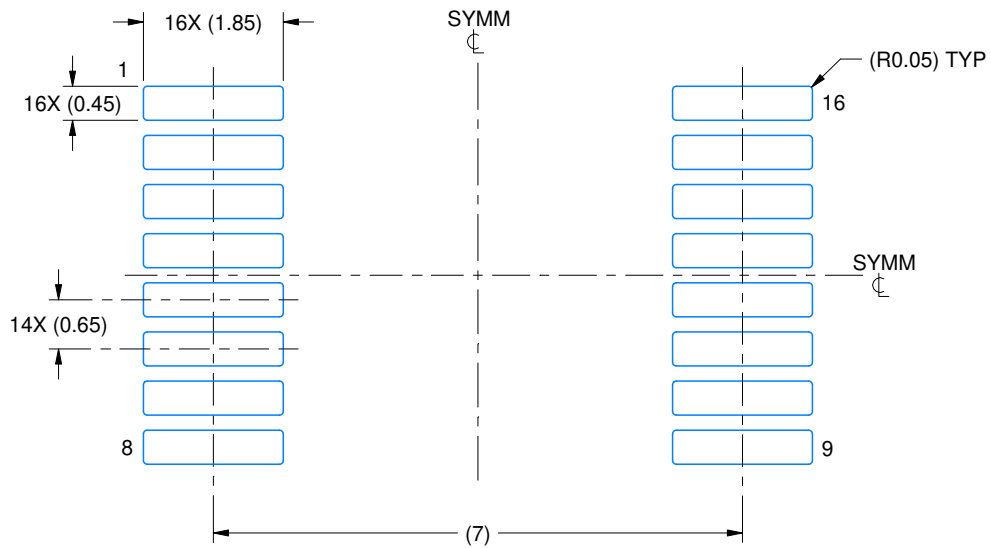
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
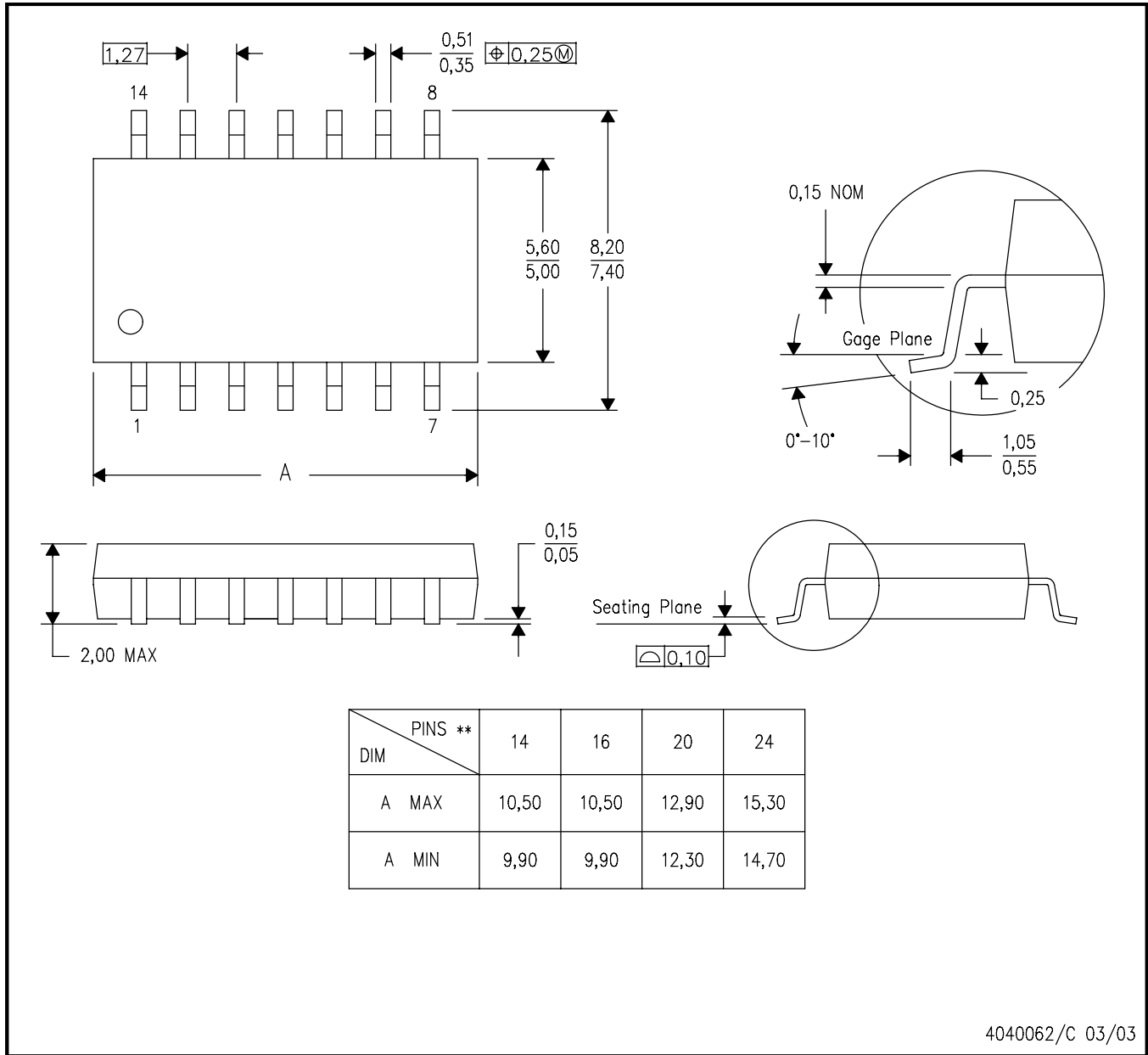SCALE: 10X

4220763/A   05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

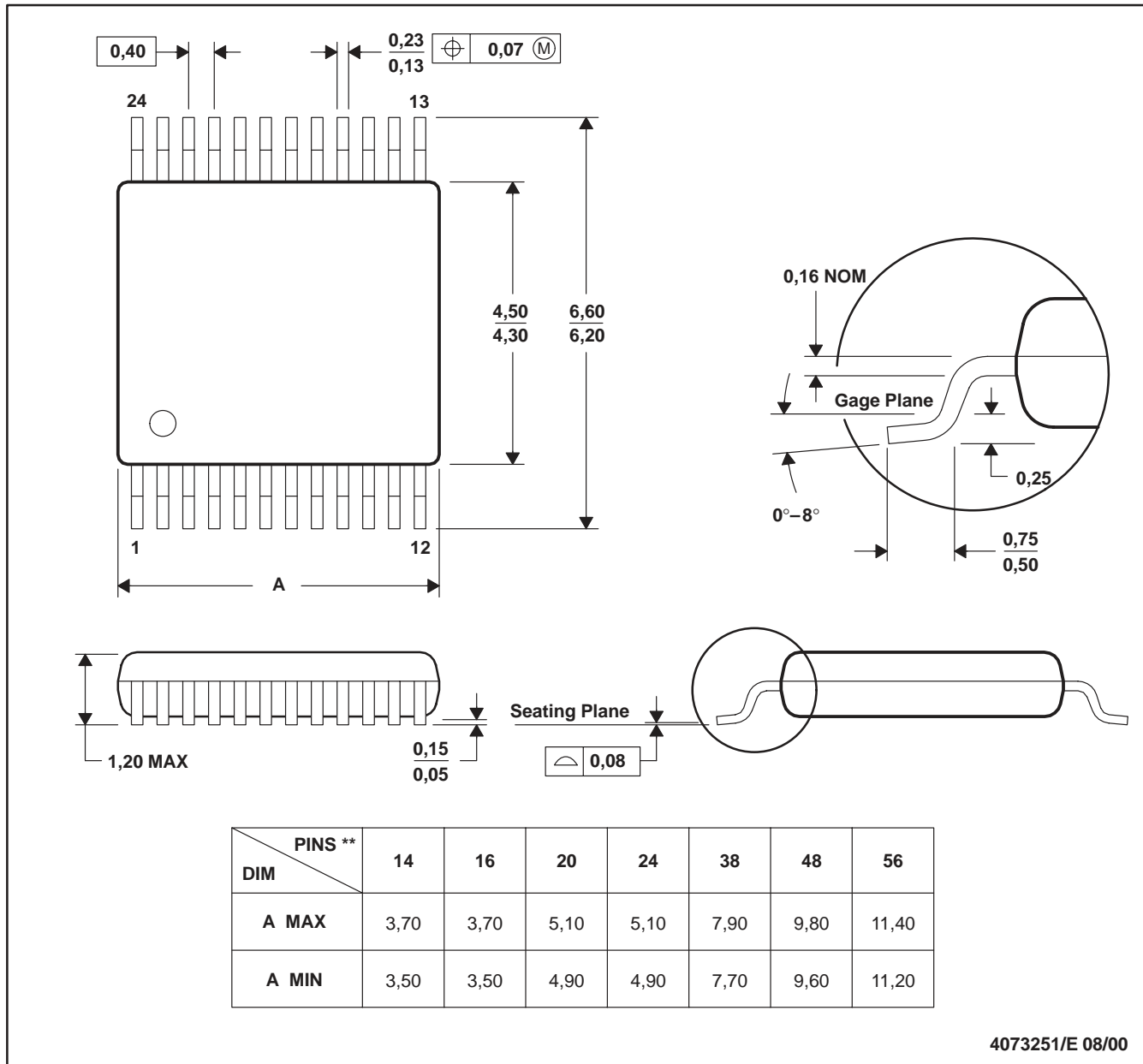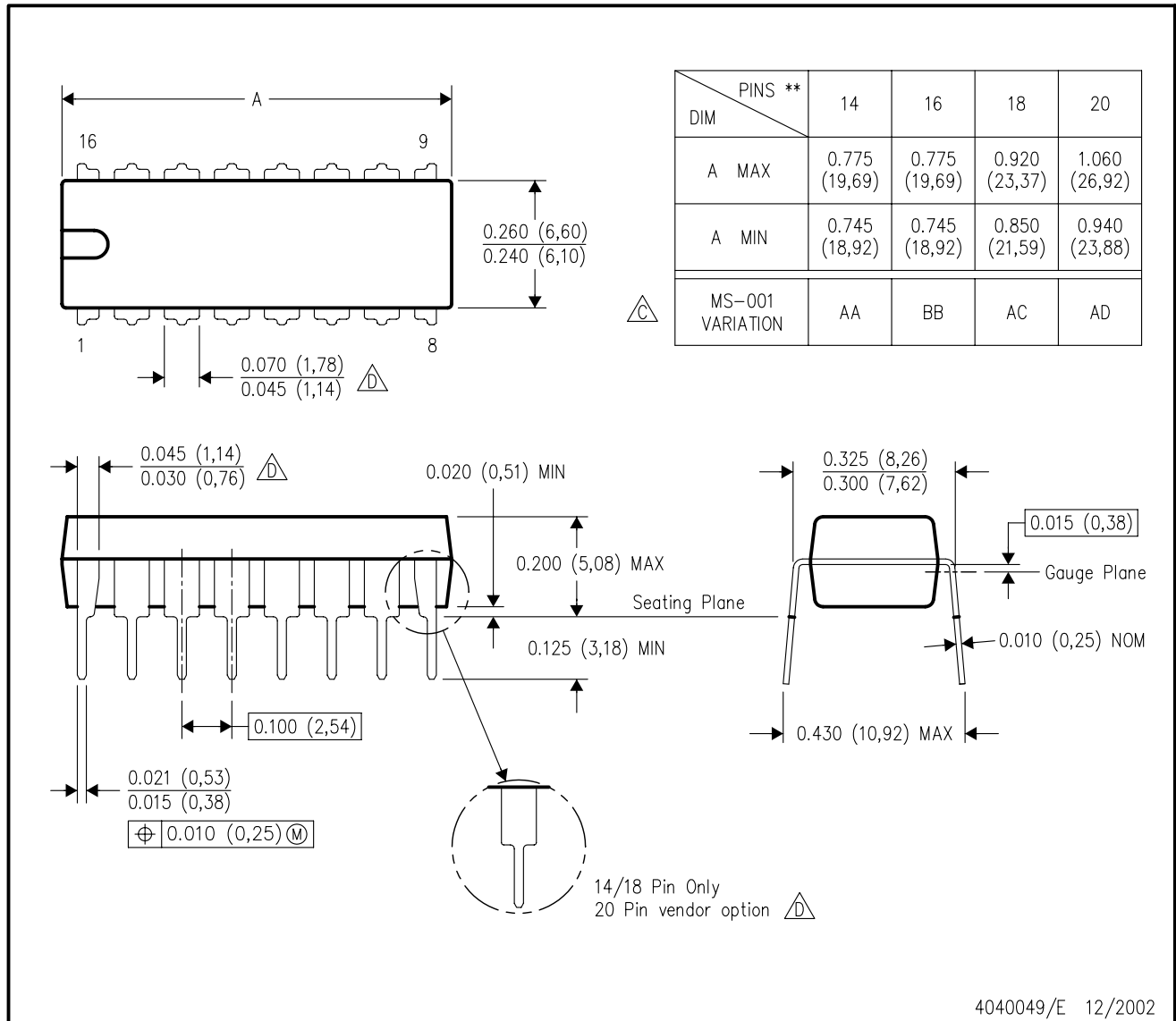| PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

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N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD

Pin 1 Index Area
Top and Bottom

0,20 Nominal
Lead Frame

Seating Plane

0,05
0,00
Seating Height

Bottom View

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

4203539-3/I   06/2011
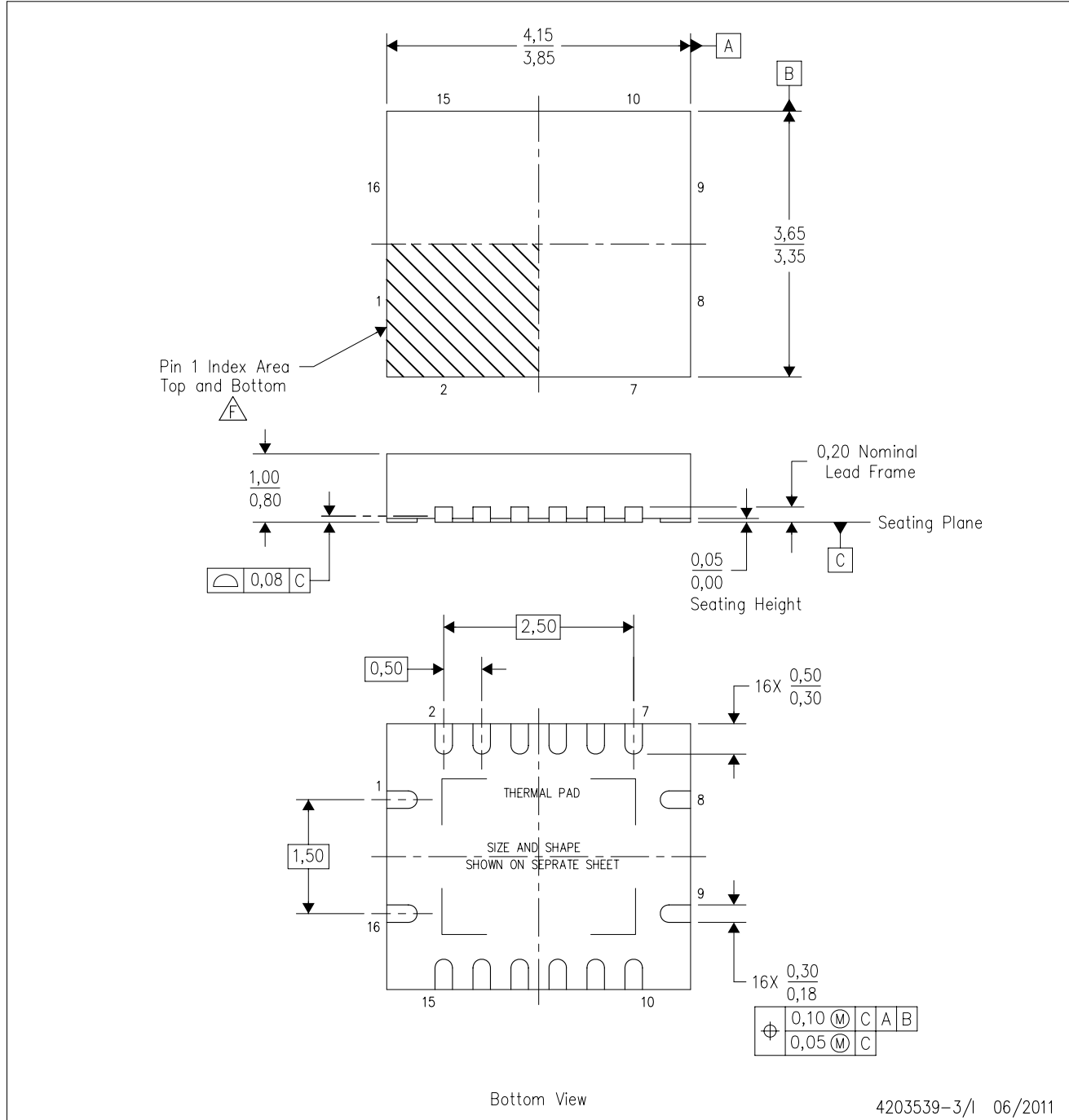
NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No-Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
              The Pin 1 identifiers are either a molded, marked, or metal feature.
   G.   Package complies to JEDEC MO-241 variation BA.

RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
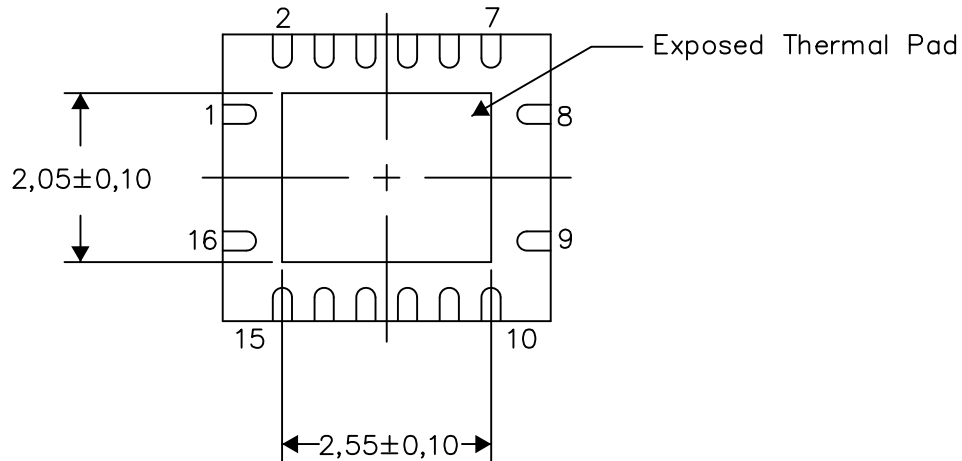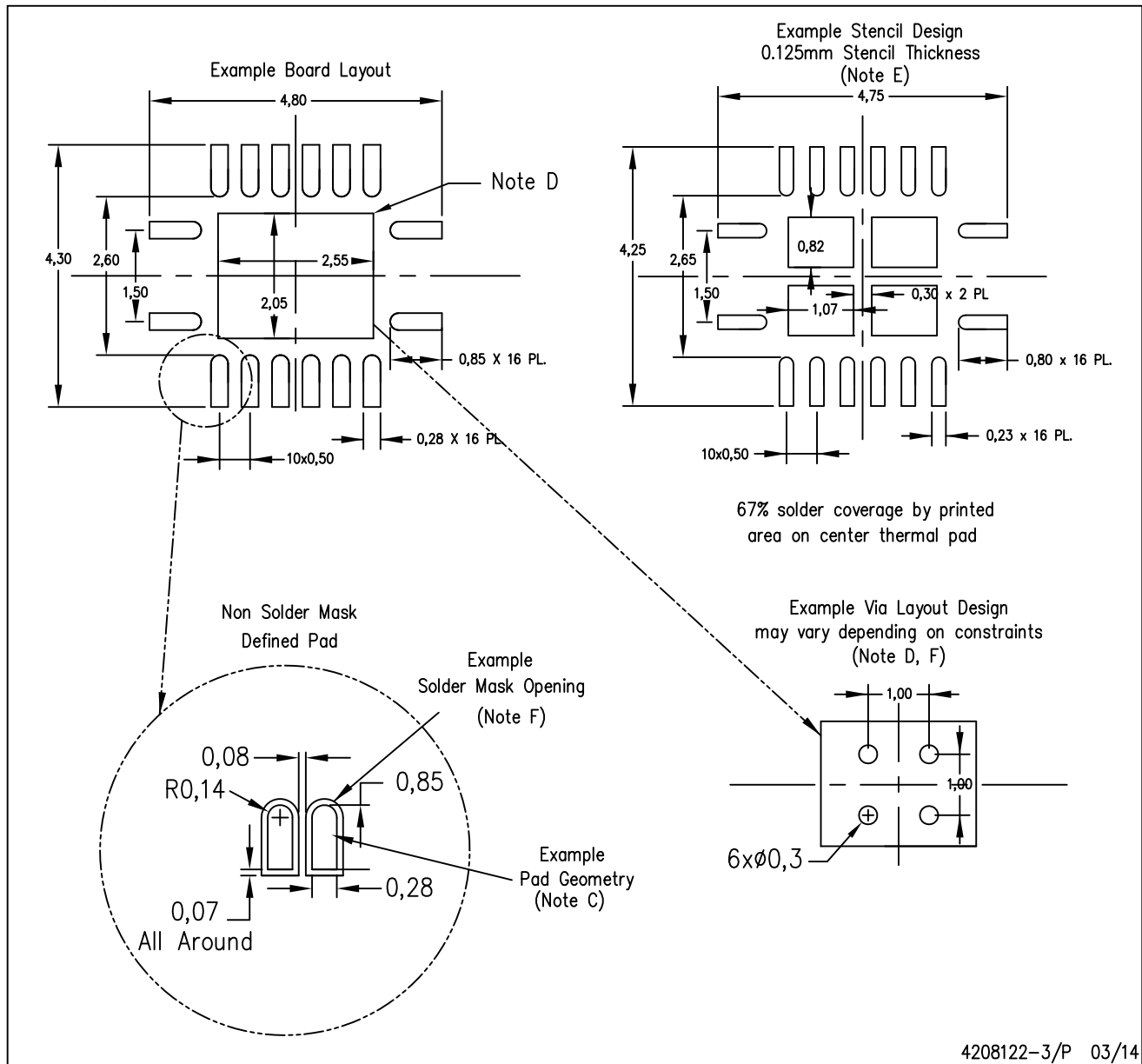

Bottom View

Exposed Thermal Pad Dimensions

4206353−3/P   03/14

NOTE: All linear dimensions are in millimeters

RGY (R—PVQFN—N16)   PLASTIC QUAD FLATPACK NO—LEAD

Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

Note D

4,80

4,30 2,60

1,50

2,55

2,05

0,85 X 16 PL.

0,28 X 16 PL.

10x0,50

4,75

4,25 2,65

1,50

0,82

0,30 x 2 PL

1,07

0,80 x 16 PL.

0,23 x 16 PL.

10x0,50

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Pad Geometry
(Note C)

1,00

1,00

6xØ0,3

4208122—3/P   03/14

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC—7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack
              QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.
              These documents are available at www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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