Ordering number : ENA2059

LV8829LFQA

ON Semiconductor®

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Bi-CMOS IC

For Brushless Motor Drive
PWM Driver IC

Overview

The LV8829LFQA is a PWM-type driver IC designed for 3-phase brushless motors. The rotational speed can be controlled by inputting the PWM pulse from the outside, and changing Duty. The IC incorporates a latch-type constraint protection circuit.

Features

- I_O max = 1.5A (built-in output Tr)
- Speed control and synchronous rectification using direct PWM input (supports 3.3V inputs)
- 1-Hall FG output
- Latch type constraint protection circuit (the latch is released by S/S and F/R.)
- Forward/reverse switching circuit, Hall bias pin
- Power save circuit (Power save in stop mode)
- Current limiter circuit, Low-voltage protection circuit, Overheat protection circuit
- Charge pump circuit, 5V regulator output.
- Start/stop circuit (short brake when motor is to be stopped)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	V_{CC} pin	36	V
	V_G max	V_G pin	42	V
Output current	I_O max	t ≤ 500ms *1	1.5	A
Allowable power dissipation	Pd max	Mounted on a circuit board.*2	1.35	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-40 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

*1 : Tj cannot exceed Tj max = 150°C

*2 : Specified circuit board : 40mm × 50mm × 0.8mm, glass epoxy (four-layer board)

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		8.0 to 35	V
5V constant voltage output current	I_{REG}		0 to -10	mA
HB pin output current	I_{HB}		0 to -200	μA
FG pin applied voltage	V_{FG}		0 to 6	V
FG pin output current	I_{FG}		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			3.3	4.0	mA
Supply current 2	$I_{CC}2$	At stop		0.7	0.8	mA
Output block						
Low-side output ON resistance	R_{ON} (L1)	I_O = 1.0A		0.47	0.65	Ω
High-side output ON resistance	R_{ON} (H1)	I_O = -1.0A		0.67	0.9	Ω
Low-side output leak current	I_L (L)				50	μA
High-side output leak current	I_L (H)		-50			μA
Low-side diode forward voltage	V_D (L1)	I_D = -1.0A		1.0	1.2	V
High-side diode forward voltage	V_D (H1)	I_D = 1.0A		1.1	1.3	V
5V Constant-voltage Output						
Output voltage	VREG	I_O = -5mA	4.8	5.1	5.4	V
Line regulation	ΔV (REG1)	V_{CC} = 8 to 35V, I_O = -5mA			50	mV
Load regulation	ΔV (REG2)	I_O = -5m to -10mA			100	mV
Hall Amplifier						
Input bias current	IB (HA)		-2			μA
Common-mode input voltage range 1	VICM1	When using Hall elements	0.3		VREG-1.7	V
Common-mode input voltage range 2	VICM2	At one-side input bias (Hall IC application)	0		VREG	V
Hall input sensitivity	VHIN	SIN wave	80			mVp-p
Hysteresis width	ΔV_{IN} (HA)		9	20	35	mV
Input voltage Low → High	VSLH		3	9	16	mV
Input voltage High → Low	VSHL		-19	-11	-5	mV
CSD oscillator circuit						
High level output voltage	V_{OH} (CSD)		2.7	3.0	3.3	V
Low level output voltage	V_{OL} (CSD)		0.9	1.1	1.3	V
Amplitude	V (CSD)		1.6	1.9	2.2	Vp-p
External capacitor charge current	ICHG1 (CSD)	VCHG1 = 2.0V	-14	-11.5	-9	μA
External capacitor discharge current	ICHG2 (CSD)	VCHG2 = 2.0V	9.5	12	14.5	μA
Oscillation frequency	f (CSD)	C = 0.022μF (Design target value)		130		Hz
Charge pump output (VG pin)						
Output voltage	VGOUT			V_{CC}+4.5		V
CP1 pin						
Output ON resistance (High level)	V_{OH} (CP1)	ICP1 = -2mA		500	700	Ω
Output ON resistance (Low level)	V_{OL} (CP1)	ICP1 = 2mA		350	500	Ω
Charge pump frequency	f (CP)		82	103	124	kHz
Internal PWM frequency						
Oscillation frequency	f (PWM)		41	51.5	62	kHz
Current limiter operation						
Limiter voltage	VRF		0.19	0.21	0.23	V

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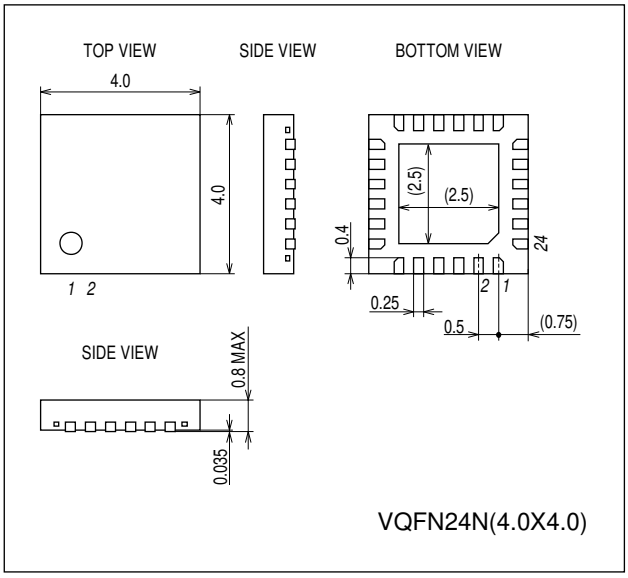
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Thermal shutdown operation						
Thermal shutdown operation temperature	TSD	*Design target value (junction temperature)	150	165	180	°C
Hysteresis width	ΔTSD	*Design target value (junction temperature)		30		°C
HB pin						
Output voltage	VHB	IHB = -100μA	3.4	3.6	3.8	V
Low-voltage protection (5V constant-voltage output detection)						
Operation voltage	VSD		3.95	4.15	4.35	V
Hysteresis width	ΔVSD		0.2	0.3	0.4	V
FG pin (3FG pin)						
Output ON resistance	VOL (FG)	IFG = 5mA		40	60	Ω
Output leak current	IL (FG)	V_O = 5V			10	μA
S/S pin						
High level input voltage	V_{IH} (SS)		2.0		VREG	V
Low level input voltage	V_{IL} (SS)		0		1.0	V
Input open voltage	V_{IO} (SS)		VREG-2.2	VREG-2.0	VREG-1.8	V
Hysteresis width	V_{IS} (SS)		0.25	0.33	0.4	V
High level input current	I_{IH} (SS)	V_{SS} = VREG	45	60	75	μA
Low level input current	I_{IL} (SS)	V_{SS} = 0V	-115	-90	-65	μA
PWMIN pin						
Recommended input frequency	f(PWIN)		0.5		60	kHz
High level input voltage	V_{IH} (PWIN)		2.0		VREG	V
Low level input voltage	V_{IL} (PWIN)		0		1.0	V
Input open voltage	V_{IO} (PWIN)		VREG-2.2	VREG-2.0	VREG-1.8	V
Hysteresis width	V_{IS} (PWIN)		0.25	0.33	0.4	V
High level input current	I_{IH} (PWIN)	VPWIN = VREG	45	60	75	μA
Low level input current	I_{IL} (PWIN)	VPWIN = 0V	-115	-90	-65	μA
F/R pin						
High level input voltage	V_{IH} (FR)	*Design target value	2.0		VREG	V
Low level input voltage	V_{IL} (FR)	*Design target value	0		1.0	V
Input open voltage	V_{IO} (FR)		VREG-2.2	VREG-2.0	VREG-1.8	V
Hysteresis width	V_{IS} (FR)	*Design target value	0.25	0.33	0.4	V
High level input current	I_{IH} (FR)	VF/R = VREG	45	60	75	μA
Low level input current	I_{IL} (FR)	VF/R = 0V	-115	-90	-65	μA

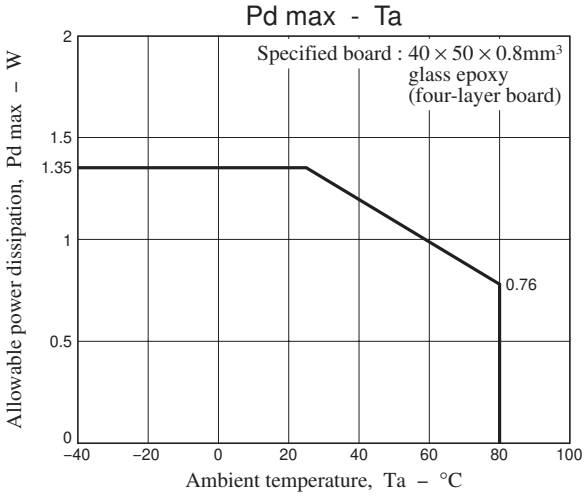
* : Design target value and no measurement is made.

Package Dimensions

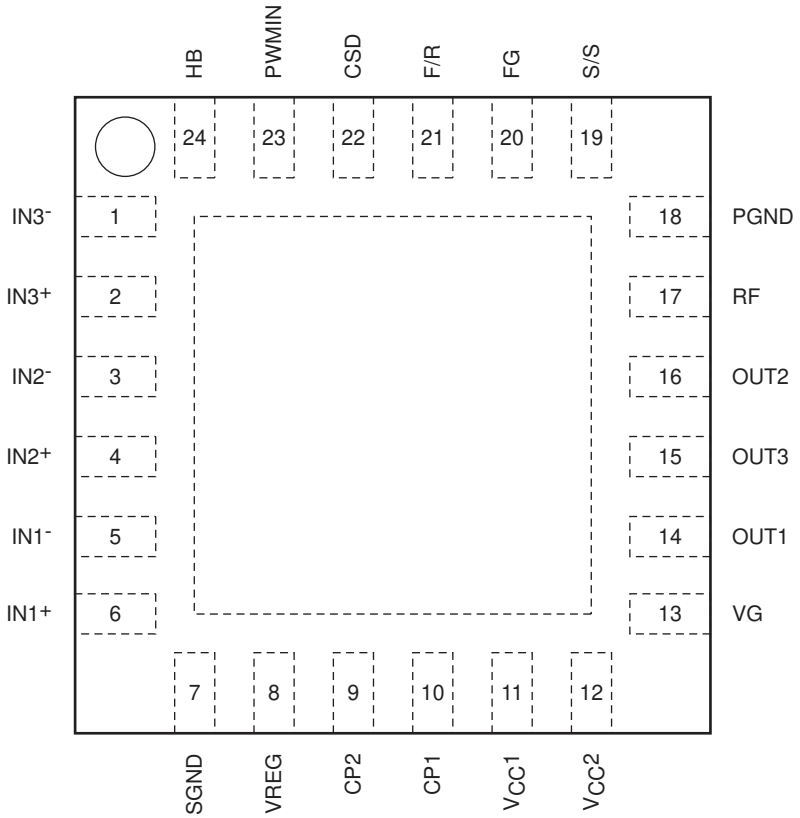
unit : mm (typ)

3430





Pin Assignment



Three-phase logic truth table (IN = "High" indicates the state where $IN^+ > IN^-$.)

("H" = SOURCE, "L" = SINK, and "M" = output OFF are shown with OUT1 to 3.)

F/R = 「H」			F/R = 「L」			Output		
IN1	IN2	IN3	IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	L	L	H	M
H	L	L	L	H	H	L	M	H
H	H	L	L	L	H	M	L	H
L	H	L	H	L	H	H	L	M
L	H	H	H	L	L	H	M	L
L	L	H	H	H	L	M	H	L

FG output			
IN1	IN2	IN3	FG
H	L	H	L
H	L	L	L
H	H	L	L
L	H	L	H
L	H	H	H
L	L	H	H

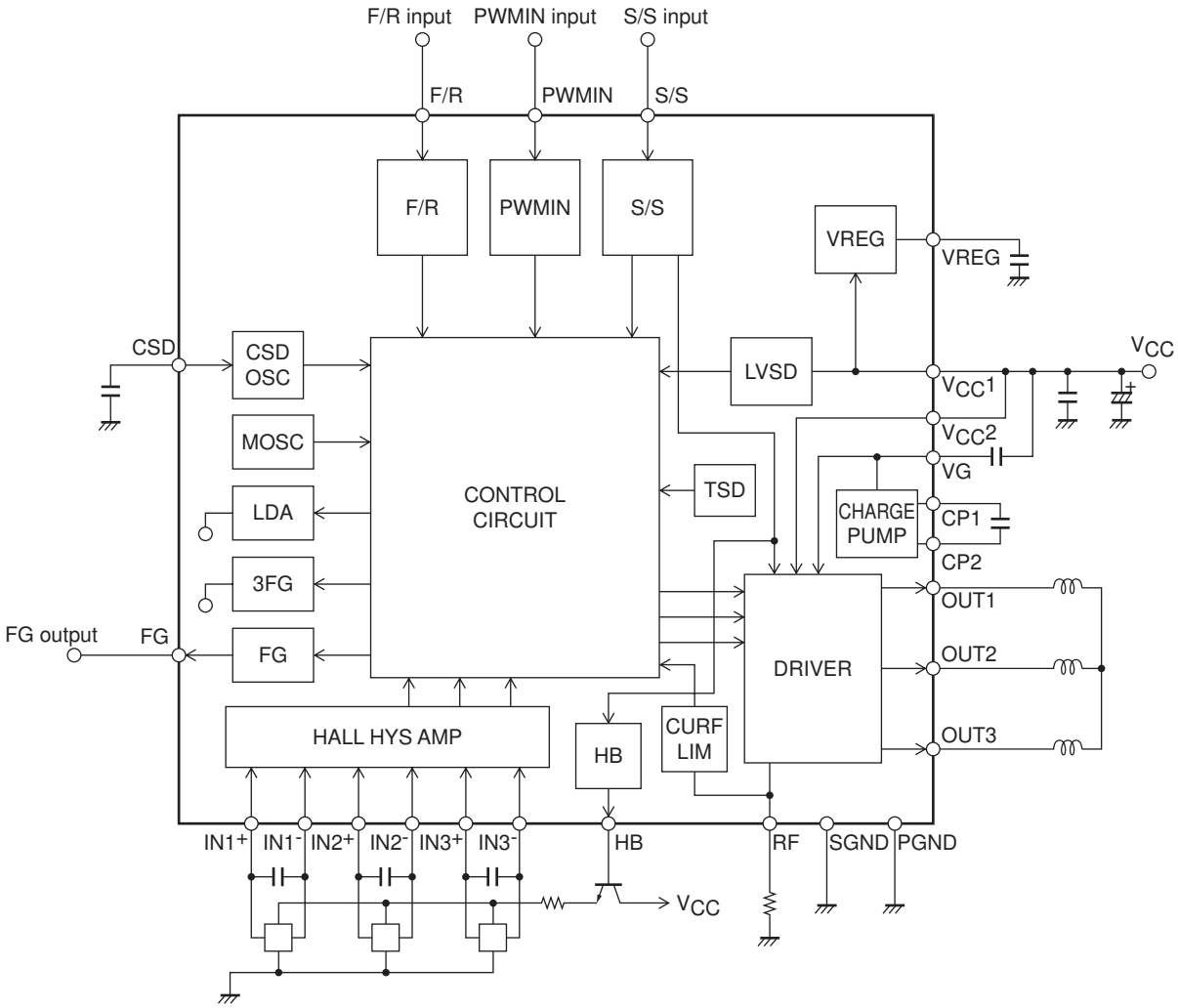
S/S pin, PWMIN pin

Input state	S/S pin	PWMIN pin
High or Open	Stop (short brake)	Output OFF
Low	Start	Output ON

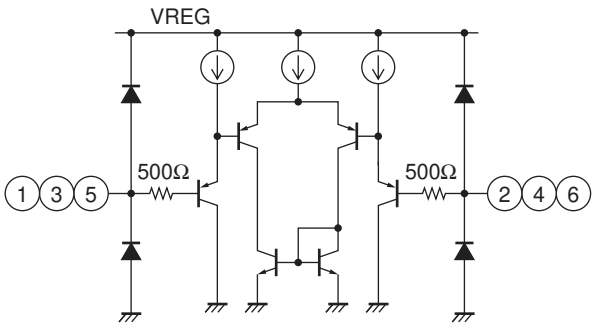
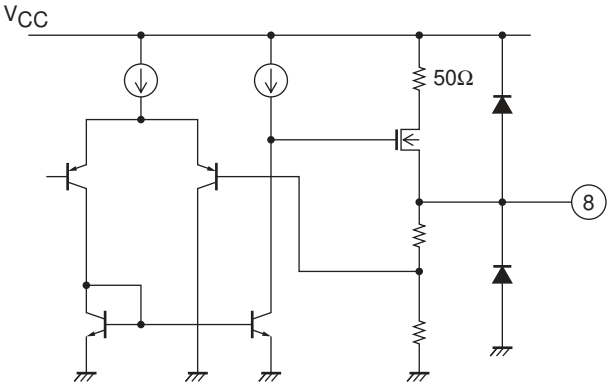
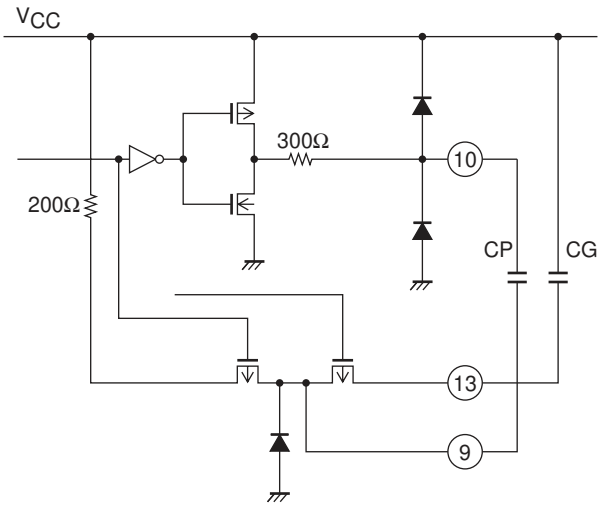
CSD function

When the S/S pin is in a STOP state → Protection released and count reset(Initial reset)
When the F/R pin is switched → Protection released and count reset
When 0% duty is detected at the PWMIN pin input → Protection released and count reset
When low-voltage condition is detected → Protection released and count reset (Initial reset)
When TSD condition is detected → Stop counting

Internal Equivalent Circuit and Sample External Component Circuit



Pin Functions

Pin No.	Pin Name	Pin function	Equivalent Circuit
1 2 3 4 5 6	$IN3^-$ $IN3^+$ $IN2^-$ $IN2^+$ $IN1^-$ $IN1^+$	Hall input pin. •High when $IN^+ > IN^-$. Low in reverse relationship. The input amplitude of over 100mVp-p (differential) is desirable in the Hall inputs. Insert a capacitor between the IN^+ and IN^- pins if the noise on the Hall signal is a problem.	
7	SGND	Control circuit block ground pin.	
8	VREG	5V regulator output pin (control circuit power supply). Insert a capacitor between this pin and ground for stabilization. About 1μF is necessary. (Refer to 11 pages “5 is Low-voltage Protection Circuit.", 12 pages “10 is VREG Stabilization.”)	
9 10	CP2 CP1	Charge pump capacitor connection pin. Insert capacitor between CP1 and CP2.	
11 12	$V_{CC}1$ $V_{CC}2$	For Control (Pin 11) and for output (Pin 12) power pin. Insert a capacitor between this pin and ground to prevent the influence of noise, etc. (Refer to 12 pages “9 is Power Supply Stabilization.")	
13	VG	Charge pump output pin. (Upper-side FET gate power supply) Insert a capacitor between this pin and V_{CC}. (Refer to 12 pages “11 is Charge pump Circuit.")	

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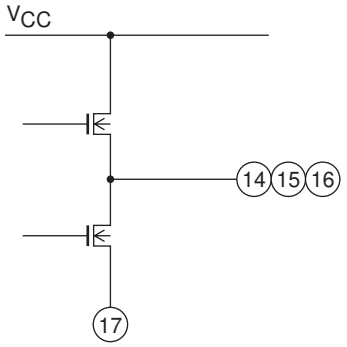
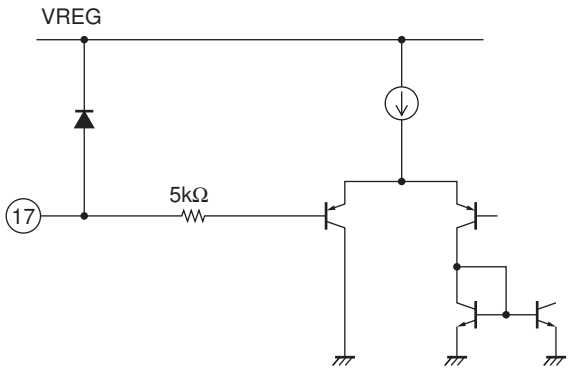
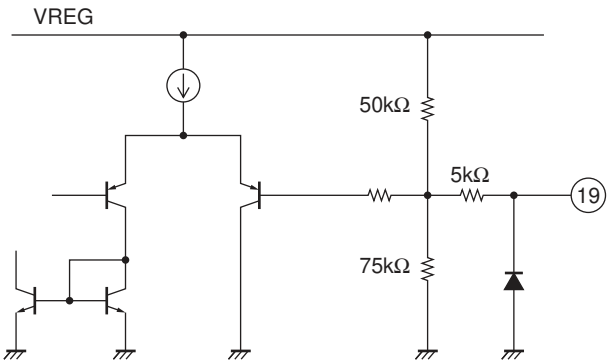
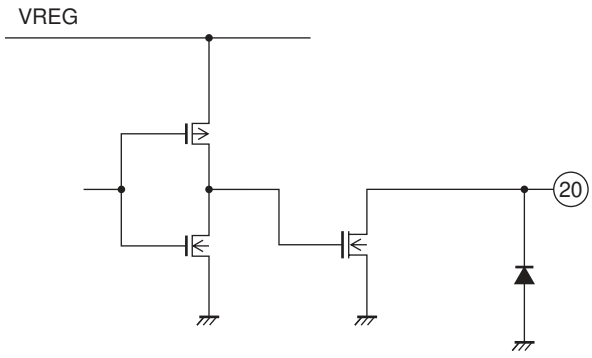
Pin No.	Pin Name	Pin function	Equivalent Circuit
14 15 16	OUT1 OUT3 OUT2	Output pin. PWM is controlled by the upper-side FET.	
17	RF	Output current detection pin. Insert a low resistance resistor (Rf) between this pin and ground. (Refer to 10 pages “2 is Current Limiter Circuit.")	
18	PGND	Out circuit block ground pin.	
19	S/S	Pin to select the start/stop type. Stop = High or open Start = Low (Refer to 12 pages “8 is Power Saving Circuit.")	
20	FG	1-Hall FG signal output pin. Open drain output.	

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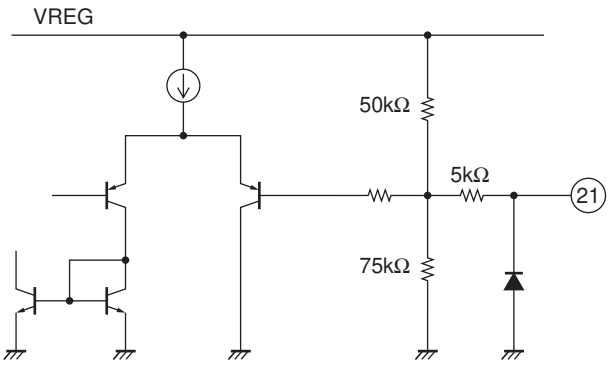
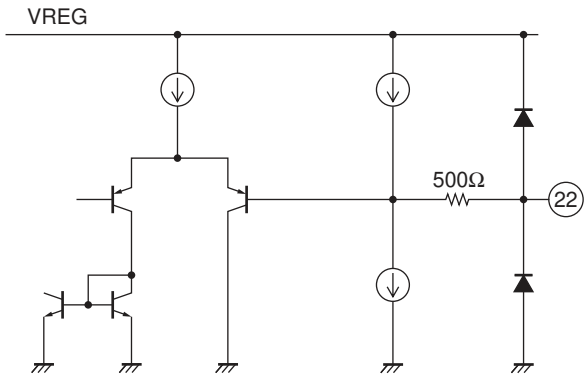
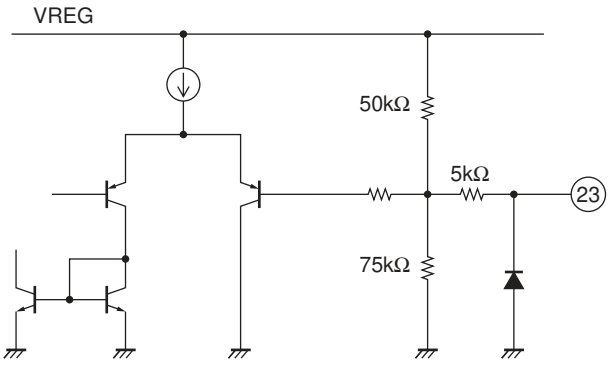
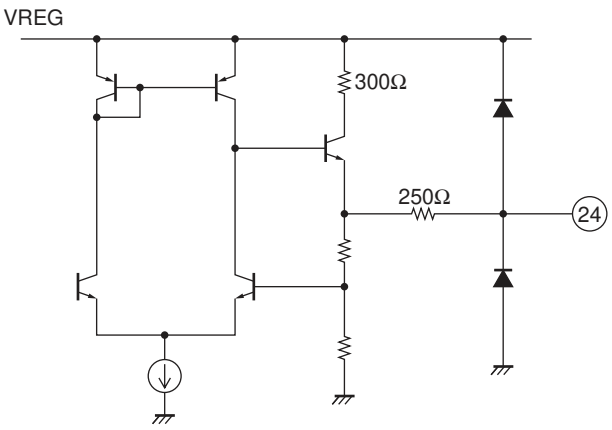
Pin No.	Pin Name	Pin function	Equivalent Circuit
21	F/R	Pin to select the forward/reverse type. This pin goes to the high level when open.	
22	CSD	Pin to set the constraint protection circuit operating time and initial reset pulse. Insert a capacitor between this pin and ground. Insert a resistor in parallel with the capacitor if the protection circuit is not to be used. (Refer to 10 pages “4 is Constraint Protection Circuit.")	
23	PWMIN	External PWM input pin. Apply an external PWM input signal to this pin. (Input frequency range is from 0.5 to 60kHz.) PWM ON = Low PWM OFF = High or open (Refer to 10 pages “3 is Speed control method.")	
24	HB	HALL bias pin (3.6V output). Connect an NPN transistor. (Refer to 11 pages “7 Hall Input Signal.")	

Description of LV8829LFQA

1. Output Drive Circuit

This IC adopts a direct PWM drive method to reduce power loss in the output. It regulates the drive force of the motor by changing the output on duty. The output PWM switching is performed by the upper-side output transistor.
The current regeneration route during the normal PWMOFF passes through the parasitic diode of the output DMOS.
This IC performs synchronous rectification, and is intended to reduce heat generation compared to diode regeneration.

2. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation $I = V_{RF}/Rf$ (V_{RF} = 0.21V (typical), Rf: current detection resistor). This circuit suppresses the output current by reducing the output on duty.
The current limiter circuit has an operation delay (approx. 700ns) to detect reverse recovery current flowing in the diode due to the PWM operation, and prevent a malfunction of the current limiting operation. If the coil resistance of the motor is small, or the inductance is low, the current at startup (the state in which there is no back electromotive force generated in the motor) will change rapidly. As a result, the operation delay may sometimes cause the current limiting operation to take place at a value above the set current. In such a case, it is necessary to set the current limit value while taking into consideration the increase in current due to the delay.

* Regarding the PWM frequency in the current limiter circuit
The PWM frequency in the current limiter circuit is determined by the internal reference oscillator, and is approximately 50kHz.

3. Speed control method

Pulses are input to the PWMIN pin, and the output can be controlled by varying the duty cycle of these pulses.
When a low-level input voltage is applied to the PWMIN pin, the output at the PWM side (upper side) is set to ON.
When a high-level input voltage is applied to the PWMIN pin, the output at the PWM side (upper side) is set to OFF.
If it is necessary to input pulses using inverted logic, this can be done by adding an external transistor (NPN).
When the input to the PWMIN pin remains high-level for a certain period, the IC judges that the duty is 0%, causing the CSD circuit count to be reset and the output from the HB pin to become low level.

4. Constraint Protection Circuit

The LV8829LFQA includes a constraint protection circuit for protecting the IC and the motor in a motor constraint mode.
This circuit operates when the motor is in an operation condition and the Hall signal does not switch over for a certain period. Note that while this constraint protection is operating, the upper-side output transistor will be OFF.
Time setting is performed according to the capacitance of the capacitor connected to the CSD pin.

Set time (s) ≈ 90 × C (μF)

When a 0.022μF capacitor is connected, the protection time becomes approximately 2.0 seconds. The set time must be selected to a value that provides adequate margin with respect to the motor startup time.
Conditions for releasing the constraint protection state:

- When the S/S pin is in a STOP state → Protection released and count reset(Initial reset)
- When the F/R pin is switched → Protection released and count reset
- When 0% duty is detected at the PWMIN pin input → Protection released and count reset
- When low-voltage condition is detected → Protection released and count reset (Initial reset)

(• When TSD condition is detected → Stop counting)

The CSD pin also functions as the initial reset pulse generation pin. If it is connected to ground, the logic circuit will go into a reset state, preventing speed control from taking place. Consequently, when not using constraint protection, connect a resistor of approximately 220kΩ and a capacitor of about 4700pF in parallel to ground.

5. Low-voltage Protection Circuit

The LV8829LFQA incorporates a comparator that uses the band gap voltage as the reference. The circuit monitors the voltage at the VREG pin (5V) while the S/S pin is low and activates the protection circuit when the voltage at the VREG pin falls below 4.15V (typ.).
When this happens, the state of the output transistors for all phases set to OFF.

In order to ensure that the IC does not exhibit any unstable behavior when the VREG voltage has increased or decreased around 4.15V, a hysteresis of 0.3V (typ.) is provided. As a result, when the VREG voltage recovers to 4.45V (typ.) after the low-voltage protection circuit has been activated, all output transistors return to their operating state.

6. Thermal shutdown Circuit

When the IC junction temperature exceeds 165°C (design target value), the thermal shutdown circuit is activated, and all the output transistors are set to OFF.

When the IC junction temperature goes below the hysteresis temperature of 30°C (design target value) or more, all the output transistors return to their operating state.

However, as the thermal shutdown circuit is activated only when the junction temperature of the IC has exceeded the rating, its activation does not constitute a guarantee that the product that incorporates this circuit will be protected from damage or destruction.

7. Hall Input Signal

A pulse input with the amplitude in excess of the hysteresis (35mV maximum) is required for the Hall inputs.

It is desirable that the amplitude of the Hall input signal be 100mVp-p or more in consideration of the effect of noise and phase displacement.

If disturbances to the output waveform (during phase switching) occur due to noise, connect a capacitor between the Hall input pins to prevent such disturbances. In the constraint protection circuit, the Hall input is utilized as a judgment signal. Although the circuit ignores a certain amount of noise, caution is necessary.

If all three phases of the Hall input signal go to the same input state (HHH or LLL), the outputs are all set to the OFF state.

If the Hall IC is used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range (between 0.3V and VREG-1.7V) allows the other input side to be used as an input over the 0V to VREG range.

○ Method of connecting Hall elements

Type (1) connection (three Hall elements connected in series)

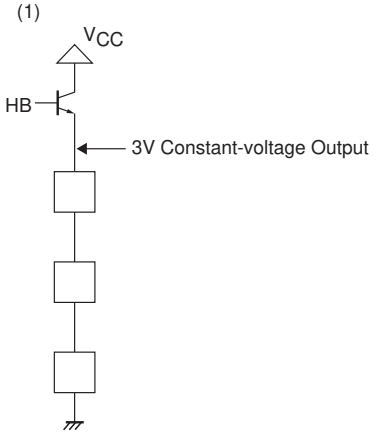
Advantages

- Because the current flowing in Hall elements can be shared by connecting the Hall elements in series, the current consumption is less than that of a parallel-connected arrangement.
- The use of a current limiting resistor can be eliminated.
- Fluctuations of amplitude with temperature are reduced.

Disadvantages

- Because only 1V can be applied to one Hall device, there is a possibility that adequate amplitude cannot be obtained.
- The current flowing in the Hall elements varies with temperature.
- HALL element unevenness (input resistance in particular) is easy to influence the amplitude.

(1)



Type (2) connection (three Hall elements connected in parallel)

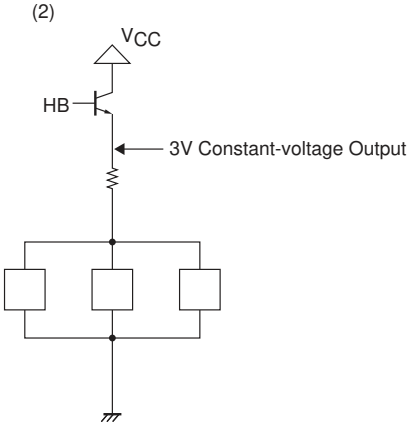
Advantages

- The current flowing in the Hall elements can be determined by the current limiting resistor.
- The voltage applied to the Hall elements can be varied, enabling adequate amplitude to be obtained.

Disadvantages

- Because it is necessary to supply current separately to each Hall element, the current consumption becomes large.
- A current limiting resistor is necessary.
- The amplitude varies with temperature.

(2)



○ HB pin

The HB pin is used for cutting off the current flowing in the Hall elements during standby (for saving electricity).

The output from the HB pin is set to OFF in the following cases.

- When the S/S pin is in a STOP state
- When 0% duty is detected at the PWMIN pin input

8. Power Saving Circuit (Start/Stop circuit)

To save power when the LV8829LFQA is in the stop state, most of the circuit is stopped, aiming at reducing current consumption. If the Hall bias pin is used, the current consumption in the power-saving mode will be approximately 700μA. Even in the power-saving mode, a 5V regulator voltage is output. Also, in the power-saving mode, the IC is in a short break state. (lower-side shorted)

9. Power Supply Stabilization

This IC generates a large output current, and employs a switching drive method, so the power supply line level can be disturbed easily. For this reason, it is necessary to connect a capacitor (electrolytic) of sufficient capacitance between the V_{CC} pin and ground to ensure a stable voltage. Connect the ground side of the capacitor to the PGND pin, which is the power ground, as close as possible to the pin. If it is not possible to connect a capacitor of sufficiently large capacitance close to the pin, connect a ceramic capacitor of approximately 0.1μF to the vicinity of the pin.
If diodes are inserted in the power supply line to prevent IC destruction resulting from reverse-connecting the power supply, the power supply lines are even more easily disrupted. And even larger capacitor is required.

10. VREG Stabilization

To stabilize the VREG voltage, which is the power supply for the control circuit, connect a capacitor of 0.1μF or larger. Connect the ground of this capacitor as close as possible to the control block ground (SGND pin) of the IC.

11. Charge pump Circuit

The voltage is stepped-up by the charge pump circuit, causing the gate voltage of the upper-side output FET to be generated. The voltage is stepped-up by capacitor CP connected between pins CP1 and CP2, causing charge to accumulate in capacitor CG connected between pins VG and V_{CC}. The capacitance of CP and CG must always satisfy the following relationship.

$$CG \geq 4 \times CP$$

Charging and discharging of capacitor CP take place based on a frequency of 100kHz. When the capacitance of capacitor CP is large, the current supply capability of power supply VG will increase. However, if the capacitance is too large, the charging and discharging operations will be insufficient. The larger the capacitance of capacitor CG, the more stable voltage VG will become. However, if the capacitance is made too large, the period during which voltage VG is generated when the power is switched ON will become long, so caution is necessary.
The capacitance settings of CP and CG should be the following.

$CP = 0.01\mu F$
$CG = 0.1\mu F$

12. Difference point of LV8829LFQA and LV8827LFQA

This difference that IC is the more following compared with LV8827LFQA exists.

	LV8829LFQA	LV8827LFQA
When Duty=0% of PWM input is detected	Synchronous rectification OFF (Free run)	Short brake
At the low frequency number of PWM input (About 7.5kHz under)	Synchronous rectification OFF	Like synchronous rectification ON
At low ON Duty of the PWM input (ex. frequency: 20kHz, ON Duty: 3% under)	Synchronous rectification OFF	Like synchronous rectification ON
Backflow current detecting function	It is. (At detection -> Synchronous rectification OFF)	non

13. Metal part at the rear of the IC

The metal part at the rear of the IC (exposed die-pad) constitutes the sub ground of the IC, so connect it to the control ground (SGND pin) and power ground pin (PGND) at points close to the IC.

14. Notes on Using the IC

This IC performs synchronous rectification in order to achieve high-efficiency drive.

The synchronous rectification operation reduces the output transistor loss so it has the effect of reducing heat generation and improving efficiency.

However, the synchronous rectification operation may cause the supply voltage to rise depending on the conditions under which the IC is used, such as:

- When the output duty ratio has suddenly decreased
- When the PWM input frequency is low, etc.

Protective measures must be taken to ensure that the maximum ratings are not exceeded even when the supply voltage has risen. These measures include:

- Appropriate selection of the capacitance of the capacitor inserted between the power supply and the ground
- Insertion of a zener diode between the power supply and the ground