To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

EOL announced Product

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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EOL announced product

RENESAS

MOS FIELD EFFECT TRANSISTOR
2SJ243

P-CHANNEL MOS FET
FOR SWITCHING

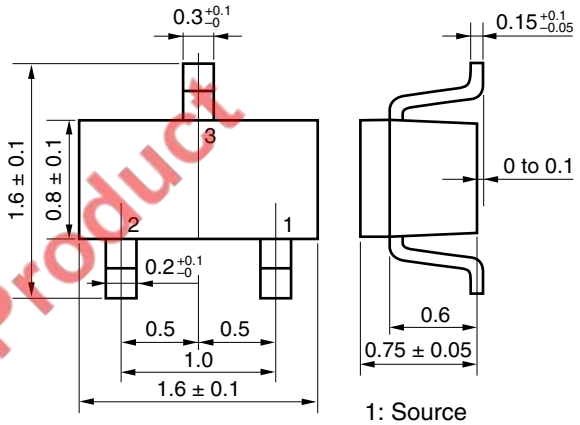
DESCRIPTION

The 2SJ243 is a P-channel vertical type MOS FET that is driven at 2.5 V.

Because this MOS FET can be driven on a low voltage and because it is not necessary to consider the drive current, the 2SJ243 is ideal for driving the actuator of power-saving systems, such as VCR cameras and headphone stereo systems.

Moreover, the 2SJ243 is housed in a super small mini-mold package so that it can help increase the mounting density on the printed circuit board and lower the mounting cost, contributing to miniaturization of the application systems.

★ PACKAGE DRAWING (Unit: mm)



1: Source
2: Gate
3: Drain

FEATURES

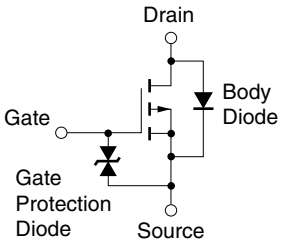
- Small mounting area: about 60% of the conventional mini-mold package (SC-70)
- Can be directly driven by 3-V IC
- Can be automatically mounted

★ ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ243	SC-75 (USM)

Marking: A1

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	−30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓ 7.0	V
Drain Current (DC)	$I_{D(DC)}$	∓ 100	mA
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓ 200	mA
Total Power Dissipation Note2	P_T	200	mW
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Notes 1. PW ≤ 10 ms, Duty Cycle ≤ 50%

2. Mounted on ceramic substrate of 3.0 cm^2 x 0.64 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Printed in Japan

The mark ★ shows major revised points.

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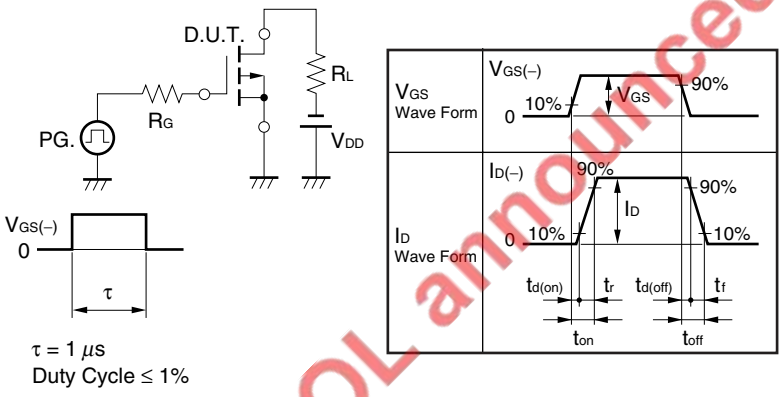
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓ 5.0 V, V_{DS} = 0 V		∓ 0.1	∓ 3.0	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –3.0 V, I_D = –10 μA	–1.6	–1.9	–2.3	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = –3.0 V, I_D = –10 mA	20	30		mS
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –2.5 V, I_D = –1.0 mA		55	100	Ω
	$R_{DS(on)2}$	V_{GS} = –4.0 V, I_D = –10 mA		20	25	Ω
Input Capacitance	C_{iss}	V_{DS} = –5.0 V		16		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		13		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		2.0		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –5.0 V, I_D = –10 mA		10		ns
Rise Time	t_r	V_{GS} = –5.0 V		40		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		130		ns
Fall Time	t_f			80		ns

Note Pulsed: PW ≤ 350 μs, Duty Cycle 2%

★ TEST CIRCUIT SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

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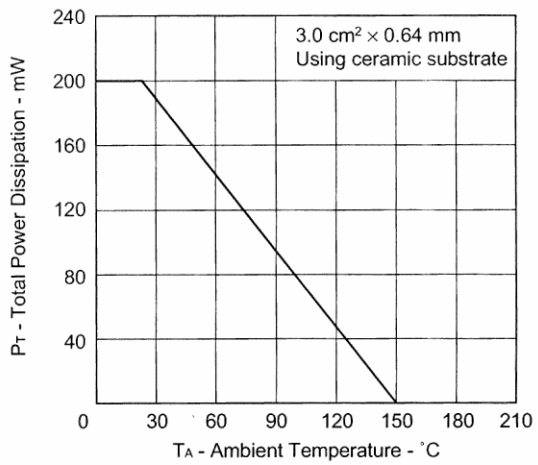
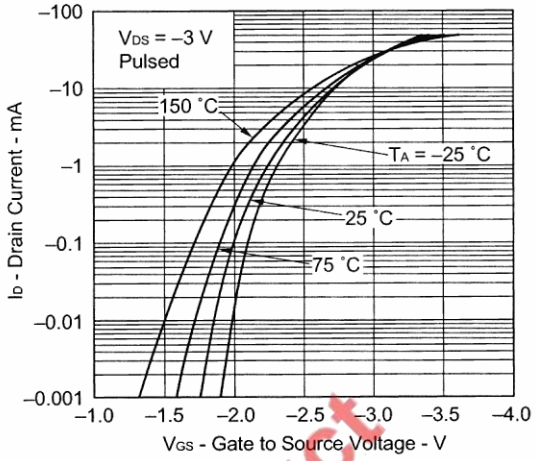
TYPICAL CHARACTERISTICS (T_A = 25°C)

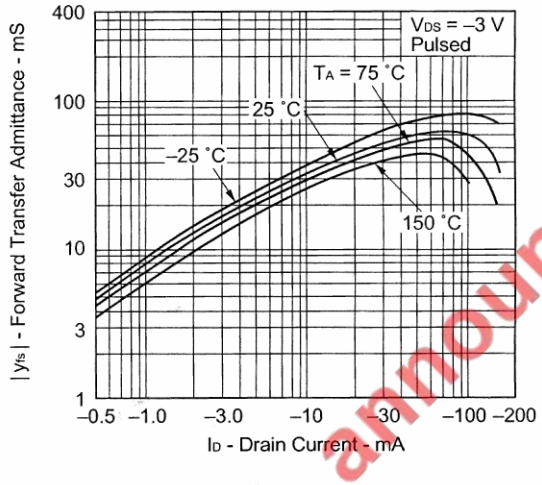
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



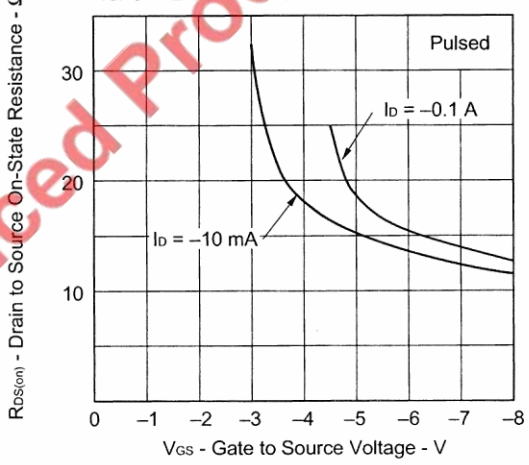
TRANSFER CHARACTERISTICS



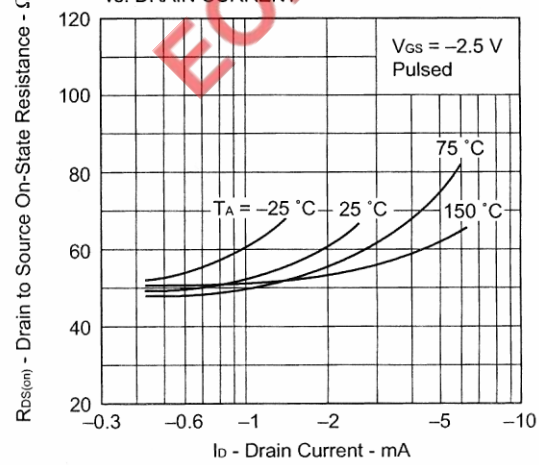
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



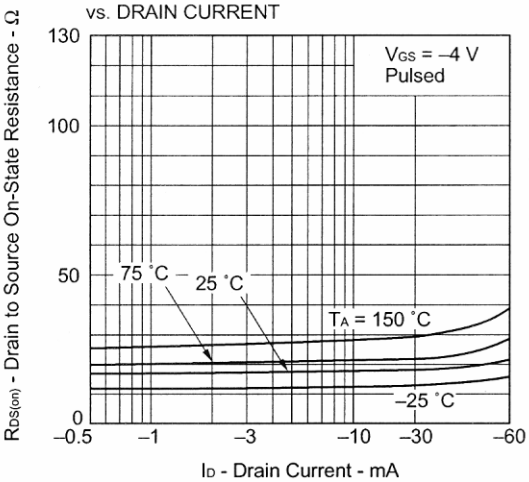
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



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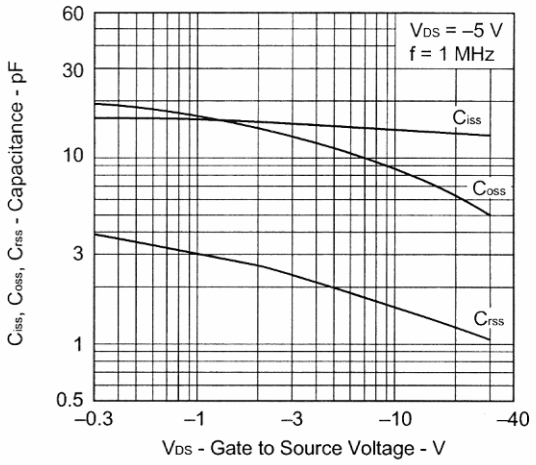
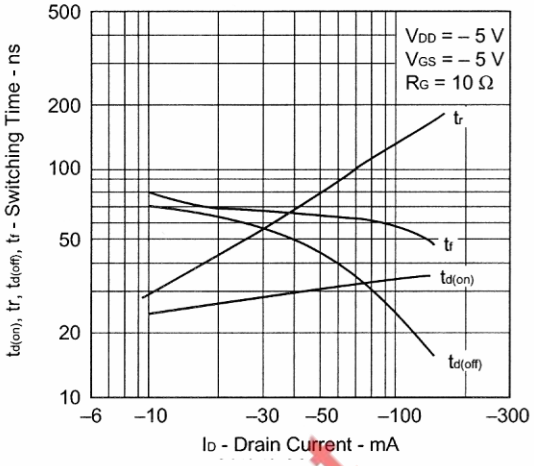
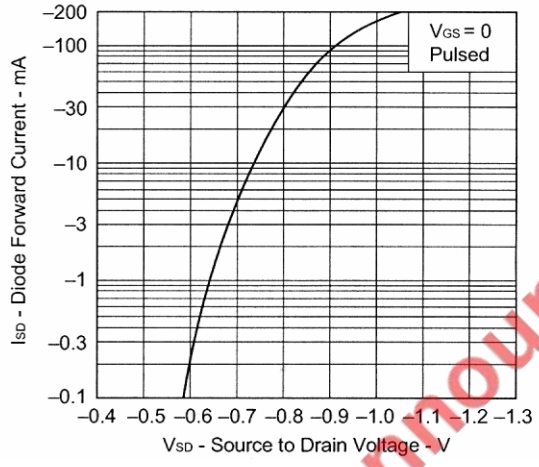
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



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