

Product Summary

V _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C
-8V	5.7mΩ@V _{GS} = -4.5V	-13.2A

Description

This 3rd generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal R_{DS(ON)} per footprint area.

Applications

- DC-DC Converters
- Battery Management
- Load Switch

Features

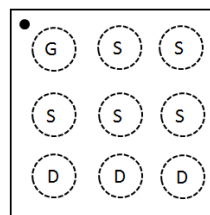
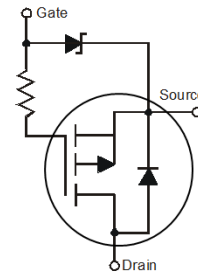
- LD-MOS Technology with the Lowest Figure of Merit:
- R_{DS(ON)} = 5.7mΩ to Minimize On-State Losses
- Q_g = 8.2nC for Ultra-Fast Switching
- V_{GS(TH)} = -0.6V Typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm × 1.5mm
- Height = 0.60mm for Low Profile
- ESD Protection of Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.**
<https://www.diodes.com/quality/product-definitions/>

Mechanical Data

- Case: U-WLB1515-9
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal: Finish - SnAgCu. Solderable per MIL-STD-202 Method 208 @1
- UBM Size: 245μm
- Terminal Connections: See Diagram Below
- Weight: 0.0018 grams (Approximate)



U-WLB1515-9 (Type F)


 Top-View
Pin Configuration


Equivalent Circuit

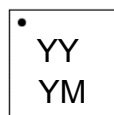
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP1008UCB9-7	U-WLB1515-9 (Type F)	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

U-WLB1515-9 (Type F)



YY = Product Type Marking Code
 YM = Date Code Marking
 Y or \bar{Y} = Year (ex: G = 2019)
 M or \bar{M} = Month (ex: 9 = September)

Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	G	H	I	J	K	L	M	N	O	P	R	S
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	-8	V
Gate-Source Voltage			V _{GSS}	-6	V
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	T _A = +25°C	I _D	-9.8	A
		T _A = +70°C		-7.8	
Continuous Drain Current (Note 6) V _{GS} = -4.5V	Steady State	T _A = +25°C	I _D	-13.2	A
		T _A = +70°C		-10.5	
Pulsed Drain Current (Pulse Duration 10μs, Duty Cycle ≤1%)			I _{DM}	-80	A
Continuous Source Pin Current (Note 6)			I _S	-1.8	A
Pulsed Source Pin Current (Pulse Duration 10μs, Duty Cycle ≤1%)			I _{SM}	-80	A
Continuous Gate Current			I _G	-0.8	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P _D	0.84	W
Total Power Dissipation (Note 6)	P _D	1.53	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	151.4	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	R _{θJA}	82	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-8	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current @T _C = +25°C	I _{DSS}	—	—	-1	μA	V _{DS} = -6.4V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	-100	nA	V _{GS} = -6.0V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	-0.4	-0.6	-1.1	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	4.7	5.7	mΩ	V _{GS} = -4.5V, I _D = -2A
			6.3	8.2		V _{GS} = -3.0V, I _D = -2A
			6.8	9.1		V _{GS} = -2.5V, I _D = -2A
Diode Forward Voltage (Note 6)	V _{SD}	—	-0.63	-1	V	V _{GS} = 0V, I _S = -2A
Reverse Recovery Charge	Q _{RR}	—	9.2	—	nC	V _{DD} = -5V, I _F = -2A, di/dt = 200A/μs
Reverse Recovery Time	t _{RR}	—	25	—	ns	
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	900	—	pF	V _{DS} = -4V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	730	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	158	—	pF	
Series Gate Resistance	R _G	—	21.4	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge	Q _g	—	8.2	—	nC	V _{GS} = -4.5V, V _{DS} = -4V, I _D = -2A
Gate-Source Charge	Q _{gs}	—	0.9	—	nC	
Gate-Drain Charge	Q _{gd}	—	1.0	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	20.0	—	ns	V _{DD} = -4V, V _{GS} = -4.5V, I _{DS} = -2A, R _G = 10Ω
Turn-On Rise Time	t _R	—	5.8	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	99.6	—	ns	
Turn-Off Fall Time	t _F	—	36.4	—	ns	

- Notes:
5. Device mounted on FR-4 PCB with minimum recommended pad layout.
 6. Device mounted on FR-4 material with 1-inch² (6.45cm²), 2oz (0.071mm thick) Cu.
 7. Short duration pulse test used to minimize self-heating effect.
 8. Guaranteed by design. Not subject to production testing.

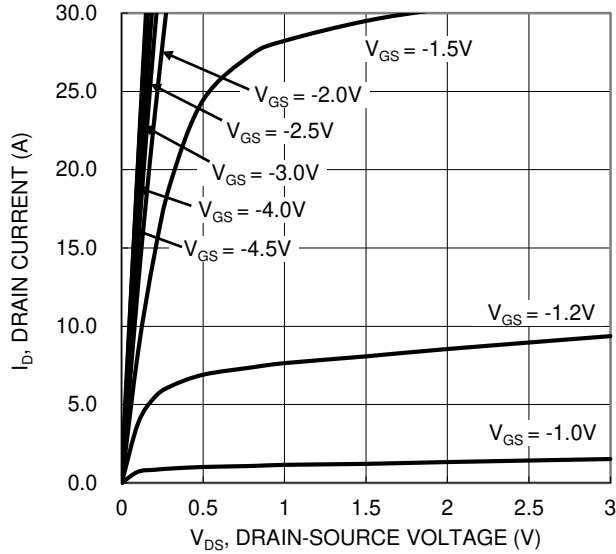


Figure 1. Typical Output Characteristic

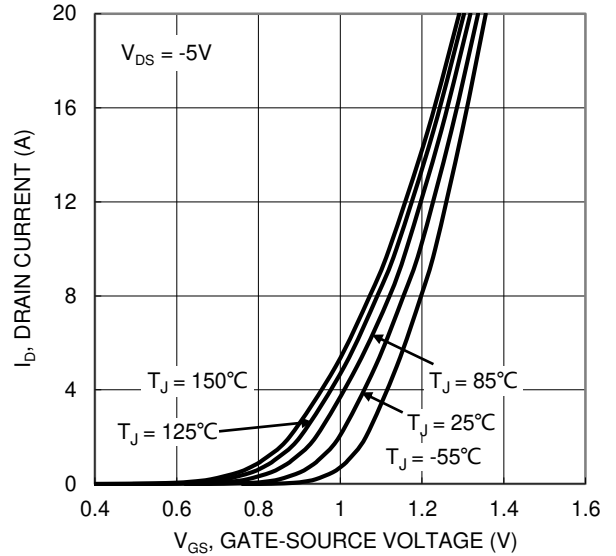


Figure 2. Typical Transfer Characteristic

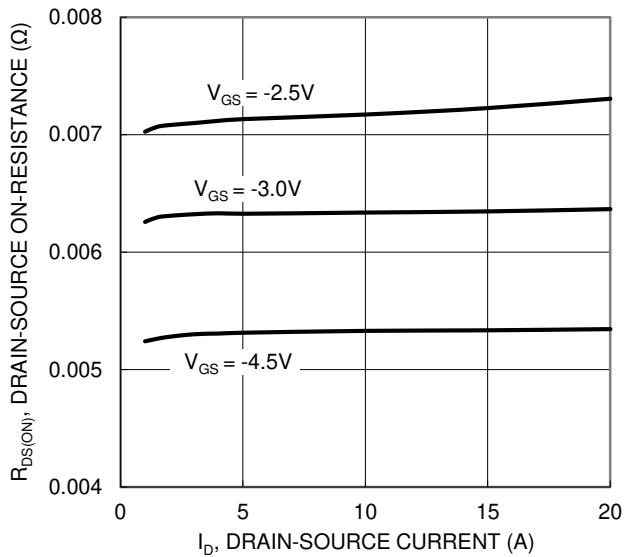


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

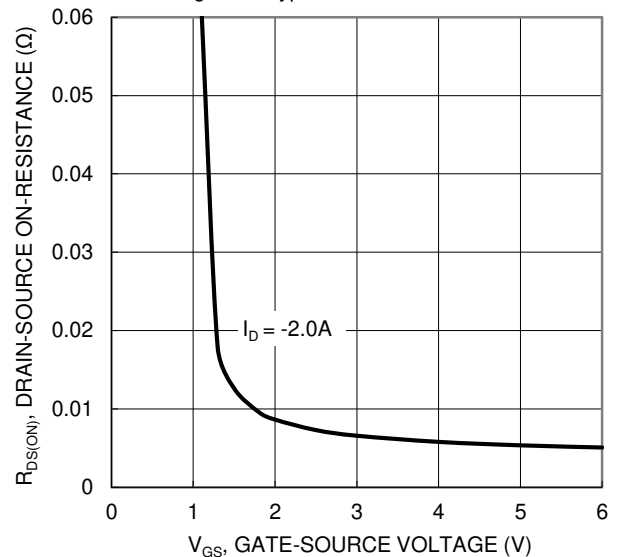


Figure 4. Typical Transfer Characteristic

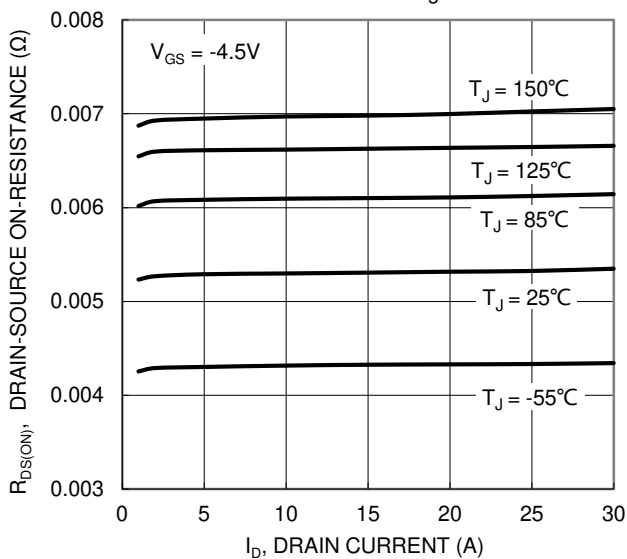


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

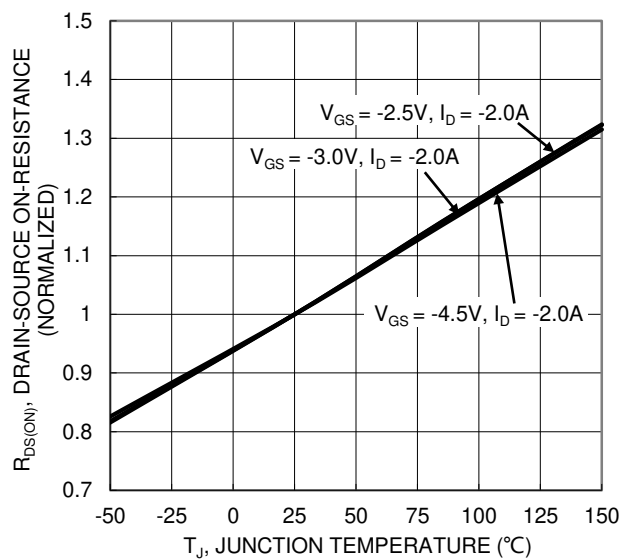


Figure 6. On-Resistance Variation with Junction Temperature

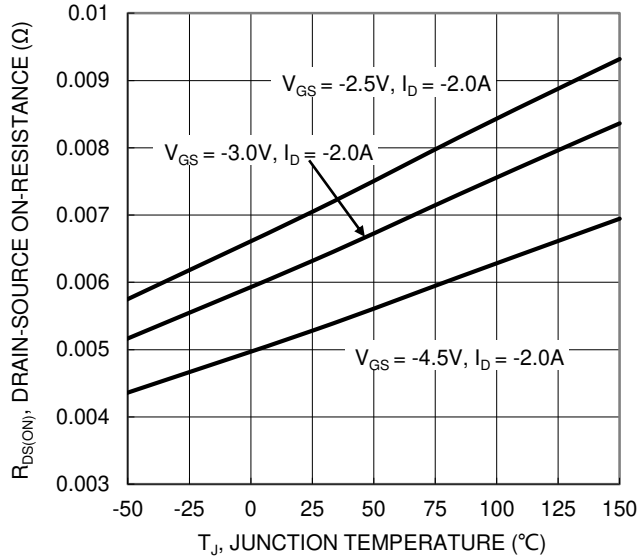


Figure 7. On-Resistance Variation with Junction Temperature

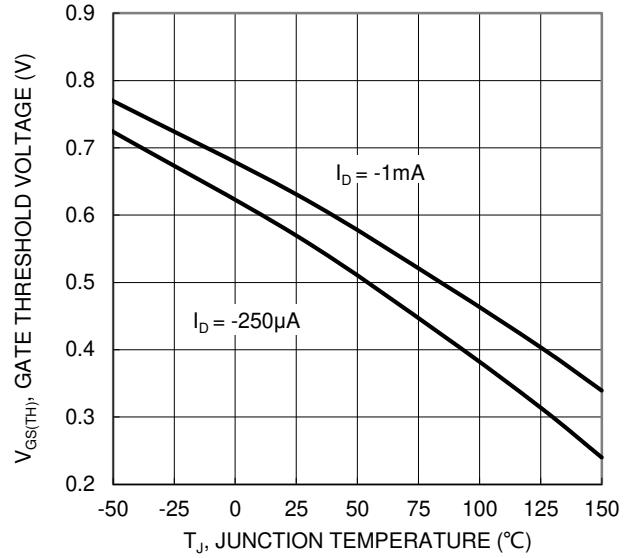


Figure 8. Gate Threshold Variation vs. Junction Temperature

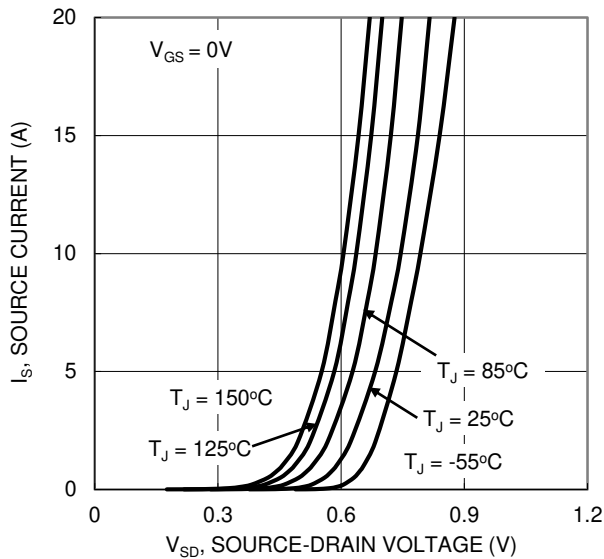


Figure 9. Diode Forward Voltage vs. Current

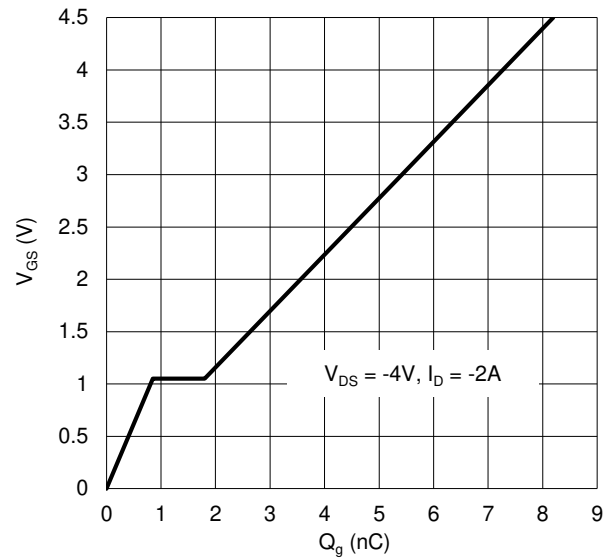


Figure 10. Gate Charge

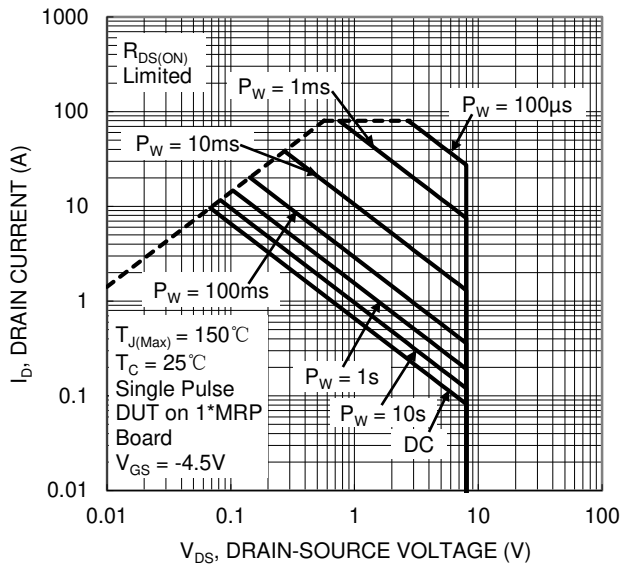


Figure 11. SOA, Safe Operation Area

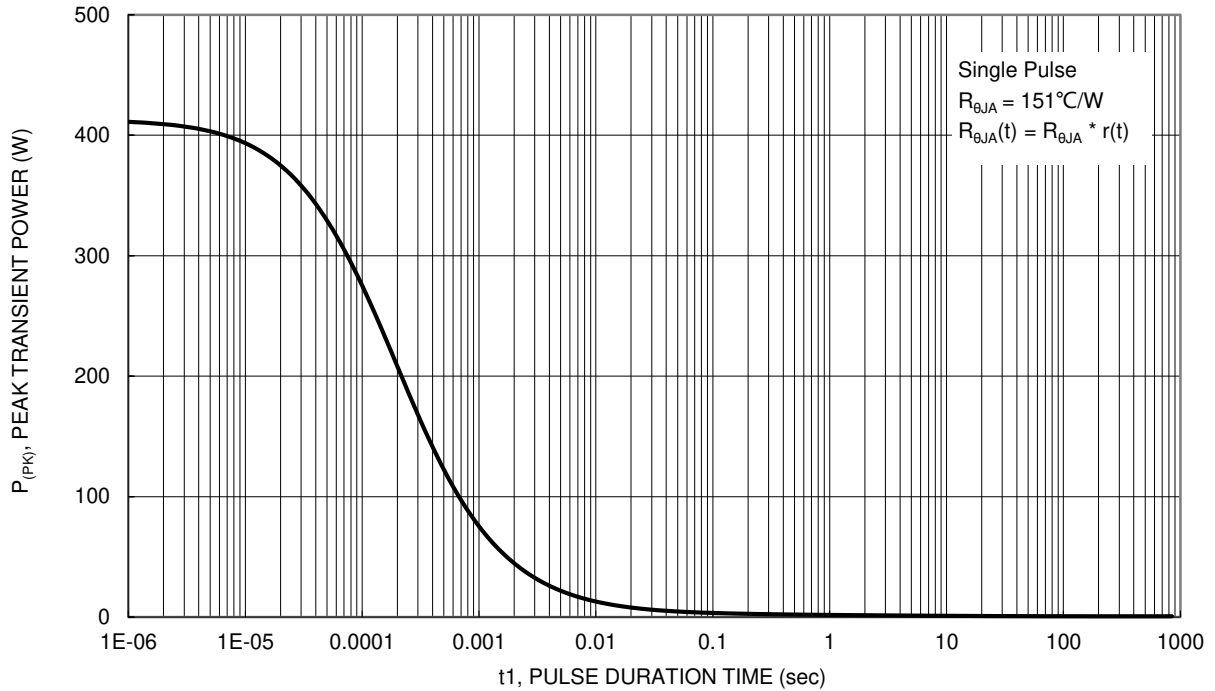


Figure 12. Single Pulse Maximum Power Dissipation

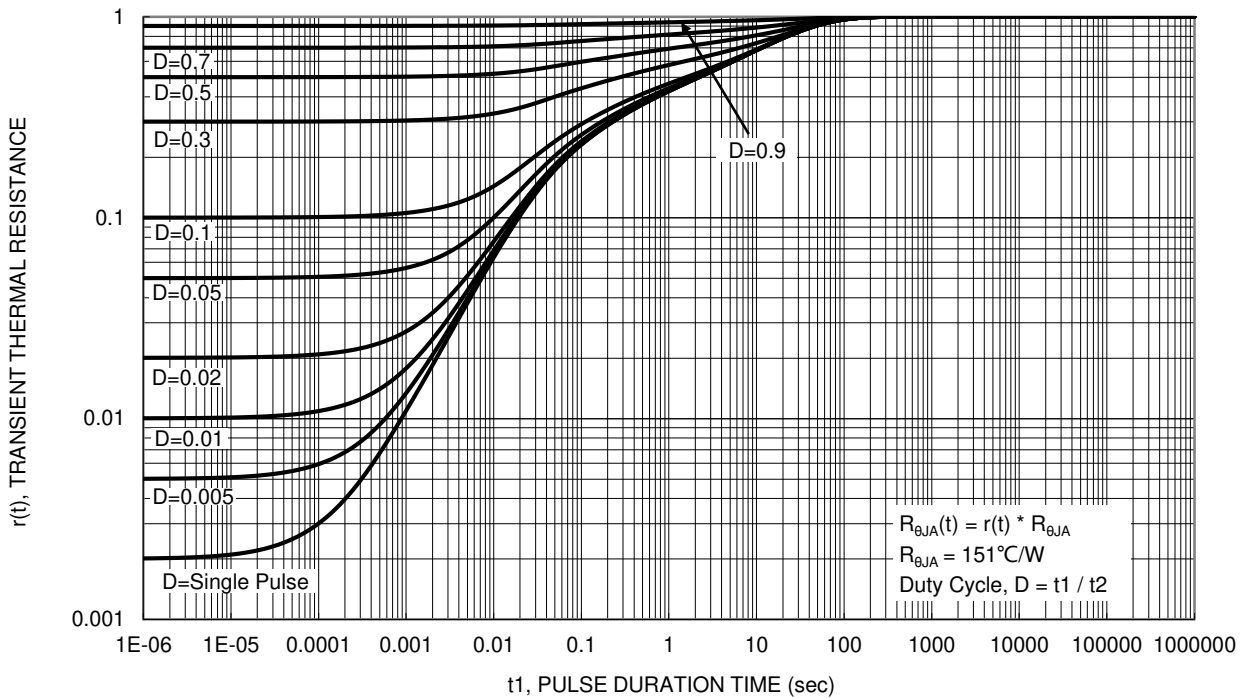
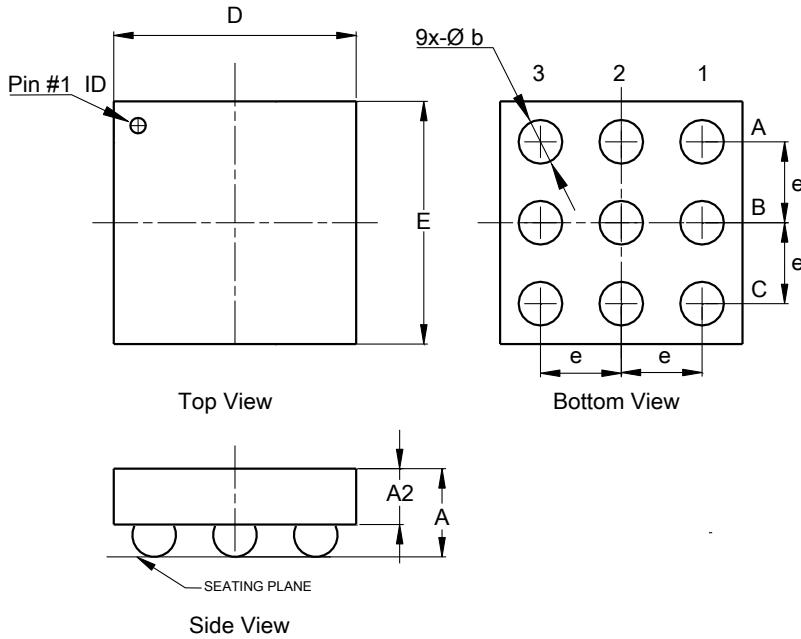


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-WLB1515-9 (Type F)

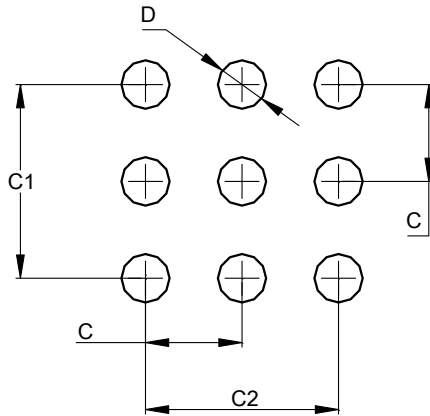


U-WLB1515-9 (Type F)			
Dim	Min	Max	Typ
A	--	0.60	--
A2	0.31	0.36	0.335
b	0.220	0.320	0.270
D	1.48	1.53	1.505
E	1.48	1.53	1.505
e	--	--	0.50
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-WLB1515-9 (Type F)



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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