TS4974

1W differential audio power amplifier with up/down digital volume control pins

Features

- Operates from V_{CC}= 2.5 V to 5.5 V
- Zero pop & click
- 1 W output power @ V_{CC} = 5 V, THD = 1%, F = 1 kHz, with 8 Ωload
- Ultra-low consumption in standby mode (2 µA max.)
- 85 dB PSRR @ 217Hz
- 16-step digital volume control
- Two discrete up and down volume control pins
- Gain range from -33 dB to + 12 dB
- Integrated debouncing system
- Ultra-fast start-up time: 15 ms typ.
- DFN10 3x3 mm (pitch 0.5)

Applications

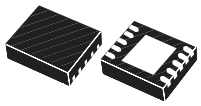
- Mobile phones (cellular / cordless)
- PDAs
- Laptop/notebook computers
- Portable audio devices

Description

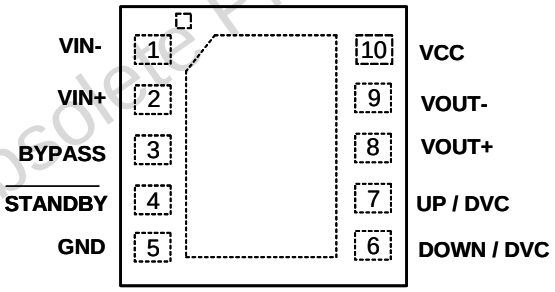
At 3.3 V, the TS4974 is a dual power audio amplifier capable of delivering 380 mW of continuous RMS output power into a 8 Ω bridged-tied loads with 1% THD+N. An external standby mode control reduces the supply current to less than 2 µA. An internal over-temperature shutdown protection is provided.

The TS4974 has been designed for high quality audio applications such as mobile phones and minimizes the number of external components necessary.

DFN10 (3x3)



Pin connections (top view)



The TS4974 features 16-step digital volume control through two discrete Up and Down control pins. The start-up gain is internally fixed to -12 dB. An integrated debounce system prevents voltage spikes on the UP/DOWN pins during volume control mode from being taken into account during a debounce time of 10 ms (typ).

Contents

1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
P_d	Power dissipation	Internally limited(4)	
ESD	Human body model	2	kV
ESD	Machine model	200	V
Latch-up	Latch-up immunity	200	mA
	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V.
3. Device is protected in case of over temperature by a thermal shutdown active @ 150° C.
4. Exceeding the power derating curves during a long period, may provoke abnormal operation.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{STBY}	Standby voltage input: Device ON Device OFF	 $1.5 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
$V_{U/D}$	Volume control UP/DOWN voltage input: UP/DOWN mode ON UP/DOWN mode OFF	 $0 \leq V_{U/D} \leq 0.3xV_{CC,}$ $0.7xV_{CC} \leq V_{U/D} \leq V_{CC}$	V
R_L	Load resistor	≥ 8	Ω
T_{SD}	Thermal shutdown temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (1)	80	°C/W

1. With heat sink surface = 125 mm^2.

2 Typical application schematics

Figure 1. Typical application schematics for the TS4974

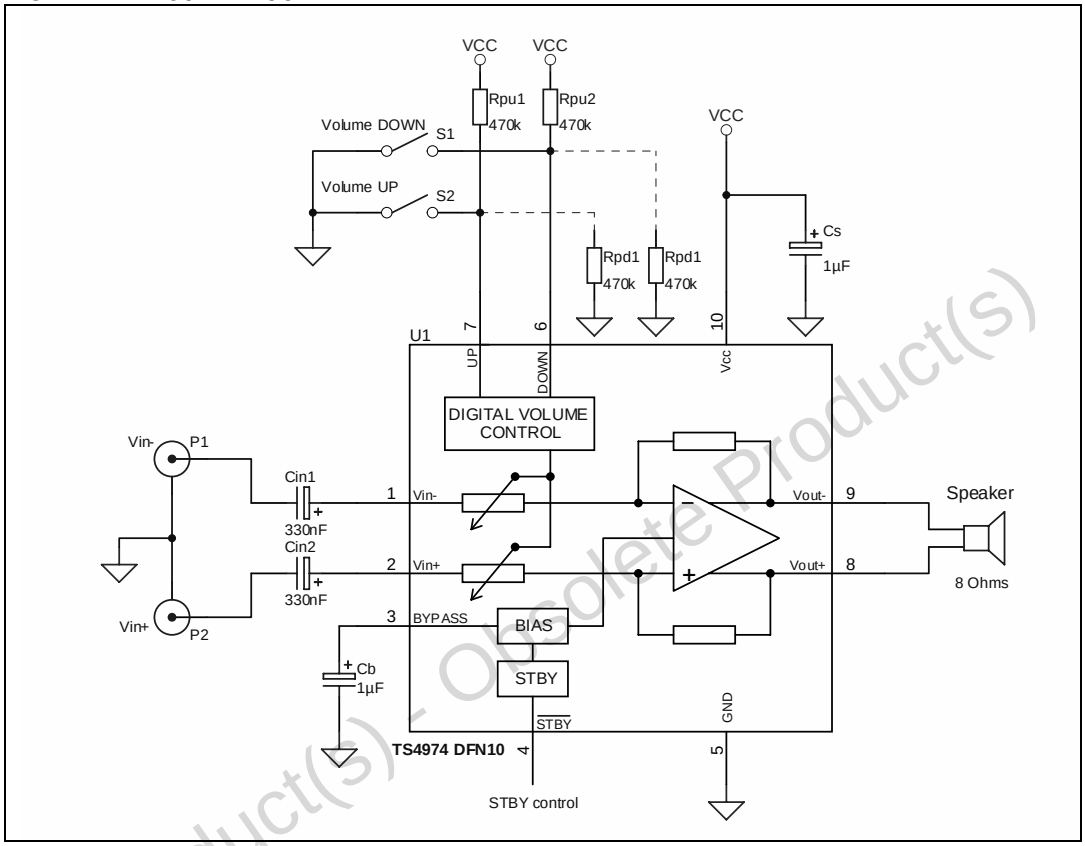


Table 3. External component descriptions

Components	Functional description
Rpu1, Rpu2 Rpd1, Rpd2	Pair of pull-up (Rpu1, Rpu2) or pull down (Rpd1, Rpd2) resistors that are connected to the digital volume control pins UP/DVC and DOWN/DVC. See *Section 4.9: Volume setting on page 20*.
C_{IN}	Input coupling capacitors that block the DC voltage at the amplifier input terminal. They form together with the amplifier's differential input impedance Z_{IN} a first order high pass filter with a -3dB cut-off frequency ($f_{cut-off} = 1 / (2 \times \pi \times Z_{IN} \times C_{IN})$). See *Section 4.2: Low frequency response on page 16*.
C_S	Supply bypass capacitor that provides power supply filtering. See *Section 4.4: Decoupling of the circuit on page 19*.
C_B	Bypass pin capacitor that provides half supply filtering. See *Section 4.4: Decoupling of the circuit on page 19*.

3 Electrical characteristics

Table 4. V_{CC} = +5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current, no input signal, no load		3.2	3.85	mA
I_{STBY}	Standby current No input signal, V_{STBY} = GND, R_L = 8Ω		300	2000	nA
$I_{U/D}$	Volume control UP/DOWN current $0 \leq V_{U/D} \leq 0.3\ V_{CC}$		10		µA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω, G=0 dB, floating inputs		5	20	mV
P_o	Output power THD = 1% max, f = 1 kHz, R_L = 8Ω	0.8	1		W
THD + N	Total harmonic distortion + noise Po = 500 mW rms, 20 Hz < F < 20 kHz, R_L = 8 Ω, G = 0 dB, C_b= 1 µF, C_{in} = 330 nF		0.5		%
PSRR	Power supply rejection ratio(1) F = 217Hz, RL = 8Ω) V_{ripple} = 200 mV_{pp}, input grounded, C_b=1 µF, C_{in}=330 nF, G=0 dB		85		dB
CMRR	Common mode rejection ratio(2) F = 217 Hz, R_L = 8 Ω, V_{incm} = 200 mV_{pp}, C_b = 1 µF, C_{in}= 330 nF, G= 0 dB		61		dB
SNR	Signal-to-noise ratio (weighted A, G= 0 dB) (R_L = 8 Ω, THD + N ≤ 0.5%, 20 Hz < F < 20 kHz)		100		dB
Gs	Start up gain (when powered up from V_{CC} - see *Section 4.9: Volume setting on page 20*)		-12		dB
G	Gain range	-33		+12	dB
Gain step size			3		dB
Gain accuracy	Tolerance between theoretical gain set and real gain	-1		+1	dB
t_{wu}	Wake-up time C_b=1 µF		10		ms
V_N	Output voltage noise F = 20 Hz to 20 kHz, R_L = 8 Ω, G= 0 dB Unweighted A-weighted		 21 14		μV_{RMS}
Z_{in}	Differential input impedance	48	60	75	kΩ
$t_{debounce}$	Debouncing time		10		ms
$t_{autorepeat}$	Time between volume changes		220		ms
t_{range}	During autorepeat mode, necessary time to cover the whole gain range		3200		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} @ F = 217 Hz.
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vincm)).

Table 5. V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3.0	3.6	mA
I_{STBY}	Standby current No input signal, V_{STBY} = GND, R_L = 8 Ω		260	2000	nA
$I_{U/D}$	Volume control UP/DOWN current $0 \leq V_{U/D} \leq 0.3\ V_{CC}$		10		µA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω, G= 0 dB, floating inputs		5	20	mV
P_o	Output power THD = 1% max, f = 1 kHz, R_L = 8 Ω	300	380		mW
THD + N	Total harmonic distortion + noise Po = 500 mW rms, 20 Hz < F < 20 kHz, R_L = 8 Ω, G = 0 dB, C_b= 1 µF, C_{in} = 330 nF		0.5		%
PSRR	Power supply rejection ratio(1) F = 217 Hz, R_L = 8 Ω V_{ripple} = 200 mV_{pp}, input grounded, C_b = 1 µF, C_{in}= 330 nF, G = 0 dB		85		dB
CMRR	Common mode rejection ratio(2) F = 217 Hz, R_L = 8 Ω, V_{incm} = 200 mV_{pp}, C_b = 1 µF, C_{in} = 330 nF, G = 0 dB		61		dB
SNR	Signal-to-noise ratio (weighted A, G= 0 dB) (R_L = 8 Ω, THD + N ≤ 0.5%, 20 Hz < F < 20 kHz)		100		dB
Gs	Start up gain (when powered up from V_{CC} - See *Section 4.9: Volume setting on page 20*)		-12		dB
G	Gain range	-33		+12	dB
Gain step size			3		dB
Gain accuracy	Tolerance between theoretical gain set and real gain	-1		+1	dB
t_{wu}	Wake-up time C_b= 1 µF		10		ms
V_N	Output voltage noise F = 20 Hz to 20 kHz, R_L = 8 Ω, G = 0 dB Unweighted A-weighted		 21 14		μV_{RMS}
Z_{in}	Differential input impedance	48	60	75	kΩ
$t_{debounce}$	Debouncing time		10		ms
$t_{autorepeat}$	Time between volume changes		220		ms
t_{range}	During autorepeat mode, necessary time to cover the whole gain range		3200		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} @ F = 217 Hz.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{incm})).

Table 6. V_{CC} = +2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.8	3.4	mA
I_{STBY}	Standby current No input signal, V_{STBY} = GND, R_L = 8 Ω		230	2000	nA
$I_{U/D}$	Volume control UP/DOWN current $0 \le V_{U/D} \le 0.3\ V_{CC}$		10		µA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω, G = 0 dB, floating inputs		5	20	mV
P_o	Output power THD = 1% max, f = 1 kHz, R_L = 8 Ω	200	250		mW
THD + N	Total harmonic distortion + noise Po = 500 mW rms, 20 Hz < F < 20 kHz, R_L = 8 Ω, G = 0 dB, C_b= 1 µF, C_{in}= 330 nF		0.5		%
PSRR	Power supply rejection ratio(1) F = 217 Hz, R_L = 8 Ω V_{ripple} = 200 mV_{pp}, input grounded, C_b= 1 µF, C_{in}= 330 nF, G= 0 dB		85		dB
CMRR	Common mode rejection ratio(2) F = 217 Hz, R_L = 8 Ω, V_{incm} = 200 mV_{pp}, C_b = 1 µF, C_{in}= 330 nF, G= 0 dB		61		dB
SNR	Signal-to-noise ratio (weighted A, G = 0 dB) (R_L = 8 Ω, THD + N ≤ 0.5%, 20 Hz < F < 20 kHz)		100		dB
Gs	Start up gain (when powered up from V_{CC} - see *Section 4.9: Volume setting on page 20*)		-12		dB
G	Gain range	-33		+12	dB
Gain step size			3		dB
Gain accuracy	Tolerance between theoretical gain set and real gain	-1		+1	dB
t_{wu}	Wake-up time C_b=1 µF		10		ms
V_N	Output voltage noise F = 20 Hz to 20 kHz, R_L = 8 Ω, G = 0 dB Unweighted A-weighted		 21 14		μV_{RMS}
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1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} @ F = 217 Hz.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{incm})).

Table 7. Output noise

	Unweighted filter 20 Hz to 20 kHz V_{out} (µA)	A-weighted filter V_{out} (µA)
G=+12 dB	22	15
G=+6 dB	21.5	14.5
G=0 dB	21	14
G=-12 dB	19	13
G=-33 dB	17	12

Figure 2. THD+N vs. output power

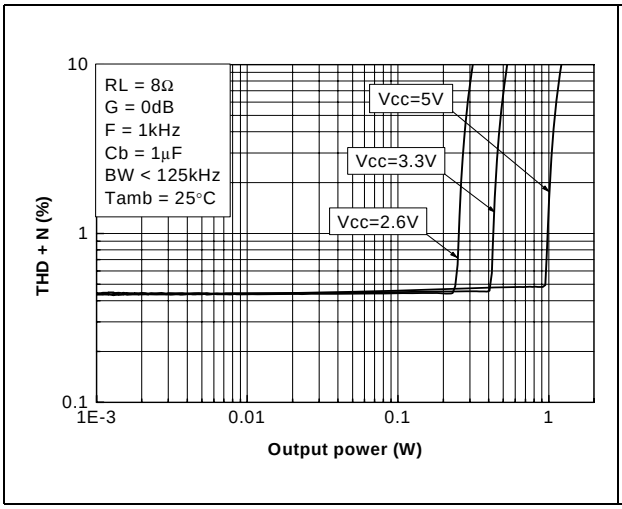


Figure 3. THD+N vs. output power

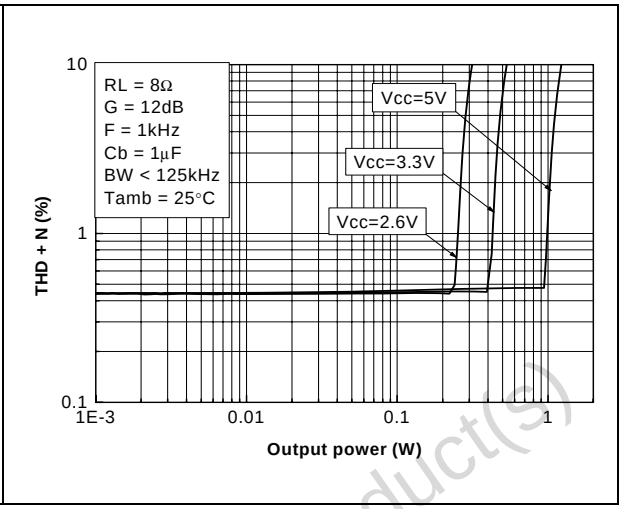


Figure 4. THD+N vs. output power

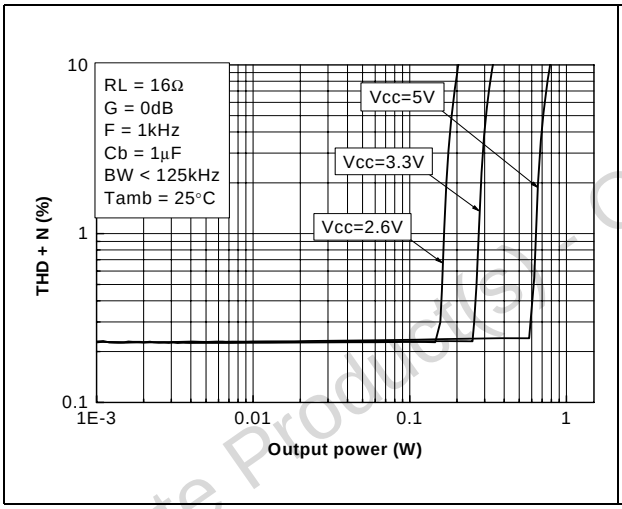


Figure 5. THD+N vs. output power

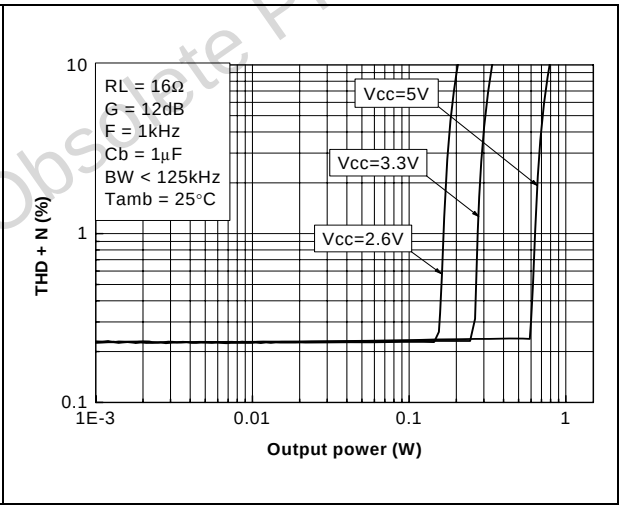


Figure 6. THD+N vs. output power

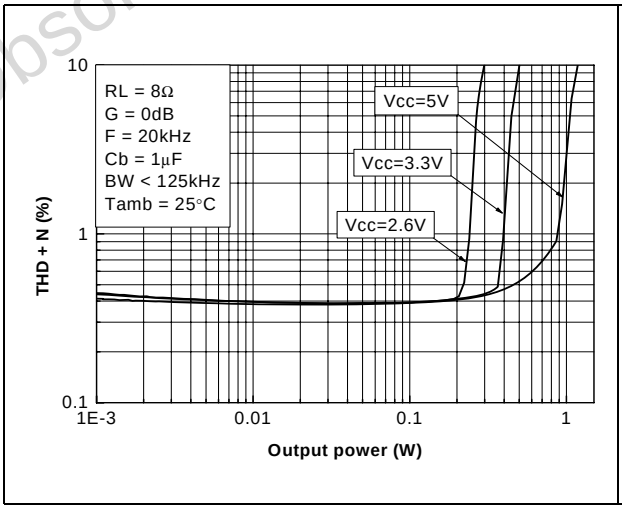


Figure 7. THD+N vs. output power

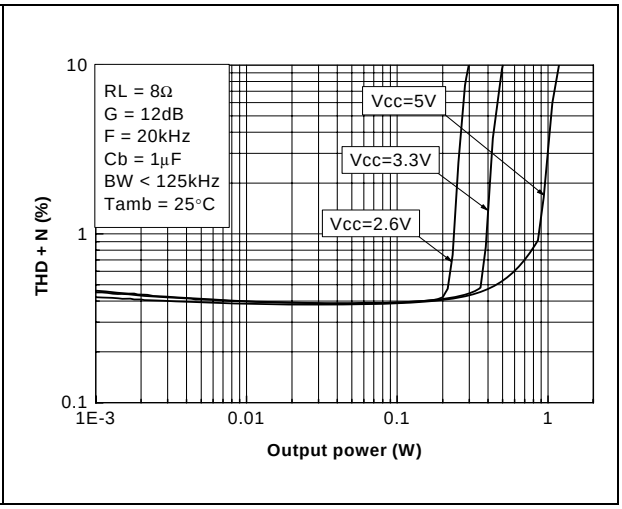


Figure 8. THD+N vs. output power

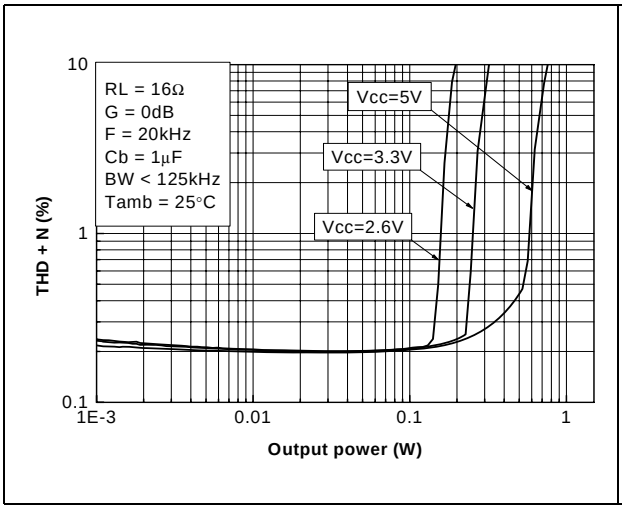


Figure 9. THD+N vs. output power

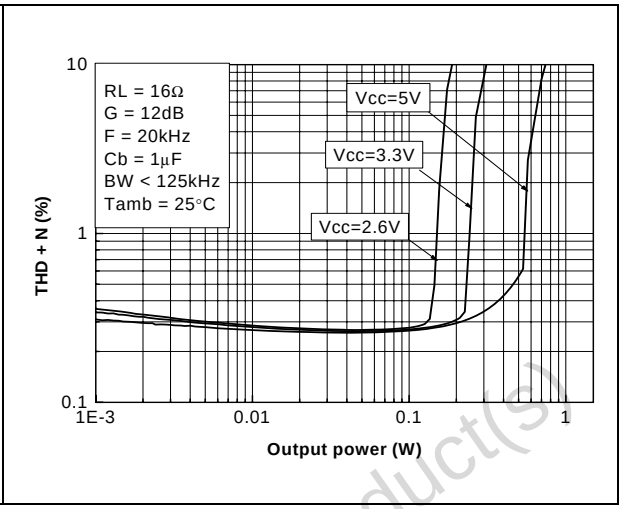


Figure 10. THD+N vs. frequency

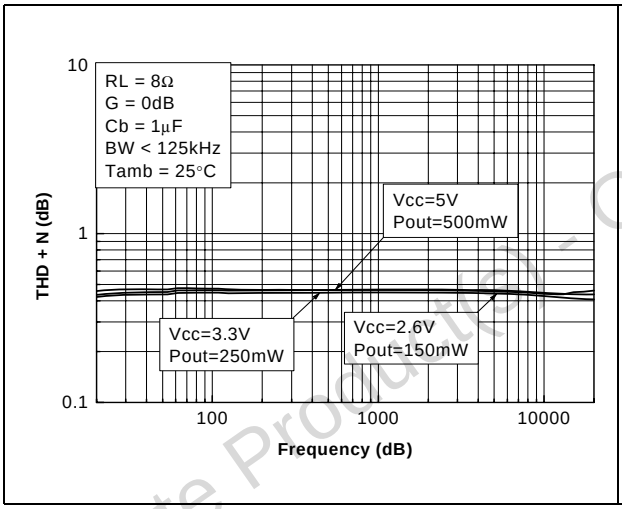


Figure 11. THD+N vs. frequency

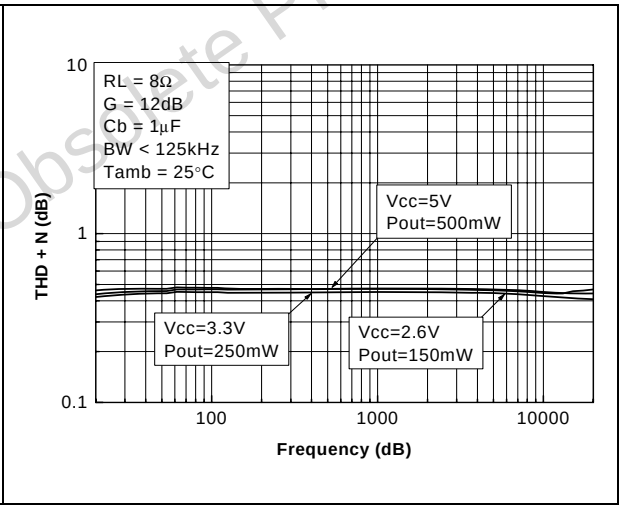


Figure 12. THD+N vs. frequency

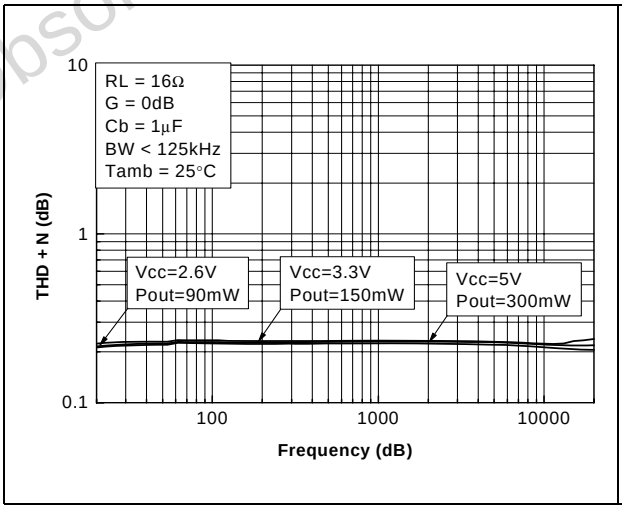


Figure 13. THD+N vs. frequency

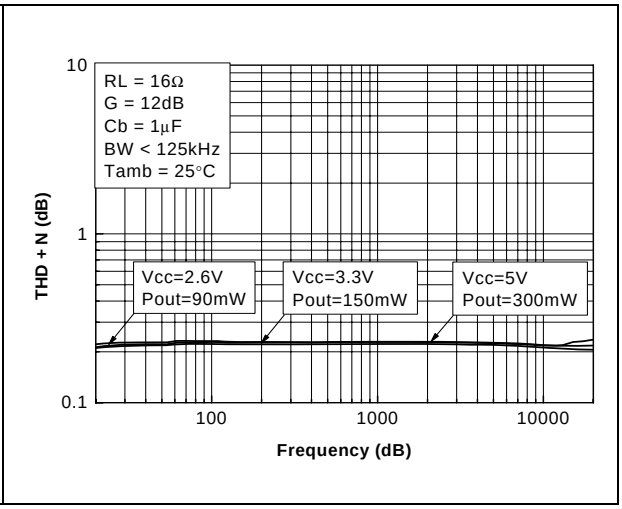


Figure 14. PSRR vs. frequency

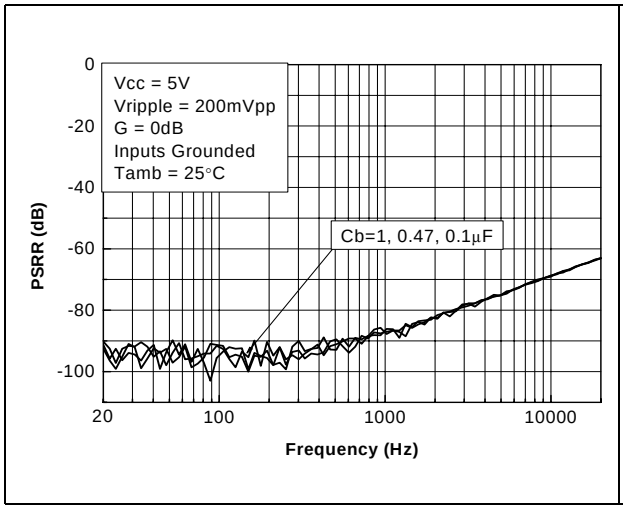


Figure 15. PSRR vs. frequency

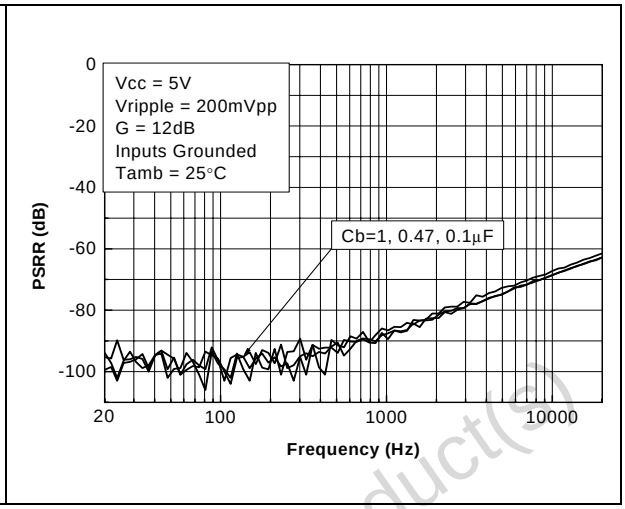


Figure 16. PSRR vs. frequency

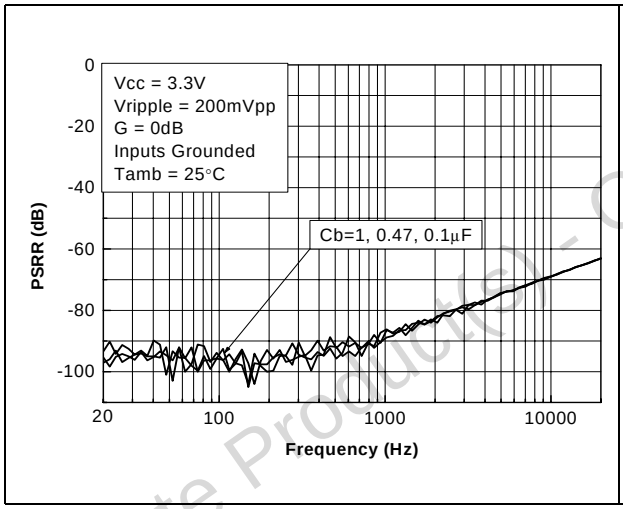


Figure 17. PSRR vs. frequency

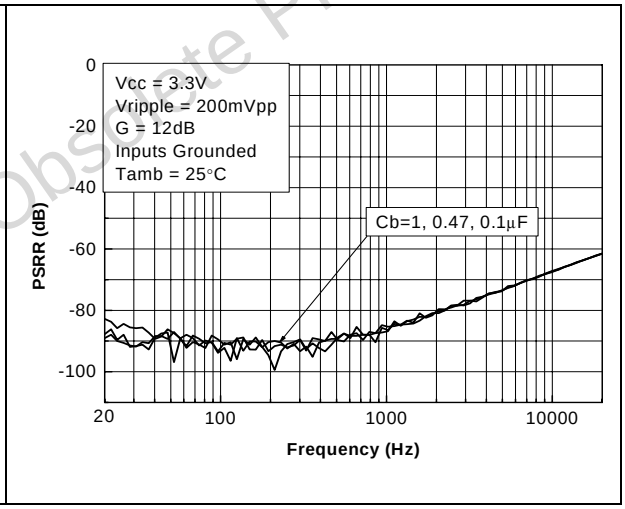


Figure 18. PSRR vs. frequency

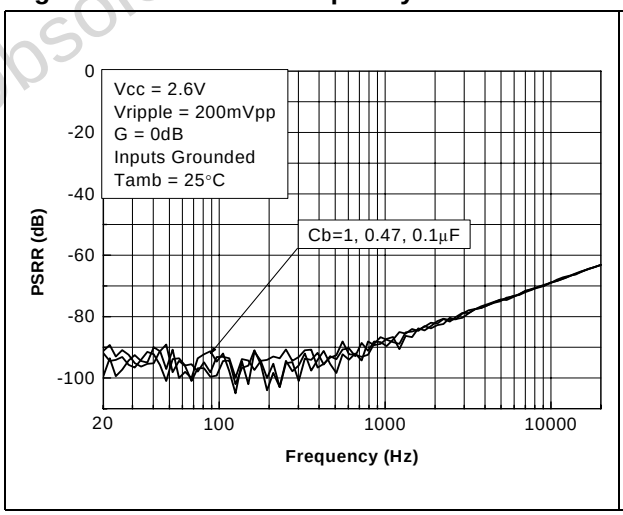


Figure 19. PSRR vs. frequency

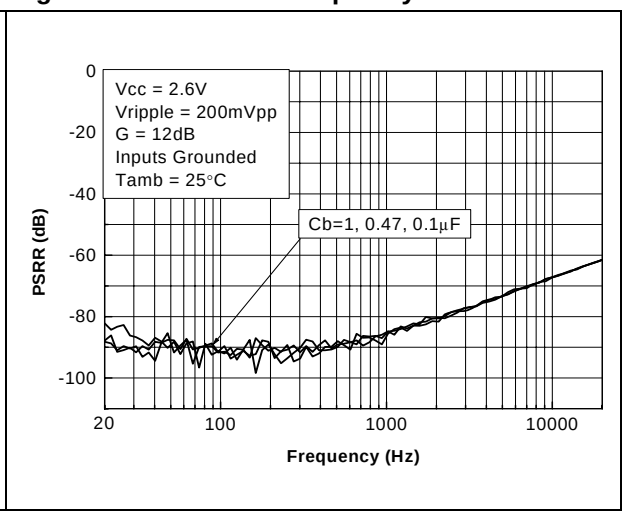


Figure 20. CMRR vs. frequency

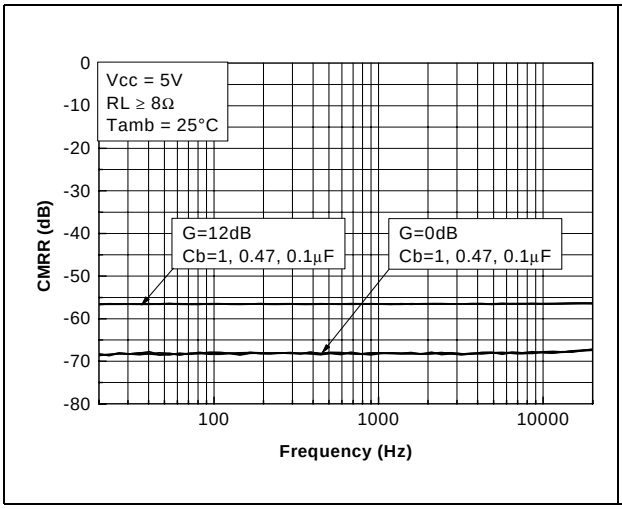


Figure 21. CMRR vs. frequency

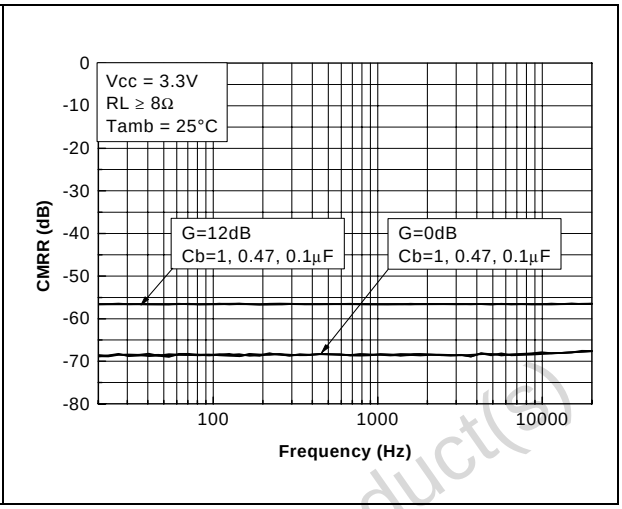


Figure 22. CMRR vs. frequency

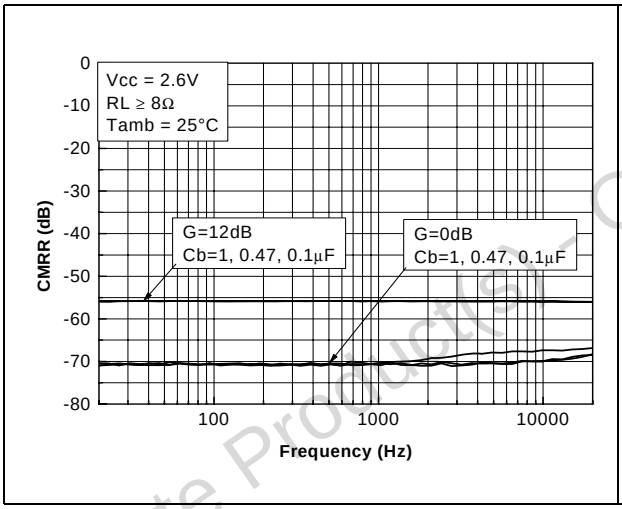


Figure 23. SNR vs. supply voltage

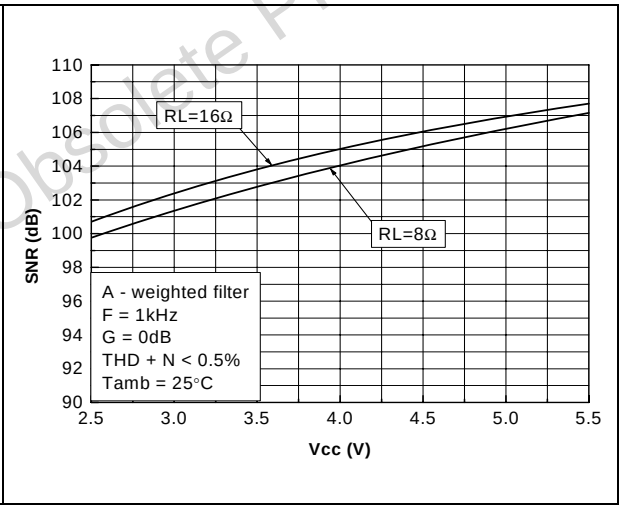


Figure 24. SNR vs. supply voltage

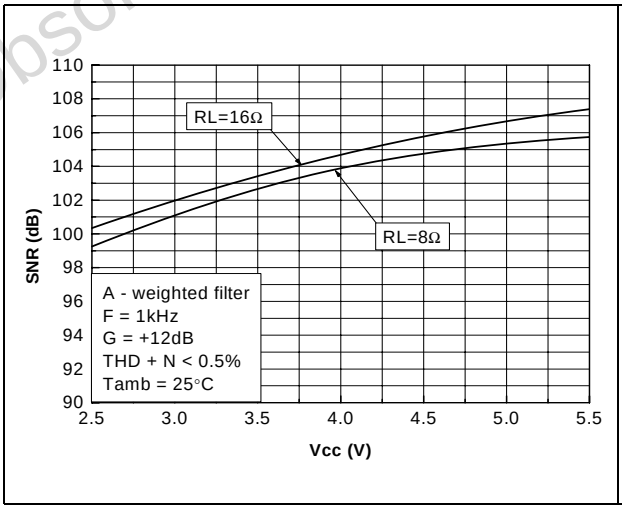


Figure 25. SNR vs. supply voltage

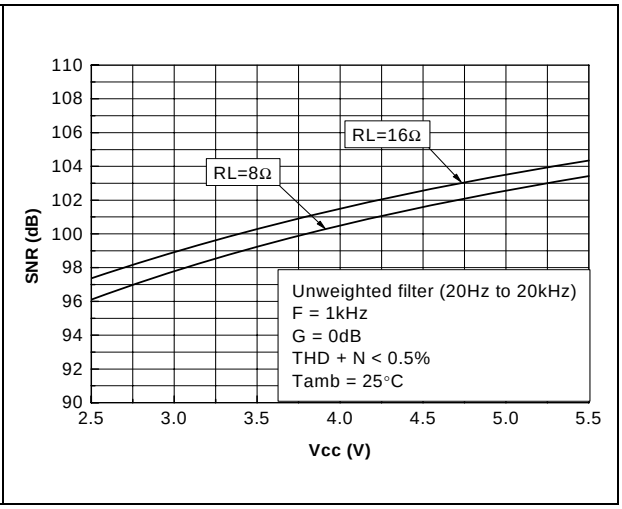


Figure 26. SNR vs. supply voltage

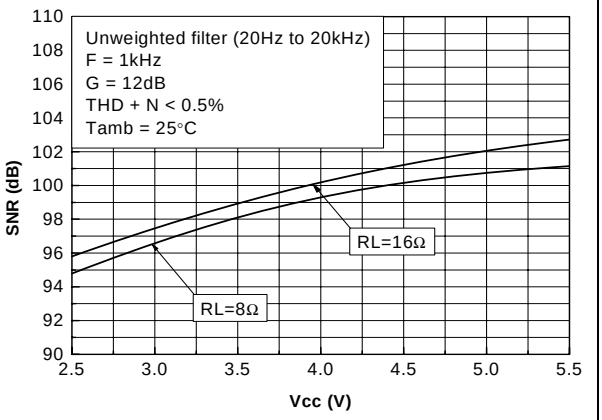


Figure 27. Output power vs. supply voltage

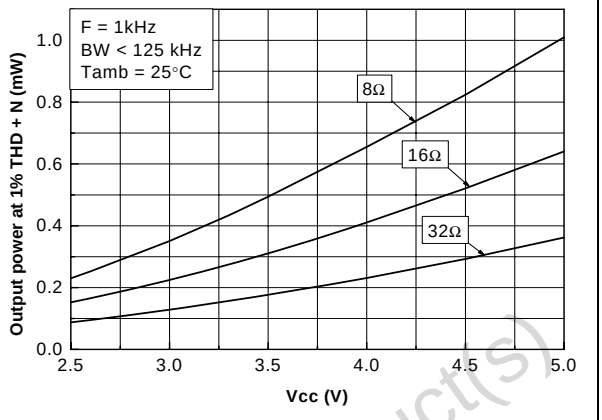


Figure 28. Output power vs. supply voltage

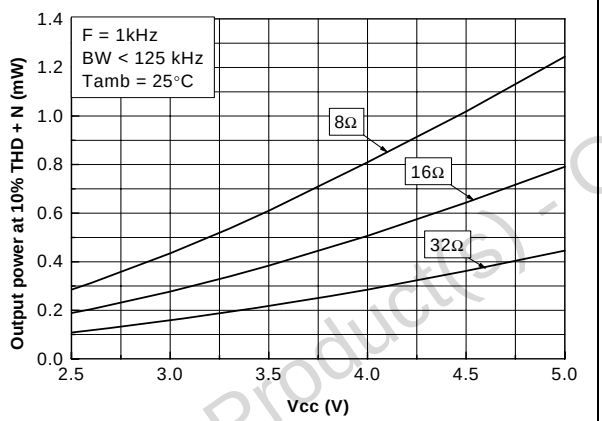


Figure 29. Output power vs. load resistance

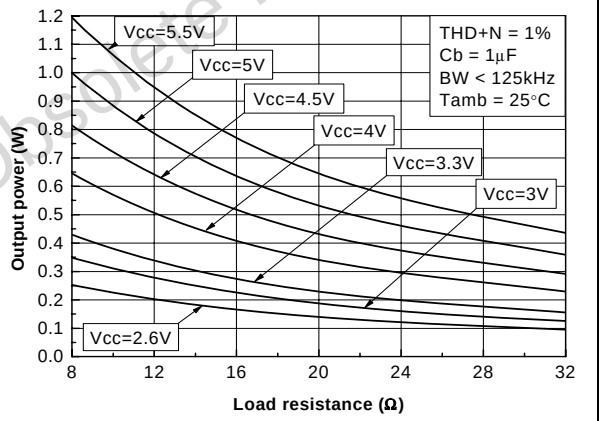


Figure 30. Current consumption vs. supply voltage

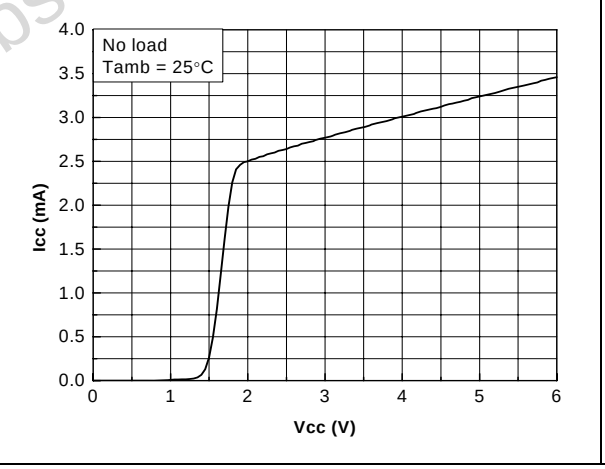


Figure 31. Standby current vs. supply voltage

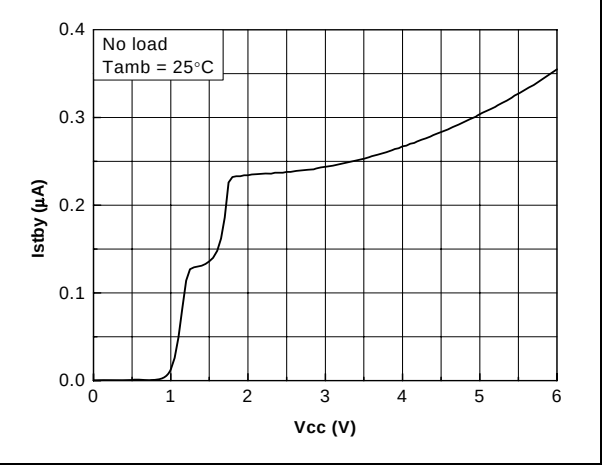


Figure 32. Standby voltage vs. supply current

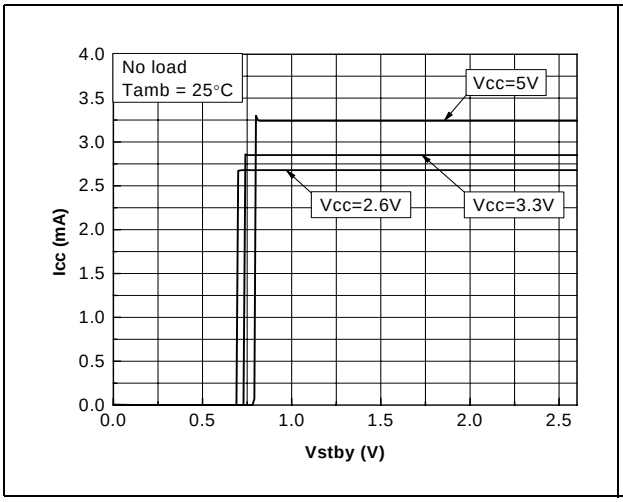


Figure 33. Frequency response

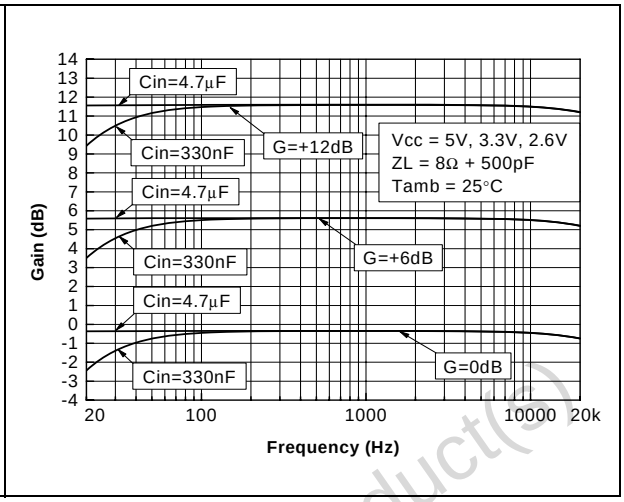


Figure 34. Frequency response

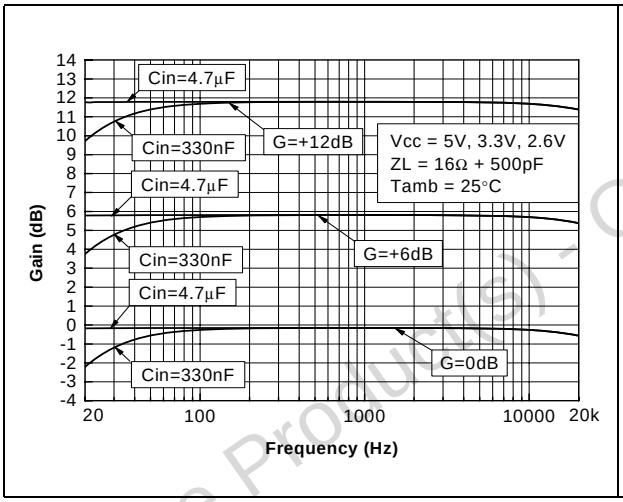


Figure 35. Power dissipation vs. output power

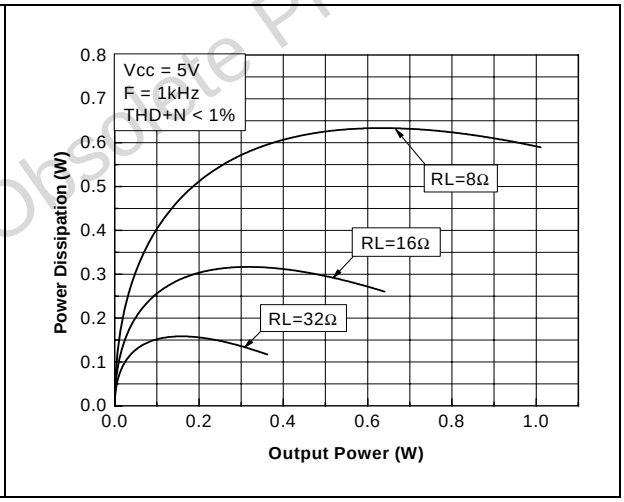


Figure 36. Power dissipation vs. output power

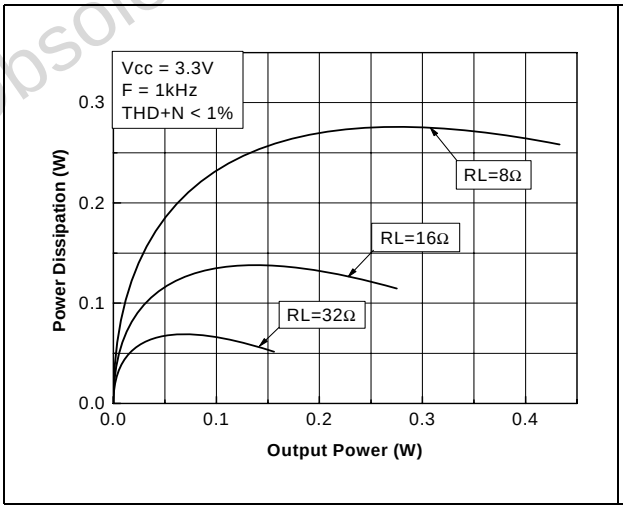


Figure 37. Power dissipation vs. output power

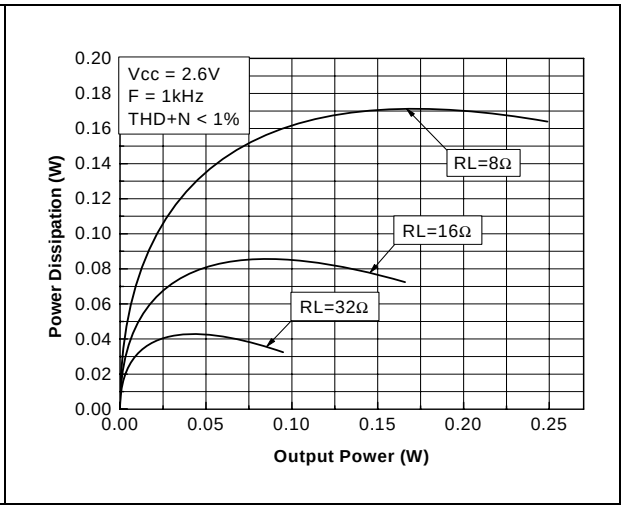
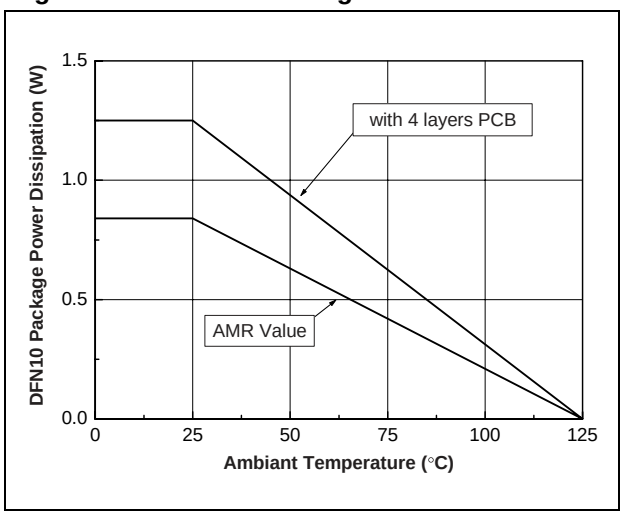


Figure 38. Power derating curves



4 Application information

4.1 Differential configuration principle

The TS4974 is a monolithic full-differential input/ output power amplifier with a digital volume control. It has an internal gain range of -33 dB up to +12 dB, by steps of 3dB (see *Section 4.9: Volume setting on page 20*), which offers better performance in terms of noise immunity and PSRR.

The advantages of a full-differential amplifier are:

- Very high PSRR (power supply rejection ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers.
- Easier interfacing with differential output audio DAC.

In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. But, to reach maximum performance in all tolerance situations, it is better to keep this option.

4.2 Low frequency response

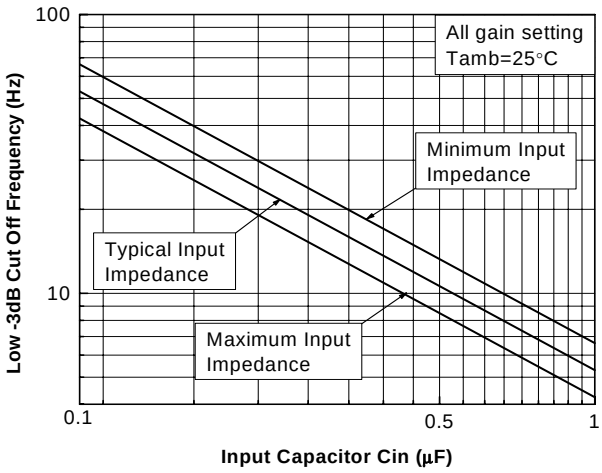
The input coupling capacitors block the DC part of the input signal at the amplifier inputs. Input capacitors C_{in} and input impedance Z_{in} forms a first-order, high pass filter with -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad \text{(Hz)}$$

Note: Differential input impedance of 60 kΩ is a typical value, and there is tolerance around this value.

From *Figure 39* you can easily establish the C_{in} value required for a cut-off frequency of -3 dB.

Figure 39. -3dB lower cut-off frequency vs. input capacitance



4.3 Power dissipation and efficiency

Assumptions:

- Load voltage and current are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{CC})

The output voltage is:

$$V_{out} = V_{peak} \sin\omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{V_{peak}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

Equation 1

$$I_{CC\ AVG} = 2\frac{V_{peak}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

$P_{supply} = V_{CC}\ I_{CC\ AVG}$ (W)

Therefore, the **power dissipated by each amplifier** is:

$P_{diss} = P_{supply} - P_{out}$ (W)

Equation 2

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{out}} = 0$$

and its value is:

Equation 3

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L} (W)$$

Note: This maximum value is only dependent on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

Equation 4

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{peak}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so:

$$\eta = \frac{\pi}{4} = 78.5\%$$

The maximum die temperature allowable for the TS4974 is 125°C. However, in case of overheating, a thermal shutdown set to 150° C, puts the TS4974 in standby until the temperature of the die is reduced by about 5° C.

To calculate the maximum ambient temperature T_{amb} allowable, you need to know:

- Power supply voltage value, V_{CC}
- Load resistor value, R_L
- The package type, R_{THJA}

Example: V_{CC}=5 V, R_L=8 Ω, R_{THJA}flip-chip=80° C/W (125 mm^2 copper heatsink).

Using the power dissipation formula given above in *Equation 3* this gives a result of:

$P_{dissmax}$ = 633mW

T_{amb} is calculated as follows:

Equation 5

$$T_{amb} = 125° C - R_{TJHA} \times P_{dissmax}$$

Therefore, the maximum allowable value for T_{amb} is:

T_{amb} = 125-80x0.633 = 74.3°C

4.4 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4974. A power supply bypass capacitor C_S and a bias voltage bypass capacitor C_b.

C_S has particular influence on the THD+N in the high frequency region (above 7 kHz) and an indirect influence on power supply disturbances. With a value for C_S of 1 µF, you can expect similar THD+N performance to that shown in the datasheet.

In the high frequency region, if C_S is lower than 1 µF, it increases the THD+N, and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is higher than 1 µF, the disturbances on the power supply rail are more filtered.

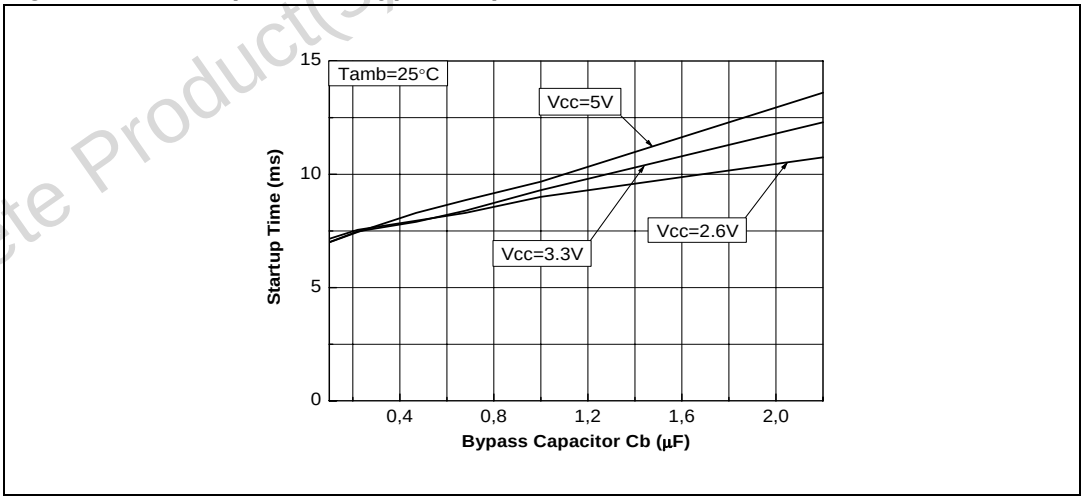
C_b has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

4.5 Wake-up time (t_{WU})

When the standby is released to put the device ON, the bypass capacitor C_b is not charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called the wake-up time or t_{WU} and is specified in the tables in *Section 3: Electrical characteristics on page 5*, with C_b=1 µF. During the wake-up phase, the TS4974 gain is close to zero. After the wake-up time, the gain is released and set to its nominal value.

If C_b has a value other than 1 µF, refer to *Figure 40* to establish the wake-up time.

Figure 40. Startup time vs. bypass capacitor



4.6 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode, the Bypass pin and Vin+, Vin- pins are short-circuited to ground by internal switches. This allows a quick discharge of C_b and C_{in} capacitors.

4.7 Pop performance

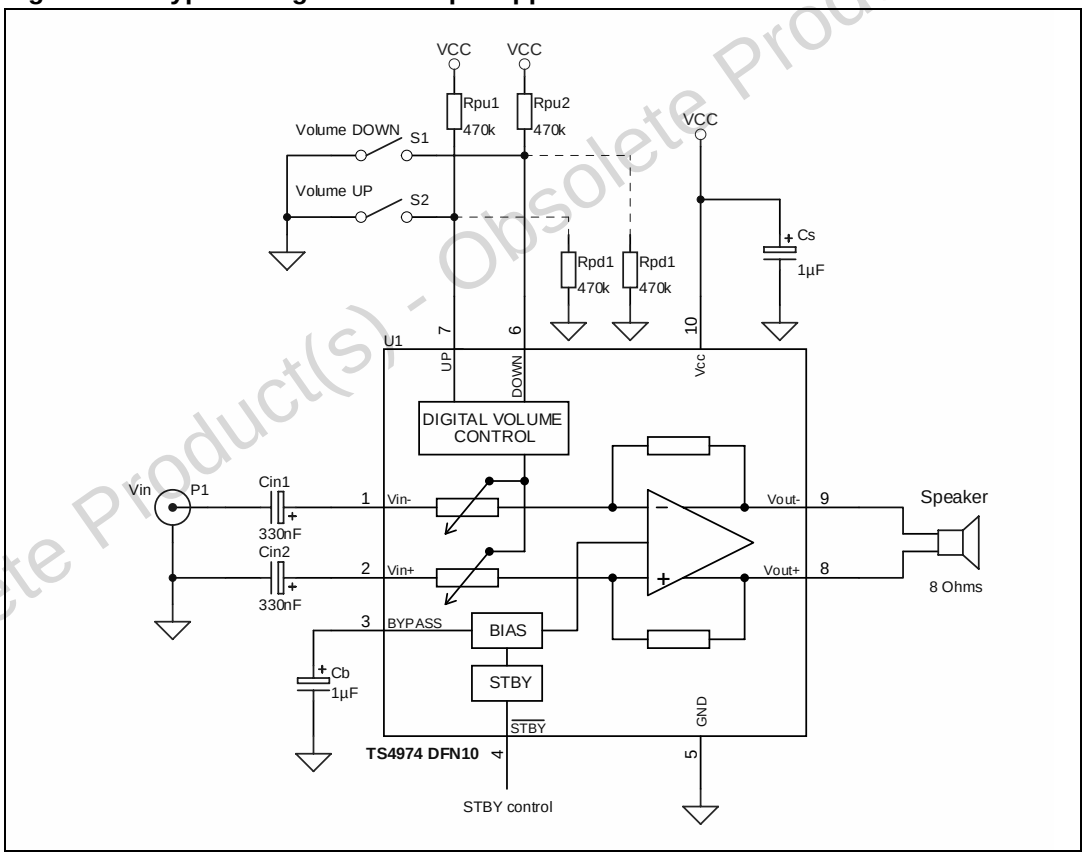
Due to its fully differential structure, the pop performance of the TS4974 is close to perfect. However, due to mismatching between internal resistors R_{in}, R_{feed}, and external input capacitors C_{in}, some noise might remain at startup. To eliminate the effect of mismatched components, the TS4974 includes pop reduction circuitry. With this circuitry, the TS4974 is close to zero pop for all possible common applications.

In addition, when the TS4974 is in standby mode, due to the high impedance output stage in this configuration, no pop is heard.

4.8 Single-ended input configuration

It is possible to use the TS4974 in a single-ended input configuration. The schematic in *Figure 41* shows an example of this configuration.

Figure 41. Typical single-ended input application



4.9 Volume setting

The TS4974 features a digital volume control with an internal gain range of -33 dB up to +12 dB, by steps of 3 dB. When the device is powered up from V_{CC} (and not from the standby pin), an initial gain of -12dB is internally fixed. When standby mode is activated, the gain value is memorized and held until standby is released.

The volume is controlled by means of two pins, UP/DVC and DOWN/DVC. When the V_{IL} voltage is applied, it activates the increase or decrease in gain. When one of the input pins is grounded, volume changing is activated. When both volume UP and DOWN functions are activated at the same time, there is no effect on the volume.

The UP/DVC and DOWN/DVC inputs need to be pulled-up or pulled-down, so a pair of external pull-up or pull-down resistors are required. When pull-up resistors are used, it is dependent on the application which values of resistors you should choose in the range from 10kΩ to 1MΩ The current flowing through the switch S1 or S2 during volume changing is adjusted by the value of the pull-up resistors.

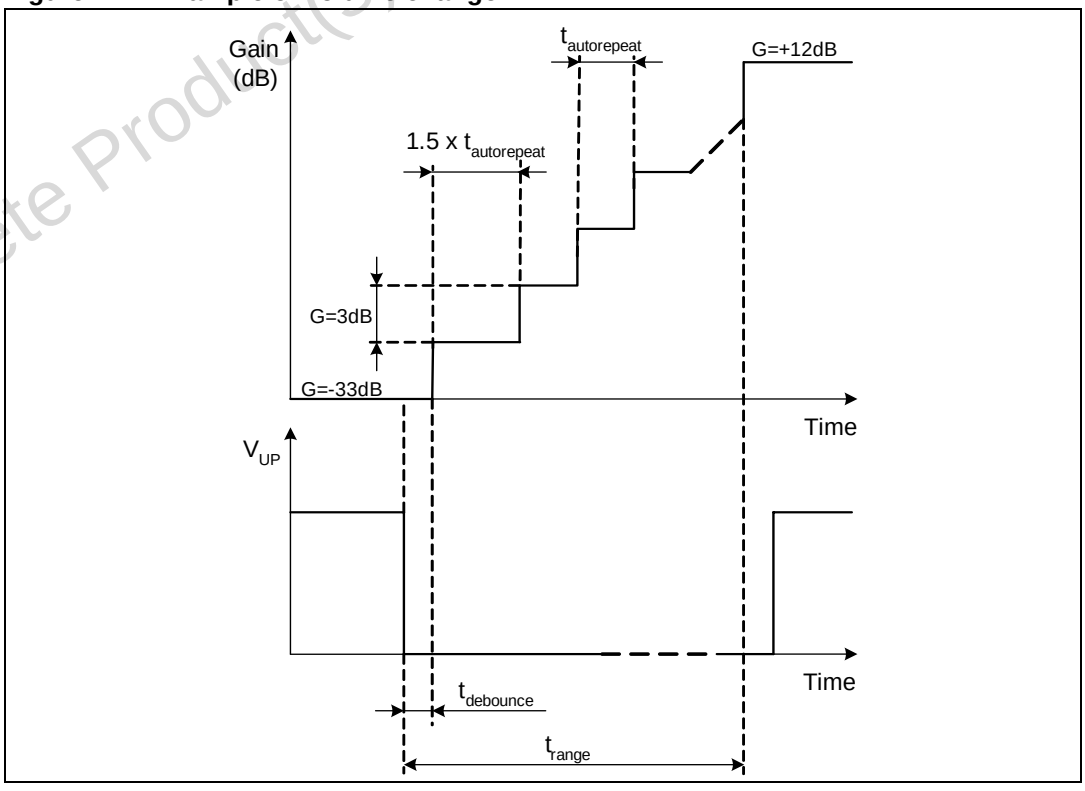
When pull-down resistors are used, the values are chosen in the range from at least 430kΩ to 1MΩ (a value 470kΩ is recommended). Typically, in this case a 10µA current flows through the switch S1 or S2 during volume changing.

Table 2 on page 3 indicates the values of the $V_{U/D}$ voltages required to activate an increase or decrease in volume. The volume can also be controlled by a microcontroller. In this case, transistors can be used as switches for grounding the UP/DVC and DOWN/DVC pins.

The TS4974 integrates a debouncing system which does not take into account UP or DOWN pulses that are shorter than the $t_{debounce}$ time. In addition, an autorepeat function is implemented. When a continuous voltage is applied to the UP or DOWN pin, the gain is continuously increased or decreased after a certain time called $t_{autorepeat}$. The first period of each autorepeat sequence is longer ($t_{autorepeat}$ x 1.5) to avoid any parasitic activation. In this mode, the time t_{range} is necessary to cover the whole gain range of the device.

Figure 42 explains the meaning of the debounce, autorepeat and range times (respectively $t_{debounce}$, $t_{autorepeat}$ and t_{range}). It shows how the volume increases over the whole volume range from the minimum gain -33 dB to the maximum gain +12 dB by 3 dB steps.

Figure 42. Example of volume change



4.10 Notes on PSRR measurement

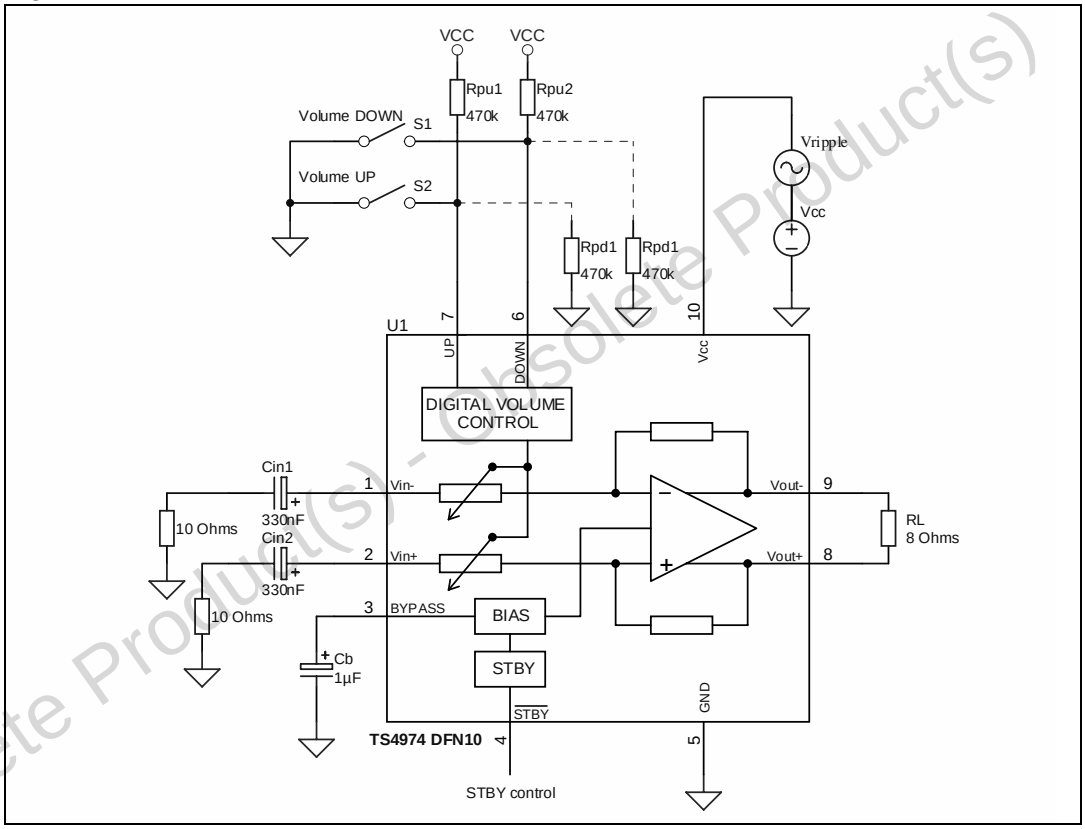
What is the PSRR?

The PSRR is the power supply rejection ratio. The PSRR of a device is the ratio between a power supply disturbance and the result on the output. In other words, the PSRR is the ability of a device to minimize the impact of power supply disturbance to the output.

How is the PSRR measured?

The PSRR is measured as shown in *Figure 43*.

Figure 43. PSRR measurement



Principles of operation

- The DC voltage supply (V_{CC}) is fixed
- The AC sinusoidal ripple voltage (V_{ripple}) is fixed
- No bypasss capacitor Cs is used

The PSRR value for each frequency is calculated as:

$$PSRR = 20 \times Log\left[\frac{RMS_{(Output)}}{RMS_{(Vripple)}}\right](dB)$$

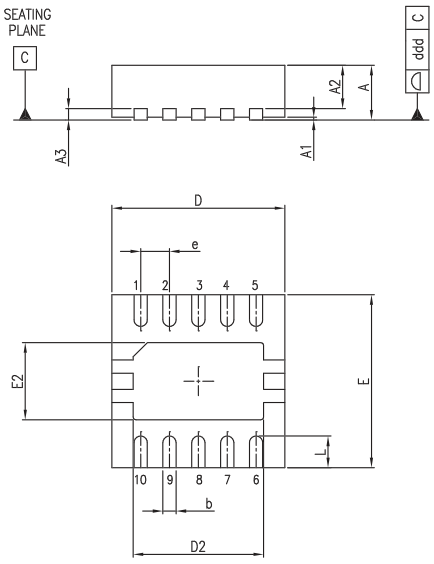
RMS is an rms selective measurement.

5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Table 8. DFN10 3x3 exposed pad package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			25.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.21	2.26	2.31	87.0	89.0	91.0
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.3	0.4	0.5	11.8	15.7	19.7



6 Ordering information

Table 9. Order codes

Part number	Temperature range	Package	Packing	Marking
TS4974IQT	-40° C to +85° C	DFN10	Tape & reel	A74

7 Revision history

Date	Revision	Changes
1-Nov-2005	1	Mechanical data updated for DFN10 package.
1-Oct-2006	2	Preliminary data.
25-Oct-2006	3	Final datasheet.
10-May-2007	4	Updated *Figure 1*, *Figure 41*, and *Figure 43*. Added *Table 3*. Modified *Section 4.9 on page 20* to add information on pull-up and pull-down resistors.

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