PL485-EK User Guide

Introduction

PL485-EK is an evaluation kit for the PL485. PL485 is a programmable System On Chip (SOC) for narrow-band Power Line Communication (PLC) from Microchip Technology Inc, able to run any PLC protocol in the frequency band below 500 kHz. Depending on the running firmware, PL485 is able to support applications not only for basic connectivity (point to point or point to multi-point connectivity) but also for complex mesh network topologies.

The PL485-EK board has been conceived to communicate in the CENELEC B-Band (95 kHz to 125 kHz) and complies with the CENELEC EN 50065 standard. It is designed to be directly connected to low voltage DC power rails and optionally to AC mains by means of an external coupler accessory. Please refer to PLC-AC-Coupler User Guide for more information about the AC coupler accessory.

Contents

- Welcome letter
- Board:
  - One PL485-EK board
- Cable:
  - One Micro A/B-type USB cable

Kit contents are protected with anti-static foam. The PL485-EK board is shipped in an anti-static shielding bag.

WARNING The board must not be subject to high electrostatic discharges. It is recommended to use a grounding strap or similar ESD protective device when handling the board in hostile ESD environments. Avoid touching the component pins or any other metallic element on the board.

Features

- PL485-EK board includes a PL485 system on chip, able to run any PLC protocol in the <500 kHz band.
- PL485-EK board implements a coupling circuit optimized for the band 95kHz to 125 kHz, compliant with CENELEC standard EN50065.
- SWD/JTAG interface for MCU debugging and programming purposes. PL485-EK board includes as well a USB Embedded Debugger (EDBG) for on-board debugging.
- USB 2.0 full-speed interface
- mikroBUS™ socket connector to interface with other circuits and add-on boards.
- Xplained PRO header connector (master) to interface with other circuits and add-on boards.
- RESET push button, ERASE jumper.
- Voltage monitor circuit on the 5V rail, or alternatively on the 3.3V rail with minor modifications.
- PL485-EK board can be powered from the following sources:
  - Micro-B USB connector (J5)
  - Micro-B USB connector (J12)

– Xplained PRO PWR connector (J7)
– DC Jack connector (J3) or 2 position terminal block (J2)

Figure 1. PL485-EK Board top view

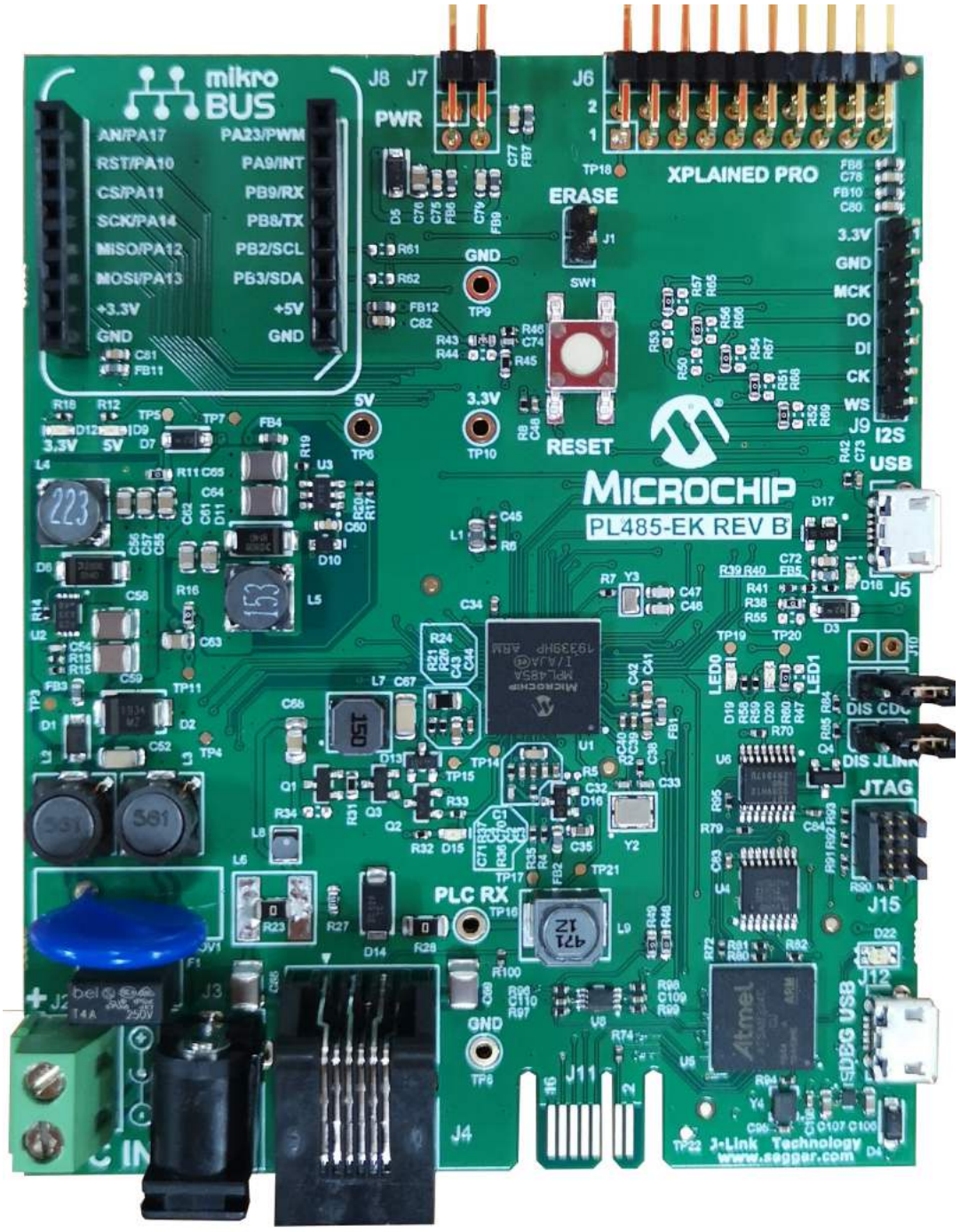


Table of Contents

1. Evaluation Kit Specifications

1.1 Safety Recommendations

This evaluation board is intended for engineering, development, demonstration or evaluation purposes only. It is not a finished product, unless otherwise noted on the board/kit, so it is intended for indoor use only.

⚠ CAUTION The PL485-EK board is not electrically isolated from the power supply inputs. Please handle the PL485-EK board with care to avoid risk of electrical shock, which may arise in case of earth faults or accidental contact with high voltage on the power rail.

Operating temperature range is 0ºC to +70ºC, limited by the rubber pads and the reset switch. The rest of the components can work properly from 0 to 85ºC. Operation for extended periods of time over the minimum and maximum values may cause permanent damage to the board.

Important: Microchip does not assume any responsibility for the consequences arising from an improper use of the PL485-EK board.

1.2 Electrical Characteristics

This section contains information about PL485-EK power supply requirements and consumption. It is assumed that the board is powered from the DC Jack connector. For more details about the power supply system, please check section 3.3.5 Power Supply System.

Table 1-1. DC Power Supply Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit
DC Mains Voltage Range	DC Jack Connector, J8	6	-	48	V_{DC}

Table 1-2. Power Consumption

Parameter	Condition	Typ.	Unit
RX Power Consumption	Measured at R16, 3.3V DC/DC output	245(1)	mW
TX Power Consumption	FW: G3 CEN-B PHY test Console Application Measured at R16, 3.3V DC/DC output	345(1)	

Note:

1. These measurements were taken running PHY TX Test Console project included in the kit with a default configuration in TX mode and RX mode. The power consumption is measured at the output of the 3.3V DC/DC converter.

2. Getting Started

2.1 Running the Demo Application

The board has to be powered by means of the included USB cable or from an external DC Power Supply ranging from 6V to 48V. When the board is powered, the LEDs D9 (3V3) and D12 (5V) turn on. Connect a suitable cable to one of the connectors J2 or J3 and plug it to a DC voltage grid to communicate.

Once the board is supplied, the PL485-EK board runs the pre-programmed application *PLC & Go* for CENELEC B-Band, a chat application between two or more end points using Microchip PLC modem boards. Any end point can transmit a message, which is received by the other end points in the network. LED0 (D19, green) blinks to indicate that the application is running. LED1 (D20, red) flashes when a PLC message is received and LED D15 (yellow) flashes at each transmission.

2.2 Code and Technical Support

Firmware developers can not only run the given example code, but also implement their own applications based on the provided firmware stacks.

Please note that the latest software code, documentation and support materials are available on www.microchip.com. Follow instructions described in the welcome letter for more information.

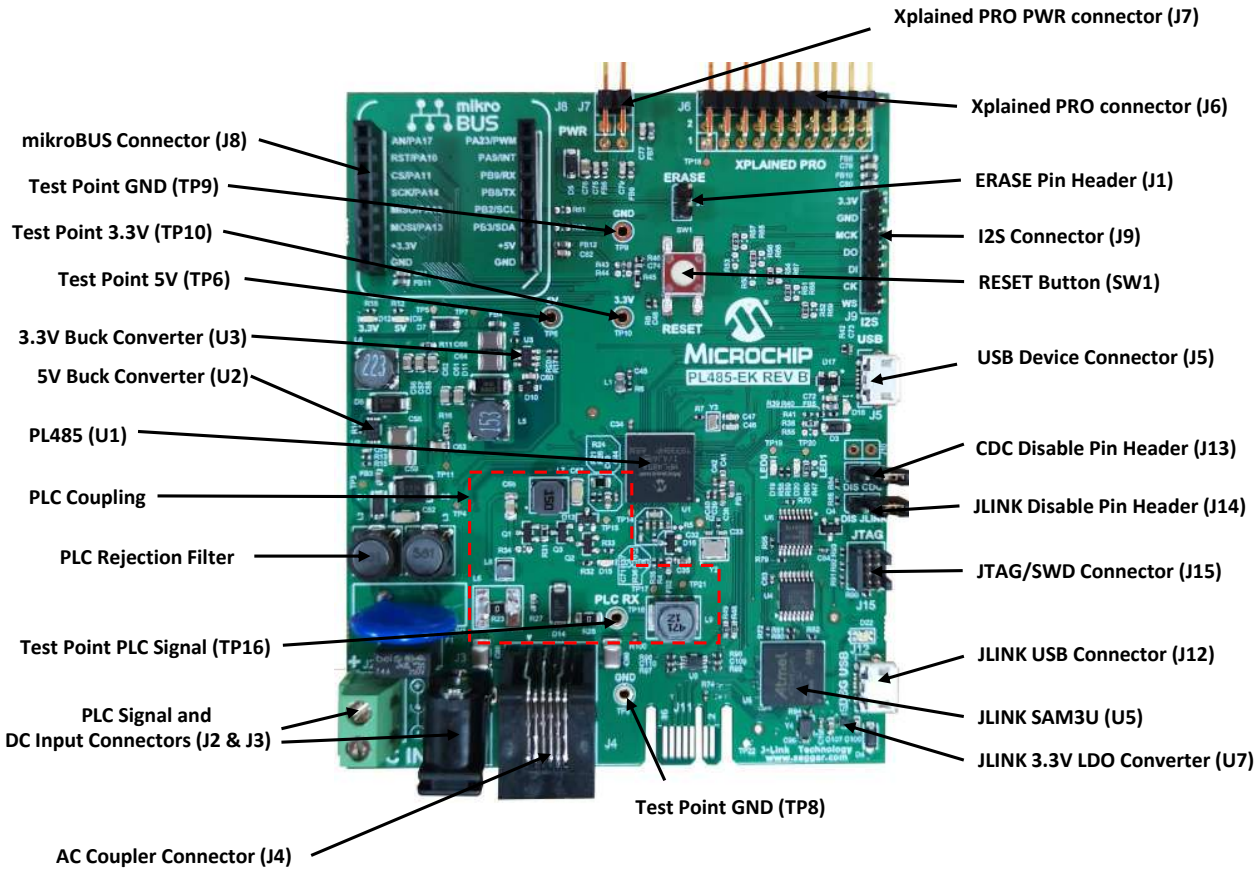
For any technical support requests, please visit http://support.microchip.com.

3. PL485-EK Board

3.1 Overview

This section summarizes the PL485-EK board design. It introduces system-level concepts, such as power supply, MCU, PLC coupling, peripherals and board interfaces.

Figure 3-1. PL485-EK Board Description



3.2 Features List

The PL485-EK board includes the following features:

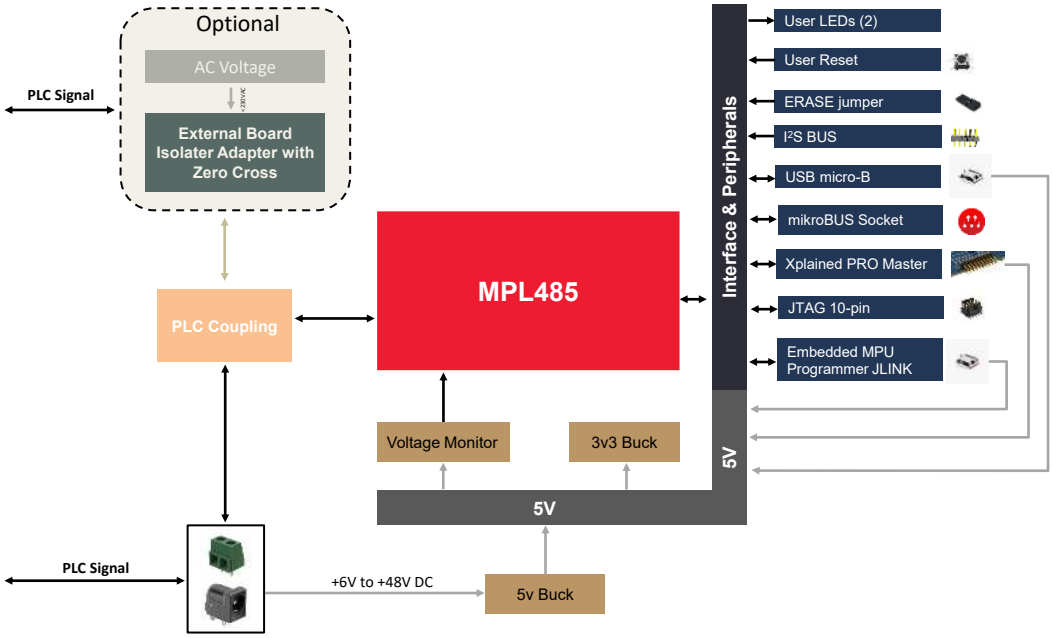
- PL485 SOC:
  - MCU Core:
    - ARM Cortex-M4 running at up to 100 MHz
    - Memory Protection Unit (MPU)
    - DSP instruction set
    - Floating-Point Unit (FPU)
    - Thumb®-2 instruction set
    - Instruction and Data Cache Controller with 2 Kbytes cache memory
  - Memories:
    - Up to 512 Kbytes of embedded Flash
    - Up to 176 Kbytes of embedded SRAM

    - Up to 8 Kbytes of ROM with embedded bootloader, single-cycle access at full speed
  - Multi-protocol PLC modem:
    - Protocols:
      - G3-PLC
      - PRIME 1.3 and PRIME 1.4
    - Zero-Cross Detection
    - Embedded PLC Analog Front End (AFE)
    - Low-power consumption in transmission and reception
- PLC Coupling designed to communicate in CENELEC B-Band (95 kHz to 125 kHz)
- A 3.3V buck converter for the digital circuitry and a 5V Buck converter for supplying 5V for mikro BUS and Xplained PRO connector
- Peripherals:
  - Supply monitor
  - User LEDs
  - Reset button
  - Chip Erase jumper
  - Disable JLINK jumper
  - Disable CDC jumper
- Interfaces:
  - USB Device
  - mikroBUS Socket Connector
  - SWD/JTAG Debugging Port
  - JLINK USB Embedded MPU Programmer
  - Xplained PRO Master
  - I2S Connector

3.2.1 PL485-EK Block Diagram

The following figure shows the block diagram of the PL485-EK board.

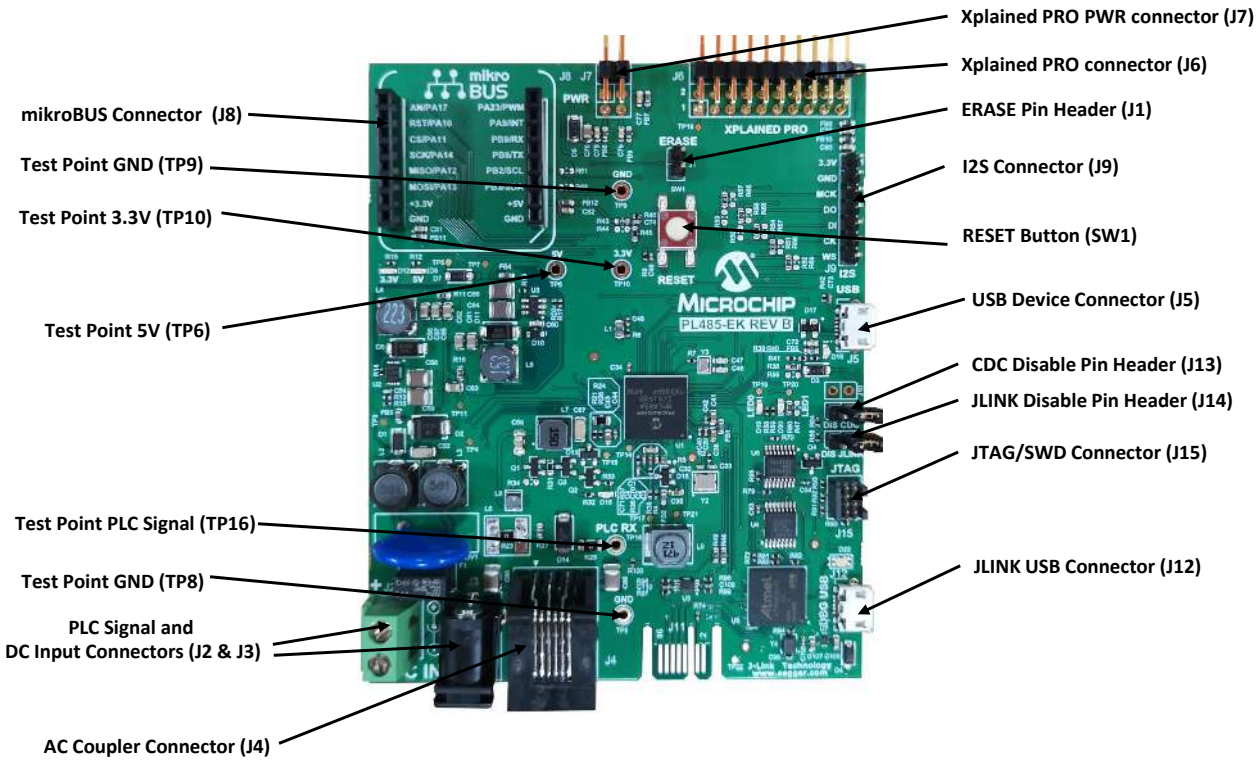
Figure 3-2. PL485-EK Block Diagram



3.2.2 Interface Connection

The following figure shows an overview of the connectors, jumpers and button of the PL485-EK board.

Figure 3-3. PL485-EK Connectors, Button and Jumpers Overview



3.2.2.1 Connectors

The PL485-EK board includes the following connectors:

1. PLC Connector and DC Input, J2 (same than J3).

Table 3-1. PLC Connector and DC Input, J2 (same than J3)

Pin	Signal Name	Description
1	+	Positive Voltage / PLC+ Signal
2	-	Negative Voltage / PLC- Signal

2. PLC Connector and DC Input, J3 (same than J2).

Table 3-2. PLC Connector and DC Input, J3 (same than J2)

Pin	Signal Name	Description
1	+	Positive Voltage / PLC+ Signal
2	-	Negative Voltage / PLC- Signal

3. PLC AC Coupler Connector, J4.

Table 3-3. PLC AC Coupler Connector, J4

Pin	Signal Name	Description
1	N.C.	Not Connected
2	PL+	PLC + Signal

.....continued		
Pin	**Signal Name**	**Description**
3	PL-	PLC - Signal
4	GND	Ground
5	PL VZC	Zero Cross Signal
6	N.C.	Not Connected

4. USB Device Connector, J5.

Table 3-4. USB Device Connector, J5

Pin	Signal Name	Description
1	VUSB	5V power
2	D-	Data Minus
3	D+	Data Plus
4	ID	On the Go Identification
5	GND	Ground

5. Xplained Pro Standard Extension Header, J6

Table 3-5. Xplained Pro Standard Extension Header, J6

Pin	Signal Name	Mnemonic	Description
1	TP18	ID	Not connected. Pin to communicate with the ID chip on an extension board
2	GND	GND	Ground
3	PA18	ADC(+)	Analog to digital converter; alternatively, a pin for the positive terminal of a differential ADC
4	PA19	ADC(-)	Analog to digital converter; alternatively, a pin for the negative terminal of a differential ADC
5	PB10	GPIO1	General purpose I/O
6	PB11	GPIO2	General purpose I/O
7	PA0	PWM(+)	Pulse width Modulation; alternatively, a pin for the positive part of a differential PWM
8	PA1	PWM(-)	Pulse width Modulation; alternatively, a pin for the negative part of a differential PWM
9	PA2	IRQ/GPIO	Interrupt request pin and/or general purpose I/O pin
10	PB14	GPIO	General purpose I/O
11	PA3	SDA	Data line for I^2C interface
12	PA4	SCL	Clock line for I^2C interface
13	PB1	UART_RX	Receiver pin of target device UART
14	PB0	UART_TX	Transmitter pin of target device UART
15	PA16	SPI_SS_A	Slave select for SPI
16	PA6	SPI_MOSI	Master out slave in line of serial peripheral interface

.....continued

Pin	Signal Name	Mnemonic	Description
17	PA5	SPI_MISO	Master in slave out line of serial peripheral interface
18	PA15	SPI_SCK	Clock for serial peripheral interface
19	GND	GND	Ground
20	3V3	VCC	Power pin for extension board

6. Xplained Pro Power Header, J7.

Table 3-6. Xplained Pro Power Header, J7

Pin	Signal Name	Mnemonic	Description
1	GND	GND	Ground
2	5V_XPLAIN	VEXT_P5V0	External 5V input
3	3V3	Target VTG	Regulated 3.3V (output)
4	5V	VCC_P5V0	Unregulated 5V (output)

7. mikroBUS Socket Connector, J8.

Table 3-7. mikroBUS Socket Connector, J8

Pin	Signal Name	Mnemonic	Description
1	PA17	AN	Analog
2	PA10	RST	Reset
3	PA11	CS	SPI Chip Select
4	PA14	SCK	SPI Clock
5	PA12	MISO	SPI Master Input Slave Output
6	PA13	MOSI	SPI Master Output Slave Input
7	3.3V	+3.3V	Regulated 3.3V (output)
8	GND	GND	Ground
9	GND	GND	Ground
10	5V	+5V	Unregulated 5V (output)
11	PB3	SDA	I^2C Data
12	PB2	SCL	I^2C Clock
13	PB8	TX	UART Transmit
14	PB9	RX	UART Receive
15	PA9	INT	Hardware Interrupt
16	PA23	PWM	Pulse-width Modulation

8. Inter-IC Sound (I^2S), J9.

Table 3-8. Inter-IC Sound (I^2S), J9

Pin	Signal Name	Mnemonic	Description
1	3.3V	3.3V	VCC - 3.3V power

.....continued			
Pin	**Signal Name**	**Mnemonic**	**Description**
2	GND	GND	Ground
3	PA4	MCK	Master Clock (Output)
4	PA3	DO	Serial Data Output
5	PA2	DI	Serial Data Input
6	PA0	CK	Serial Clock (Input/Output)
7	PA1	WS	I^2S Word Select (Input/Output)

9. USB Debug Connector (DBG USB), J12.

Table 3-9. USB Debug Connector (DBG USB), J12

Pin	Signal Name	Description
1	VUSB	5V power
2	D-	Data Minus
3	D+	Data Plus
4	ID	On the Go Identification
5	GND	Ground

10. JTAG/SWD 10-pin connector for PL485, J15.

Table 3-10. JTAG/SWD 10-pin connector for PL485, J15

Pin	Mnemonic	Description
1	VCC	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from V_{CC} of the target board and must not have a series resistor.
2	TMS/SWDIO	Serial Wire Input Output / Test Mode Select. JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of target CPU.
3	GND	Ground.
4	TCK/SWCLK	Serial Wire Clock / Test Clock. JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of target CPU.
5	GND	Ground.
6	TDO/SWO	Test Data Output. JTAG data output from target CPU. Typically connected to TDO of target CPU.
7	KEY	-
8	TDI/NC	Not Connected / Test Data Input. JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of target CPU.
9	GNDdetect	Ground.
10	nRESET	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET". This signal is an active low signal.

3.2.2.2 Jumper Configurations

The following table describes the functionality of the jumpers.

Table 3-11. Jumper Configuration

Jumper	Label	Default Setting	Function
J1	ERASE	Open	PL485 Flash memory code erase (closed = erase)
J13	DIS CDC	Open	Enable debug UART in JLINK (closed = Disable UART in JLINK (J12 DBG USB))
J14	DIS JLINK	Open	Select between JLINK or JTAG programmer (closed = Disable JLINK enable J15 JTAG programmer)

Note: Pitch jumpers are 2.54 mm (0.1").

3.2.2.3 Test Points

Some test points (probes and pads) have been placed on the PL485-EK board for the verification of the main signals.

Table 3-12. Test Point Probes

Reference	Function
TP6	5V
TP8	GND
TP9	GND
TP10	3V3
TP16	PLC signal

Table 3-13. Test Point Pads

Reference	Function	Reference	Function
TP1	Pin PL NRST	TP13	PL-
TP2	Pin JTAGSEL	TP14	Pin PL TXRX0
TP3	VDC	TP15	Pin PL TXRX1
TP4	GND	TP17	PLC Signal
TP5	5V REG	TP18	Xplained PRO ID
TP7	GND	TP19	Pin PA31, LED0 D19
TP8	GND	TP20	Pin PA19, LED1 D20
TP9	GND	TP21	Pin PL VZC
TP11	3.3V	TP22	3.3V JLINK
TP12	PL+	-	-

3.3 Hardware Description – System

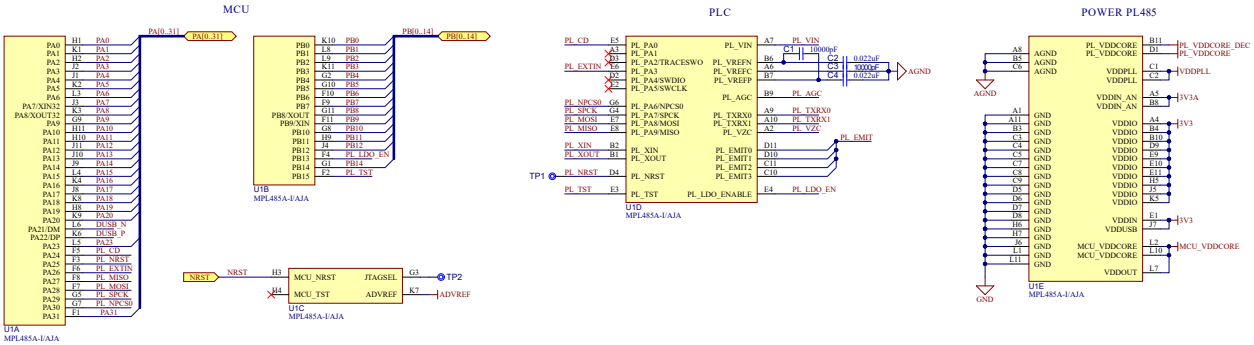
3.3.1 PL485

The PL485-EK board is equipped with a PL485 device in 121-Ball TFBGA (10x10, 0.8 mm ball pitch).

The PL485 embeds a PL360, a multi-protocol modem for Power Line Communication, and it also embeds a SAMG55, a Cortex-M4 CPU with an FPU (floating point unit). This flexible architecture allows implementation of standard and customized PLC solutions.

Figure 3-4 shows the different components of PL485 Schematic.

Figure 3-4. PL485



The following figure shows the recommended connection in the PCB between balls of the PL485 to connect SAMG55 and PL360 internal blocks and the functionalities of GPIO connections.

Figure 3-5. PL485: SAMG55-PL360 Ball Connections at PCB Level

PL485 Ballout	PL360 Signal		SAMG55 Signal	PL485 Ballout
D4	PL_NRST	↔	PA25	F3
E3	PL_TST	↔	PB15	F2
E4	PL_LDO_ENABLE	↔	PB13	F4
E5	PL_PA0	↔	PA24	F5
E6	PL_PA3	↔	PA26	F6
E7	PL_PA8/MOSI	↔	PA28	F7
E8	PL_PA9/MISO	↔	PA27	F8
G4	PL_PA7/SPCK	↔	PA29	G5
G6	PL_PA6/NPCS0	↔	PA30	G7

Table 3-14 and Table 3-15 summarize the functionality of each input/output line of the PL485-EK board.

Table 3-14. Pinout of PL485 PortA in PL485-EK Board

I/O LINE	Function	I/O LINE	Function
PA0/I2SCK0/TIOA0	I2SCK0 / PWM+ (XPLAIN)	PA16/NPCS02	SPI2_NCPS0 (XPLAIN)
PA1/I2SWS0/TIOB0	I2SWS0 / PWM- (XPLAIN)	PA17/AD0	AD0 (mikroBUS)
PA2/I2SDI0/WKUP	I2SDI0 / IRQ (XPLAIN)	PA18/AD1	AD1 (XPLAIN)
PA3/I2SDO0/TWD	I2SDO0 / I2C_SDA (XPLAIN)	PA19/AD2	UserLed1 / AD2 (XPLAIN)
PA4/I2SMCK0/TWCK3	I2SMCK0 / I2C_SCL (XPLAIN)	PA20/AD3	AD3 (Voltage Monitor)
PA5/MISO2	SPI2_MISO (XPLAIN)	PA21/DM	DUSB_N (USB Device Diff Negative)

.....continued

I/O LINE	Function	I/O LINE	Function
PA6/MOSI2	SPI2_MOSI (XPLAIN)	PA22/DP	DUSB_P (USB Device Diff Positive)
PA7/XIN32	XIN32	PA23/TIOA1	PWM (mikroBUS)
PA8/XOUT32	XOUT32	PA24	PL_CD
PA9/WKUP6	INT (mikroBUS)	PA25	PL_NRST
PA10	RST (mikroBUS)	PA26	PL_EXTIN
PA11/NPCS05	SPI5_NPCS0 (mikroBUS)	PA27/MISO7	PL_MISO
PA12/MISO5	SPI5_MISO (mikroBUS)	PA28/MOSI7	PL_MOSI
PA13/MOSI5	SPI5_MOSI (mikroBUS)	PA29/SPCK7	PL_SPCK
PA14/SPCK5	SPI5_SPCK (mikroBUS)	PA30/NPCS07	PL_NPCS0
PA15/SPCK2	SPI2_SPCK (XPLAIN)	PA31	PA31(UserLed0)

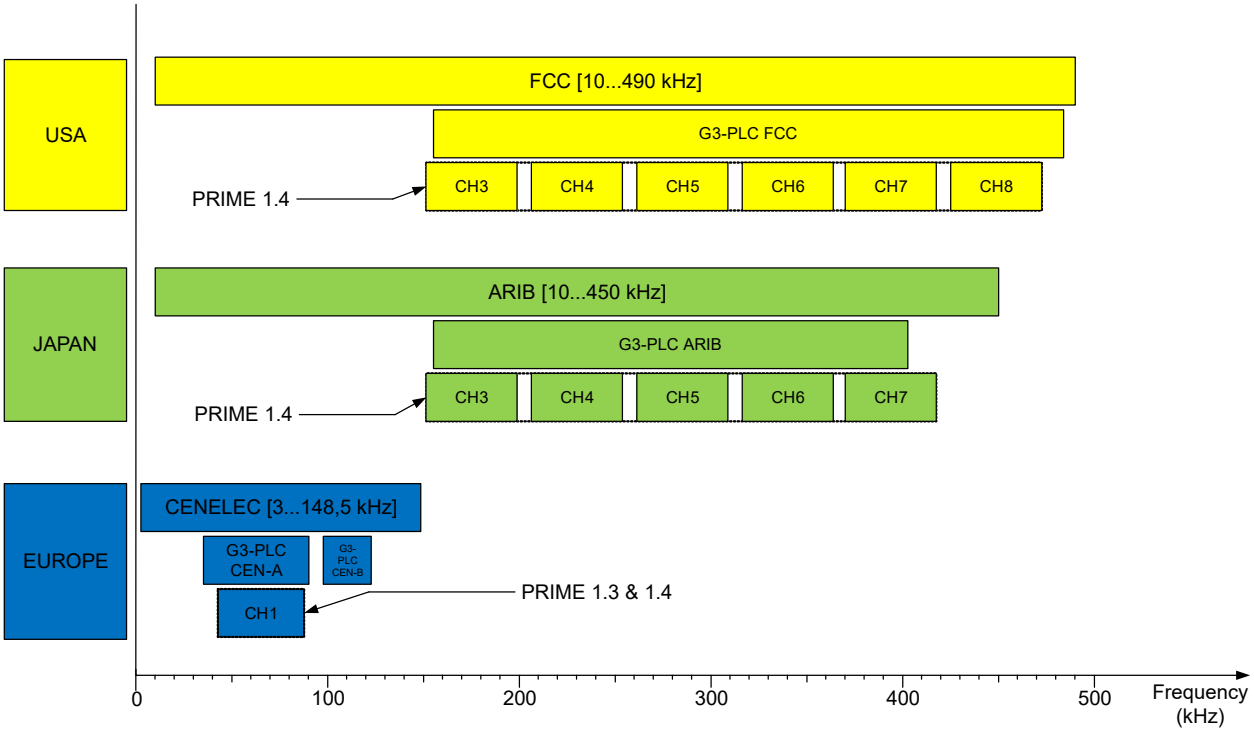
Table 3-15. Pinout of PL485 PortB in PL485-EK Board

I/O LINE	Function	I/O LINE	Function
PB0/TXD6	UART_TX (XPLAIN)	PB8/TXD4/XOUT	UART_TX (mikroBUS)
PB1/RXD6	UART_RX (XPLAIN)	PB9/RXD4/XIN	UART_RX (mikroBUS)
PB2/TWCK1	I2C_SCL (mikroBUS)	PB10/TXD4	DBGU_TX / GPIO1 (XPLAIN)
PB3/TWD1	I2C_SDA (mikroBUS)	PB11/RXD4	DBGU_RX / GPIO2 (XPLAIN)
PB4/TDI	TDI	PB12/ERASE	ERASE
PB5/TDO/TRACESWO	TDO/TRACESWO	PB13	PL_LDO_ENABLE
PB6/TMS/SWDIO	TMS/SDWIO	PB14	GPIO (XPLAIN) / Check VCC
PB7/TCK/SWCLK	TCK/SWCLK	PB15	PL_TST

For a further description of the PL485 device see the corresponding PL485 Datasheet.

The PL485 requires an external circuit to couple the PLC signal to the transmission line. Microchip provides highly efficient and reduced BOM reference designs for the different coupling options, targeting common configurations in all PLC bands (<500 kHz) complying with existing regulations and PLC communication protocols.

Figure 3-6. PLC Bands Supported by PL485



The coupling circuit of the PL485-EK kit is described with more detail in the chapter 3.3.2 PLC Coupling Circuitry Description. For more information about the available coupling circuits for the PL485 and how to use them, please read the application note Using PL485 to implement a fully featured G3-PLC/PRIME modem.

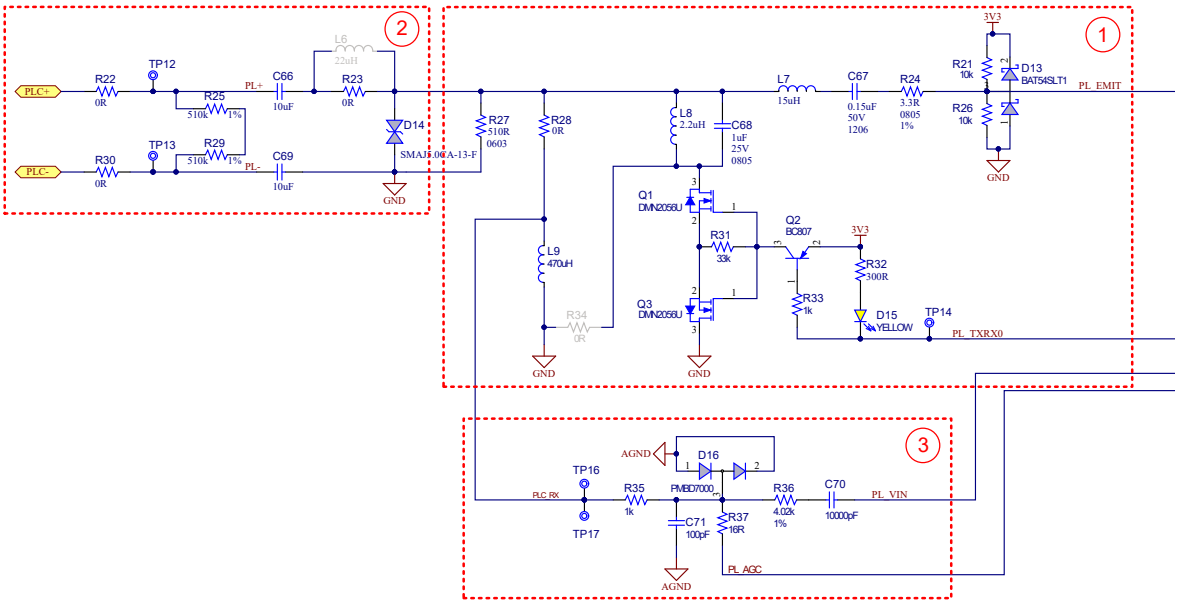
3.3.2 PLC Coupling Circuitry Description

The PL485-EK evaluation board communicates in the band between 95 kHz and 125 kHz (CENELEC B-Band). The PL485-EK board implements a circuit to couple the PLC signal to the transmission line. This design is based on Microchip reference design for a non-isolated coupling in CENELEC-B band without external amplifier, including some modifications to couple the PLC signal to a DC BUS instead to the 220 Vac mains. PL485-EK operates with PL485 internal PLC driver, with no additional external amplification.

The following figure shows the PLC coupling circuit implemented in PL485-EK, which is composed of three sub-circuits:

1. Filtering Stage
2. Coupling Stage
3. Reception Stage

Figure 3-7. PLC Coupling Schematic on the PL485-EK Board



Note: PLC coupling circuitry adds the yellow LED, D15, for visual indication of PLC frames transmission.

The following sections describe the aim of each sub-circuit assembled in the PL485-EK board.

3.3.2.1 PLC Filtering Circuit

The in-band flat response filtering stage reduces spurious emission to the limits set by the corresponding regulation and blocks potential interferences from other transmission channels without distorting the injected signal.

The filtering stage used in PL485-EK, see Figure 3-7, has three aims:

- Band-pass filtering of high frequency components of the square waveform generated by the transmission stage
- Adapt Input/Output impedance for optimal reception/transmission. This is controlled by TXRX0 signal
- A band-pass filtering for received signals

3.3.2.2 PLC Coupling Circuit

The PLC coupling circuit connects the PLC signal directly to DC power rails without requiring any hardware adaptation (or to the mains grid using an AC coupler).

The main purpose of the circuit is to block the voltage of the rail to/from which the signal is injected/received. In PL485-EK, it is carried out by the capacitors, C66 and C69, (see Figure 3-7). Resistors R25 and R29 allow to discharge C66 and C69 capacitors in case of disconnection from DC power rails.

D14 TVS diode protects the coupling circuit from the overvoltage and high transient voltages (surges and spikes) from DC power rails.

⚠ CAUTION PLC coupling components are designed for a maximum voltage of 48 V_{DC}.

Important: In case of using the AC coupler accessory, it is recommended to remove R22 and R30 for better performance. Please refer to PLC-AC-Coupler User Guide for more information about the AC coupler accessory.

3.3.2.3 PLC Reception Circuit

The PLC reception circuit used in PL485-EK, see Figure 3-7, is the reference design for the reception stage and it is composed of:

- Single-pole low pass filter, R35 and C71
- Automatic Gain Control (AGC) circuit, where the resistor R37 is used to attenuate the incoming PLC signal in case its amplitude is high enough to exceed the input dynamic range of the embedded ADC
- A resistor, R36, for impedance matching
- DC decoupling capacitor, C70

3.3.3 Clock Circuitry

Besides the embedded RC oscillators of the PL485, two crystal oscillators are assembled on the PL485-EK board to obtain a more precise and stable system clock reference:

- A 24 MHz clock signal, Y2, generated for the PLC modem (see Figure 3-8). Please refer to the PL360 Datasheet to see the characteristics of this crystal oscillator.
- A low-power 32.768 kHz crystal oscillator, Y3 (see Figure 3-9).

Note: An additional 20 MHz clock crystal, Y1, is not placed. It can be assembled if required by the customer. This crystal oscillator with robust fast start-up can be used instead of the 32.768 kHz crystal oscillator of the SAMG55 (see Figure 3-10).

Figure 3-8. 24 MHz Crystal Oscillator Scheme

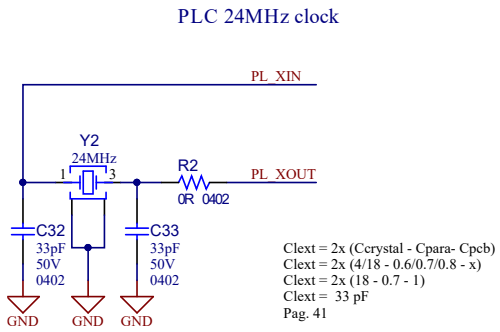


Figure 3-9. 32.768 kHz Crystal Oscillator Scheme

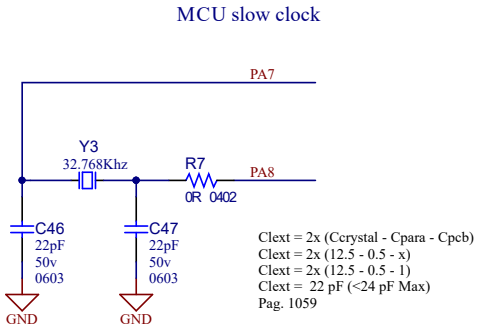
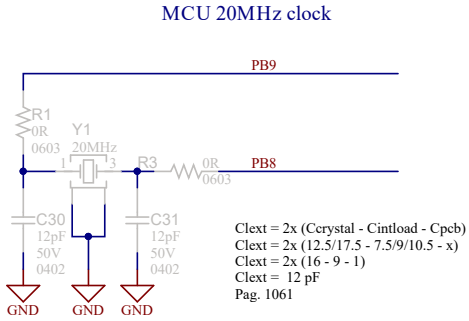


Figure 3-10. 20 MHz Crystal Oscillator Scheme



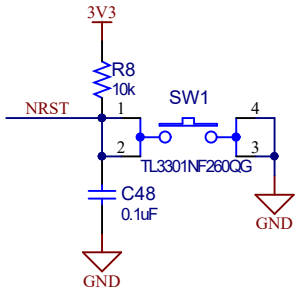
Note: The operating temperature range for crystal oscillators is -40 ºC to +85 ºC. However, please note that crystal oscillators might not cover the previous temperature range with desired performance due to aging.

3.3.4 Reset

The reset sources of the PL485-EK board are:

- Power-on Reset function, embedded in the PL485 device.
- JTAG reset from the in-circuit emulator.
- The RESET push button switch mounted directly on the board. When the RESET button is pressed it will drive the PL485 reset line (NRST) to GND.

Figure 3-11. Reset Button



3.3.5 Power Supply System

The PL485-EK board can be powered from several power sources, as is shown in Table 3-16.

Table 3-16. Power Sources for PL485-EK Board

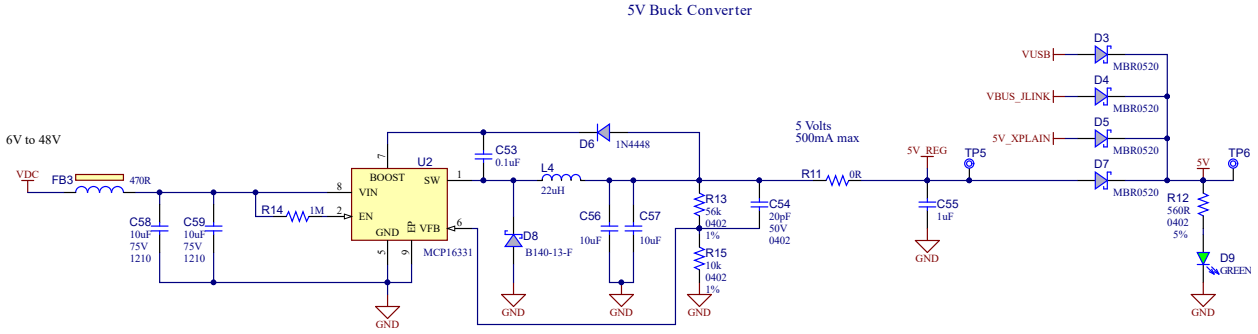
Power Input	Voltage Requirements	Power Requirements	Connector Marking
DC Jack connector (J3)	+6V to +48V (±5%)	3 Watts	DC_IN
DC Input connector (J2)	+6V to +48V (±5%)	3 Watts	DC_IN
USB Micro-B connector (J5)	+5V	According to USB specifications	USB
USB Micro-B connector (J12)	+5V	According to USB specifications	USB
Xplained PRO PWR connector (J7)	+5V	2.5 Watts	PWR

The PL485-EK board has three voltage rails:

- +5V to supply power to the 3.3V buck, Xplained PRO header and mikroBUS connector
- +3.3V buck to supply the PL485 and related peripherals
- +3.3V LDO to supply J-Link

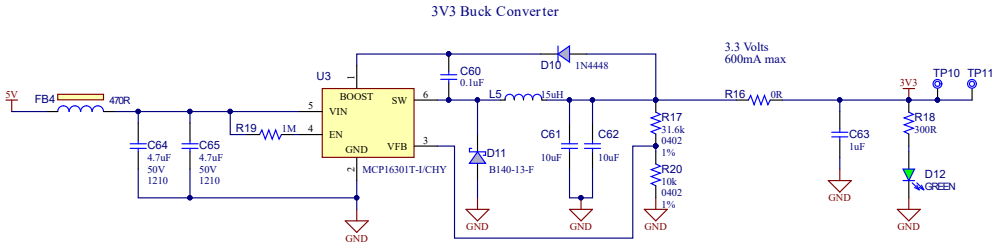
The 5V voltage rail is obtained from the MCP16331 buck converter. For a further description about the buck converter see the MCP16331 High-Voltage Input Buck Converter Evaluation Board User's Guide and MCP16331 Datasheet.

Figure 3-12. 5V Voltage Design



Another buck converter, MC16301, is used to generate a regulated 3.3V voltage rail required by the PL485. For a further description about the buck converter see the MCP16301/MCP16301H Datasheet.

Figure 3-13. 3.3V Buck Converter Design



There is one LED and two test points on each voltage rail to check whether all power supplies are operating properly.

To avoid on board self-generated disturbances within the PLC signal band, both converters are switching at 500 kHz fixed frequency, out of the PLC band (95 to 125 kHz).

Attention: To avoid noise interferences, the switching frequency of the external SMPS must be out of the PLC band and preferably in frequencies above it to avoid harmonics influence. This is essential to obtain a good reception performance.

Please refer to section 3.6 Hardware Description - JLINK Debugger for information about +3.3V LDO to supply J-Link.

3.3.5.1 PLC Rejection Filter

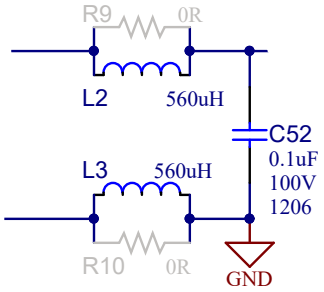
As the PLC coupling circuit is in parallel with the power supply circuit, the input impedance of the final equipment could be affected. If the requirements about total input impedance are not satisfied, an appropriate input filter is needed at the power supply input to increase the input impedance.

Besides the input filter, it is also recommended to add a PLC rejection filter to avoid the absorption of the PLC signals by the power supply circuit. This filter also increases the input impedance, so it helps to achieve the requisites about input impedance.

Notice: The PL485-EK board has PLC coupling and power supply circuits in parallel, so the PLC rejection filter is included. A PLC rejection filter is needed in case of low input impedance after connecting in the same point the PLC Coupling connector J2 and the power source of the board.

The PLC rejection filter of the PL485-EK is composed of two inductors in-series (L = 560 µH) and a capacitor in-parallel (C = 0.1 µF) at the power supply input as shown in the following picture.

Figure 3-14. PLC Rejection Filter Example



To make the filter operational, L2, L3 and C52 must be mounted and R9 and R10 must be unmounted. To disable the filter, R9 and R10 must be mounted and L2, L3 and C52 must be unmounted.

3.4 Hardware Description – MCU Peripherals

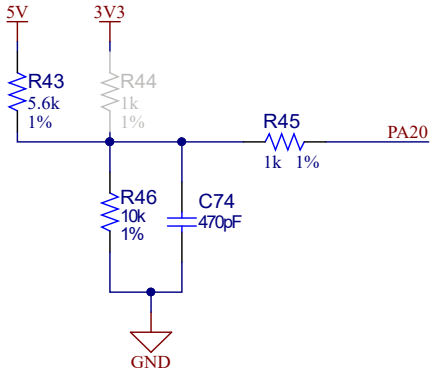
3.4.1 Voltage Monitor

The voltage monitor circuit allows the implementation of multiple functionalities such as:

- Detection of fault conditions
- Detection of Low-Power mode entering conditions
- Detection of wake-up situations

The input pin PA20 of PL485 is used to monitor the 5V voltage rail through external voltage divisors. It can be used to monitor the 3.3V voltage rail mounting R44 and removing R43 resistor.

Figure 3-15. Voltage Monitor Circuit

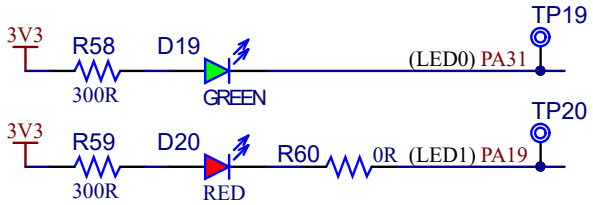


3.4.2 LEDs

The PL485-EK board includes the following LEDs:

- D9 and D12, connected to 5V and 3.3V supplies respectively to provide a visual status of these voltages
- D15 to indicate the transmission of PL485
- D18 to indicate the status of USB
- D22 to indicate the J-Link status
- D19 and D20 for general purpose, one green connected to PA31 (LED0) and one red connected to PA19 (LED1), which can be managed by the applications

Figure 3-16. User LEDs



3.4.3 Chip Erase

The 1x2 pin-header J1 marked as “MCU ERASE” is connected to the PL485 chip erase pin (PB12) and 3.3V. This header can be used to re-initialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1) by placing a jumper on the header and pressing the reset switch button. After a few seconds, the erase jumper must be removed, the PCB must be turned off and, then, turned on by disconnecting and connecting again to the power supply.

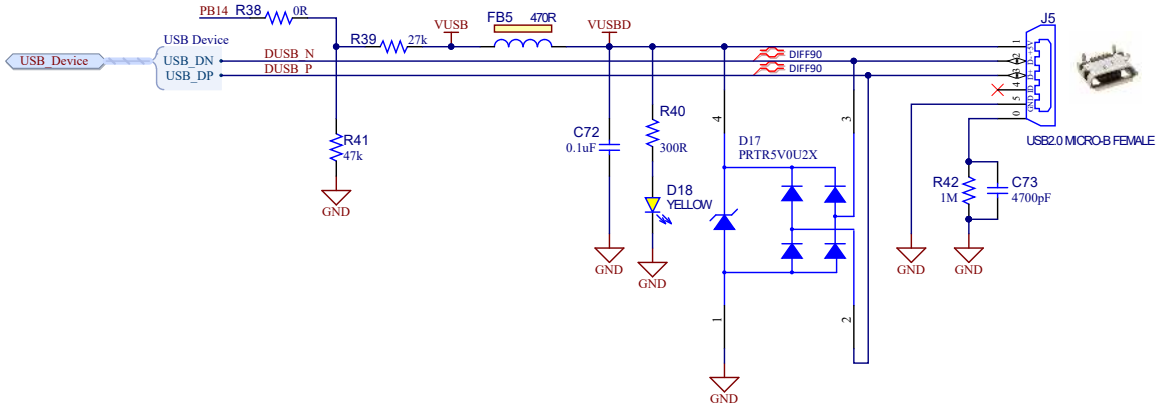
3.5 Hardware Description – MCU Interface Ports

3.5.1 USB Device Port

The USB Device Port (UDP) is compliant with the Universal Serial Bus (USB) 2.0 full-speed device specification. There is a USB available on the PL485-EK board that can act as both host and device. It has a Micro-B female USB connector with the silk screen USB.

The I/O line PB14 allows the application to check if VUSBD is available.

Figure 3-17. USB Circuit



Important: Check online resources from the Microchip Website to download the drivers according to your Operating System.

⚠ CAUTION We recommend the use of an external USB isolator device, for instance UH401, to prevent the addition of noise to the PLC network.

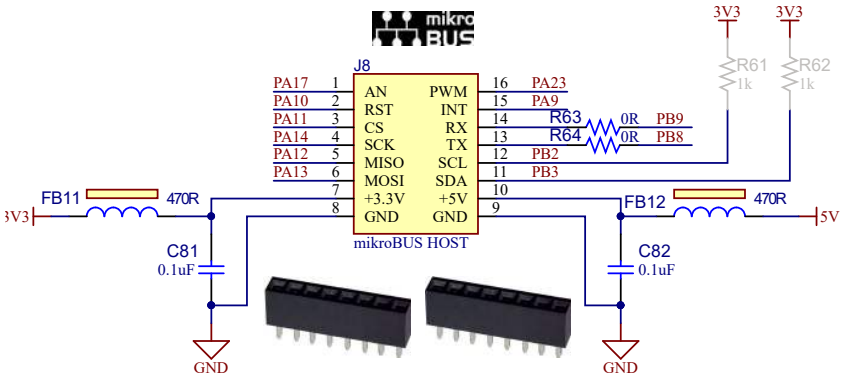
3.5.2 mikroBUS Connector

The PL485-EK board incorporates a mikroBUS socket connector (J8). By means of this socket, some mikroBUS peripherals can be connected to PL485-EK, which is the main board.

This mikroBUS standard defines two pairs of 1x8 male headers with the following signals:

- Analog
- Reset
- SPI Chip Select
- SPI Clock
- SPI Master Input Slave Output
- SPI Master Output Slave Input
- Regulated +3.3V (output)
- Unregulated +5V (output)
- I²C Data
- I²C Clock
- UART Transmit
- UART Receive
- Hardware Interrupt
- Pulse-width Modulation
- Two GND pins

Figure 3-18. mikroBUS Connector

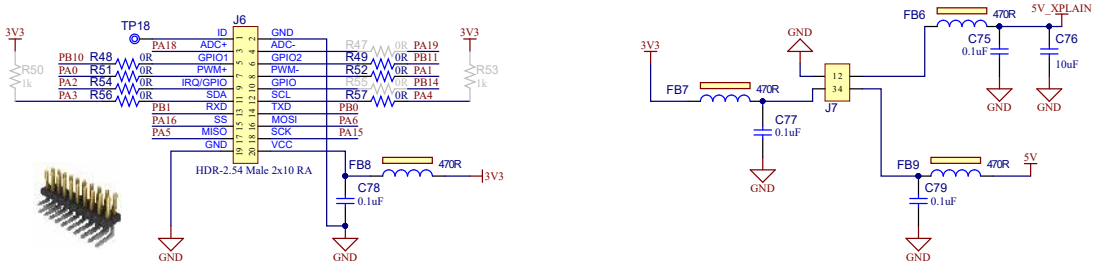


Note: R61 and R62 must be mounted in case a pull-up for the I2C line will be necessary.

3.5.3 Xplained PRO Header

All Xplained Pro kits have one or more dual row, 20-pin, 100mil extension header. Xplained Pro MCU boards have male headers. The extension headers can be used to connect a variety of Xplained Pro extensions to Xplained Pro MCU boards or to access the pins of the target MCU on Xplained Pro MCU boards directly. Note that all pins are not always connected. All connected pins follow the defined pin-out description in the Table 3-5.

Figure 3-19. Xplained PRO Header Connector (EXT1)



The power header can be used to connect external power to the PL485 Xplained Pro kit. The kit will automatically detect and switch to any external power if supplied. The power header can also be used as supply for external peripherals or extension boards.

Please refer to Table 3-6 for more information about connectors.

3.5.4 I²S

I²S (Inter-IC Sound) is an electrical serial bus interface standard used for connecting digital audio devices together. It is used to communicate PCM audio data between integrated circuits in an electronic device. The I²S bus separates clock and serial data signals, resulting in simpler receivers than those required for asynchronous communications systems that need to recover the clock from the data stream.

Table 3-17. Modifications to enable the I²S Function

Resistor for Xplained PRO Function	Needed Resistors for I²S Function
R51	R68
R52	R69
R54	R67
R56	R66
R57	R65

The default assembly of PL485-EK does not enable the I²S function. So, it is necessary to shift to the right the indicated resistors on Table 3-17.

Figure 3-20. Position of resistors to be shifted for enabling I²S function

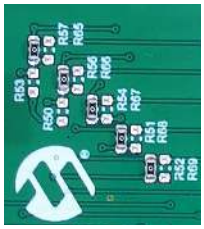
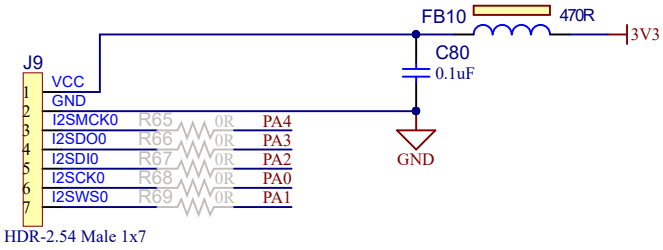


Figure 3-21. I²S Connector



Please refer to Table 3-8 for more information about connector.

3.6 Hardware Description - JLINK Debugger

The PL485-EK includes a built-in SEGGER J-Link-On-Board (J-Link-OB) device. The functionality is implemented with an ATSAM3U4C microcontroller in a TFBGA100 package. The ATSAM3U4C provides the functions of the JTAG interface and a bridge from USB to Serial debug port (known as CDC, or communication class device). The bicolored LED (D22) shows the status of the J-Link-On-Board device. The J-Link-OB device is designed to provide an efficient, low-cost, on-board alternative to the standard J-Link or Atmel-ICE. Its own dedicated USB port acts as a power source for this block and provides the communication link to program and debug the MCU.

Figure 3-22. JLINK OBD Interface

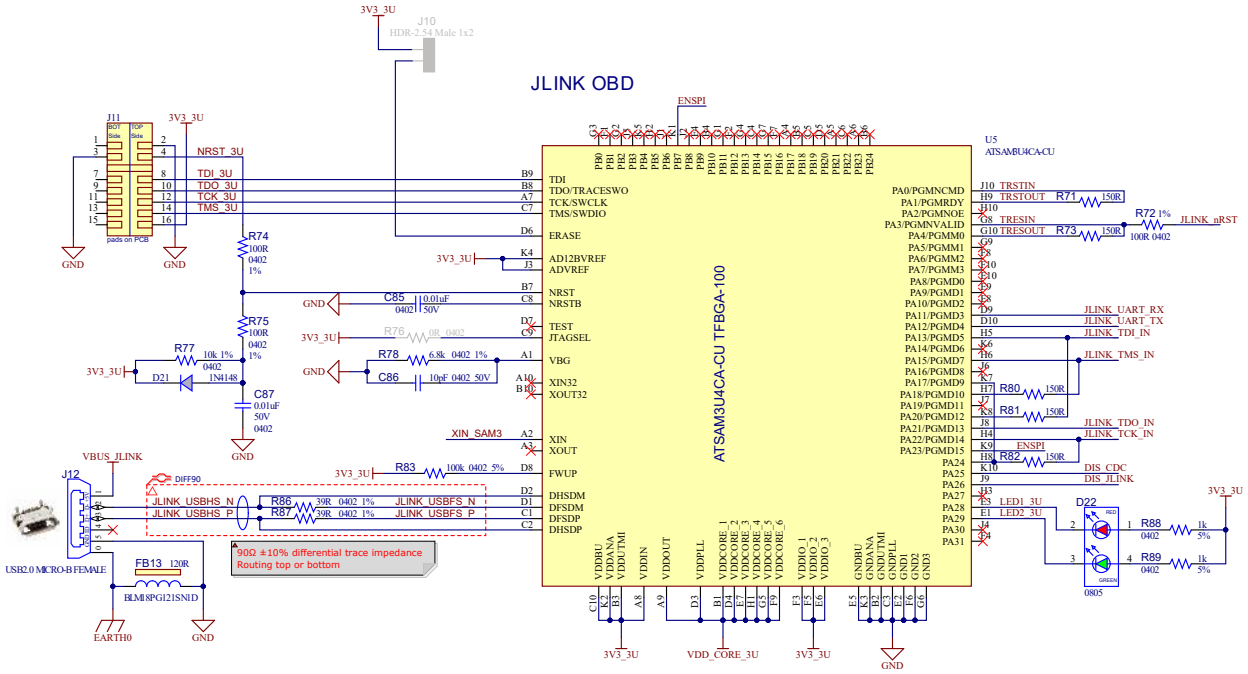


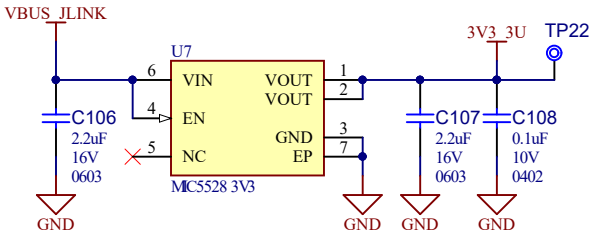
Table 3-18. J-Link-OBD and J-Link-CDC LED D22 Status

LED D22	State	Description
Red and Green	Off	J-Link (SAM3U device) is not programmed, or J13 and J14 are installed.
Green	Flashing	J-Link is operational but the USB port is not connected.
Green	On	J-Link-OB is connected and ready.

The ATSAM3U microcontroller is powered only through the J-Link USB connector.

The MIC5528 has been selected to convert the 5V coming from the USB connector into the 3.3V rail needed by the microcontroller. The MIC5528 is a simple low-power, low dropout regulator designed for optimal performance in a very small footprint. It is capable of sourcing up to 500 mA of output current while only drawing 38 µA of operating current. For more information about the MIC5528, refer to the product web page.

Figure 3-23. J-Link-OBD Power Supply



Jumper J14 disables the J-Link-OBD JTAG functionality. When installed (J14 shorted), a quad analog switch (U4/ U6) routes the JTAG interface of the PL485 to the 10-pin header J15 (Please refer to section 3.6.1 JTAG/SWD Port for more information).

- Jumper J14 not installed: J-Link-OBD-ATSAM3U4C is enabled and fully functional.
- Jumper J14 installed: J-Link-OBD-ATSAM3U4C is disabled and an external JTAG controller can be used through the 10-pin JTAG port J15.

Figure 3-24. Disable JLINK JTAG

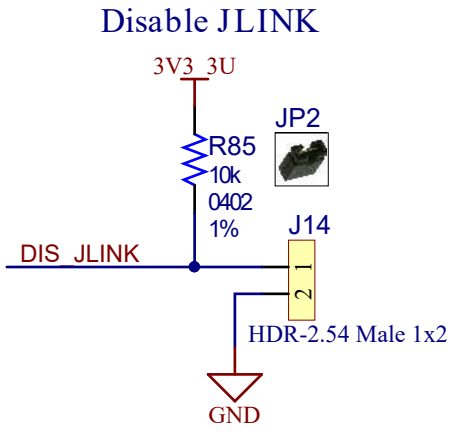
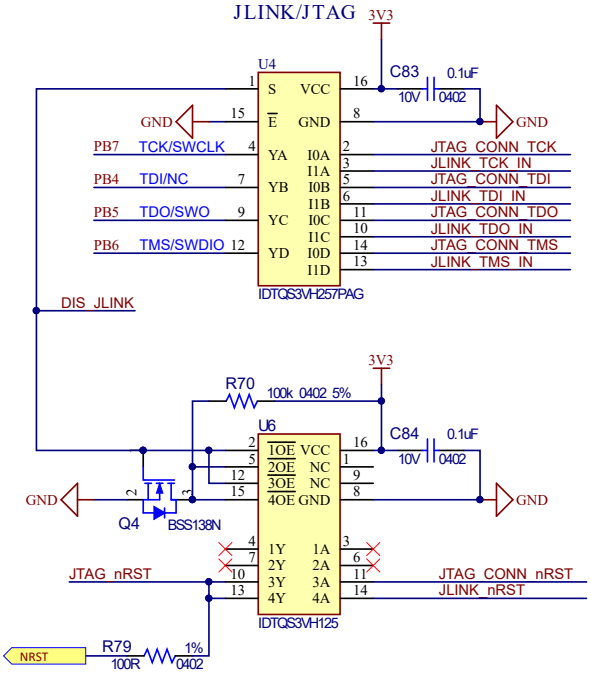


Figure 3-25. JLINK/JTAG Switch



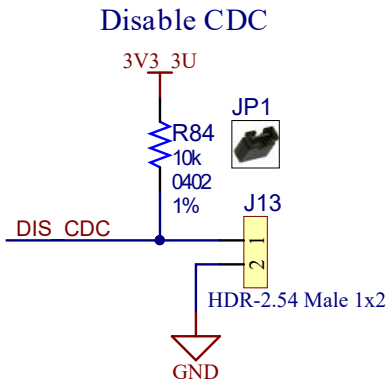
In addition to the J-Link-OBD functionality, the ATSAM3U4C microcontroller provides a bridge to a debug serial port (DBGU) of the main board processor. The port is made accessible over the same USB connection used by JTAG by implementing a Communication Device Class (CDC), which allows a terminal communication with the target device.

This feature is enabled/disabled by jumper J13.

- Jumper J13 not installed: the J-Link-OBD CDC function is enabled and fully functional.
- Jumper J13 installed: the J-Link-OBD CDC function is disabled.

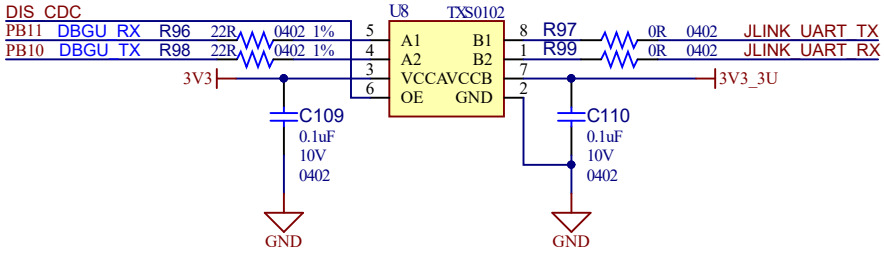
The USB CDC converts the USB device into a serial communication device. The target device running the CDC is recognized by the host as a serial interface (USB2COM, virtual COM port) without the need of installing a special host driver (the CDC is standard). All PC software using a COM port works without modifications with this virtual COM port. Under Microsoft® Windows® , the device shows up as a COM port; under Linux® , as a /dev/ACMx device. This enables the user to use host software which was not designed to be used with USB, such as a terminal program.

Figure 3-26. Disable JLINK CDC



If the user does not require the on-board programming feature, this section can be left unpowered, with no impact on the rest of the system. A level shifter has been placed on the DEBUG UART line between the PL485 MCU and the on-board programmer to properly separate the two voltage domains.

Figure 3-27. J-Link-OBD Level Shifter

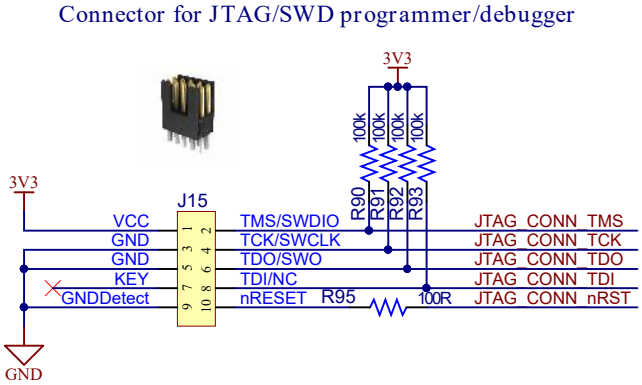


3.6.1 JTAG/SWD Port

The PL485-EK board includes an SWD (Serial Wire Debug) / JTAG interface port to provide debug level access to the system-on-chip. It also embeds a serial wire trace. This connector provides the required interface for in-circuit emulators, like the Atmel-ICE. The SW-DP/JTAG port is a 10-pin, dual row, 0.1-inch male connector (J15).

Important: Note that the PL485-EK kit does not include any external JTAG debugger/programmer.

Figure 3-28. JTAG/SWD Interface Schematic



3.7 PL485-EK Schematics

This section contains the schematics for the PL485-EK board:

- Top Level Schematic, Figure 3-29
- PL485 Schematic, Figure 3-30
- Interface Schematic, Figure 3-31
- Power Supply Schematic, Figure 3-32
- PLC Coupling Schematic, Figure 3-33
- JLINK Debugger Schematic, Figure 3-34

Figure 3-29. Top Level Schematic

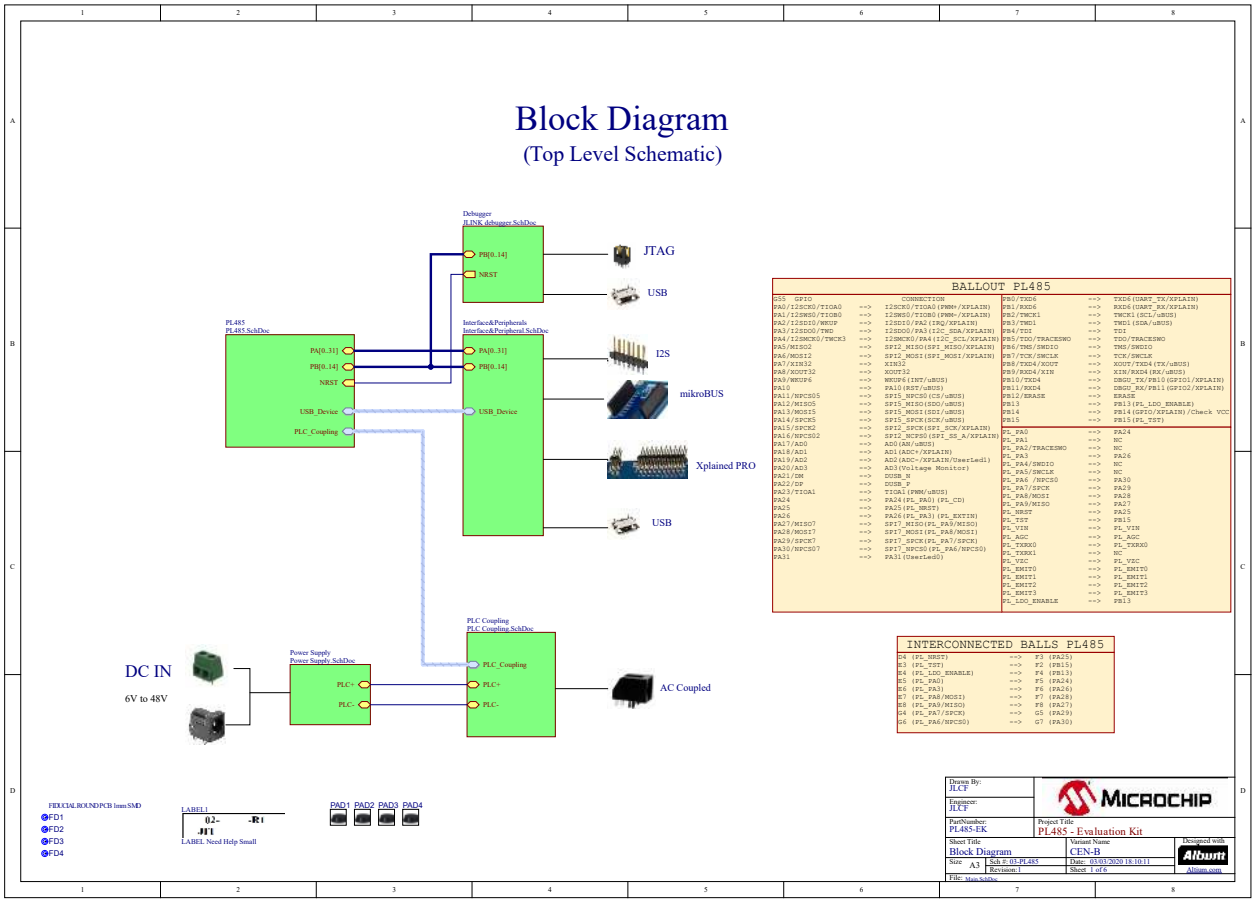


Figure 3-30. PL485 Schematic

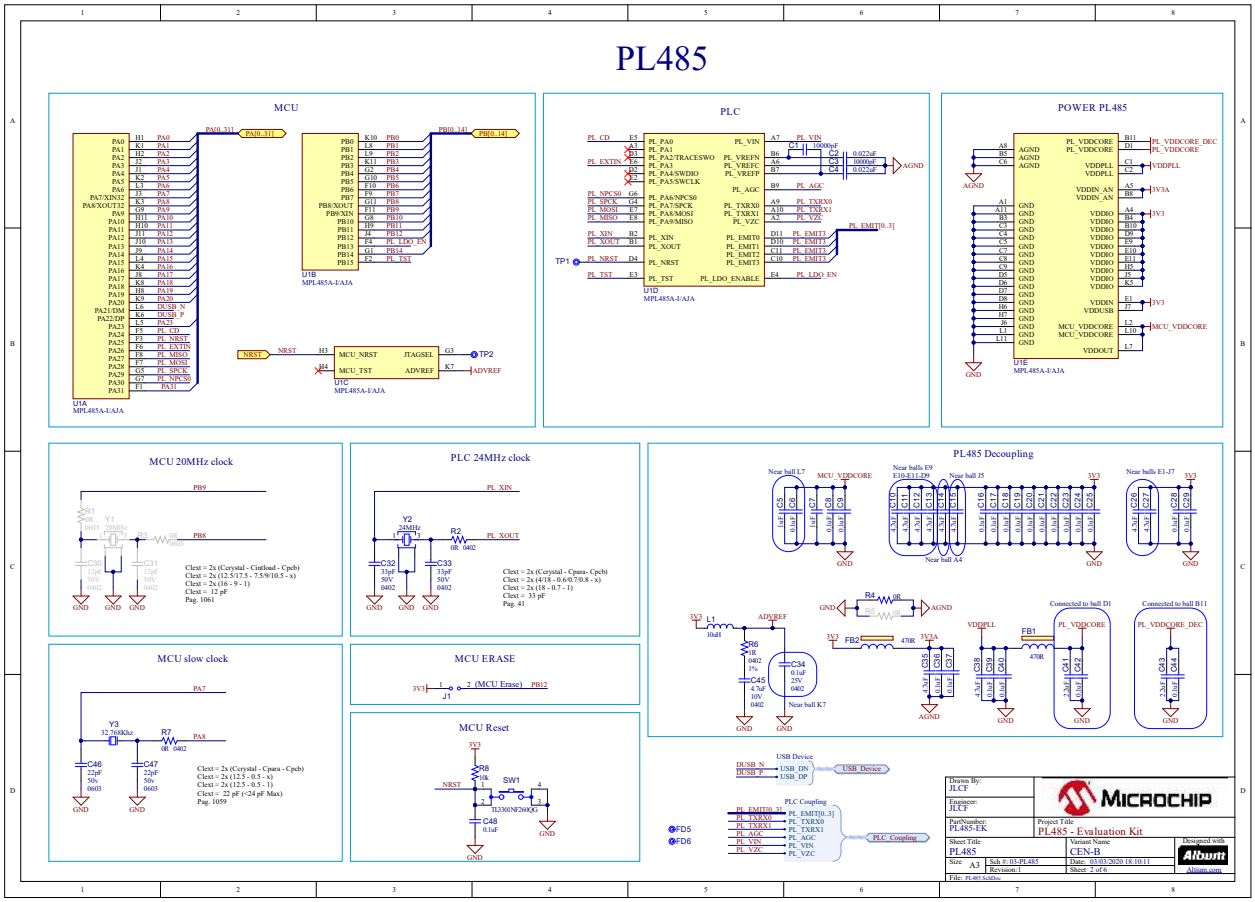


Figure 3-31. Interface Schematic

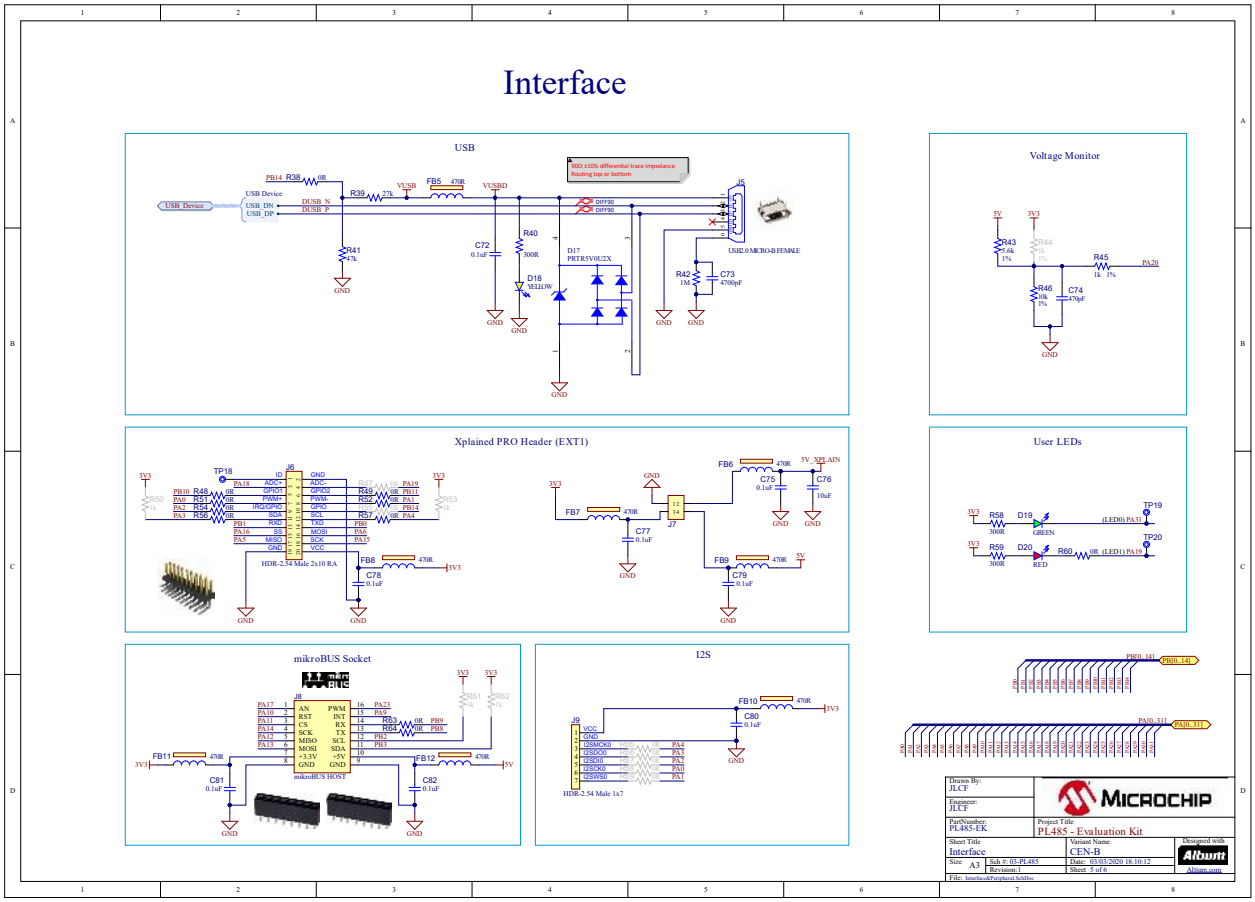


Figure 3-32. Power Supply Schematic

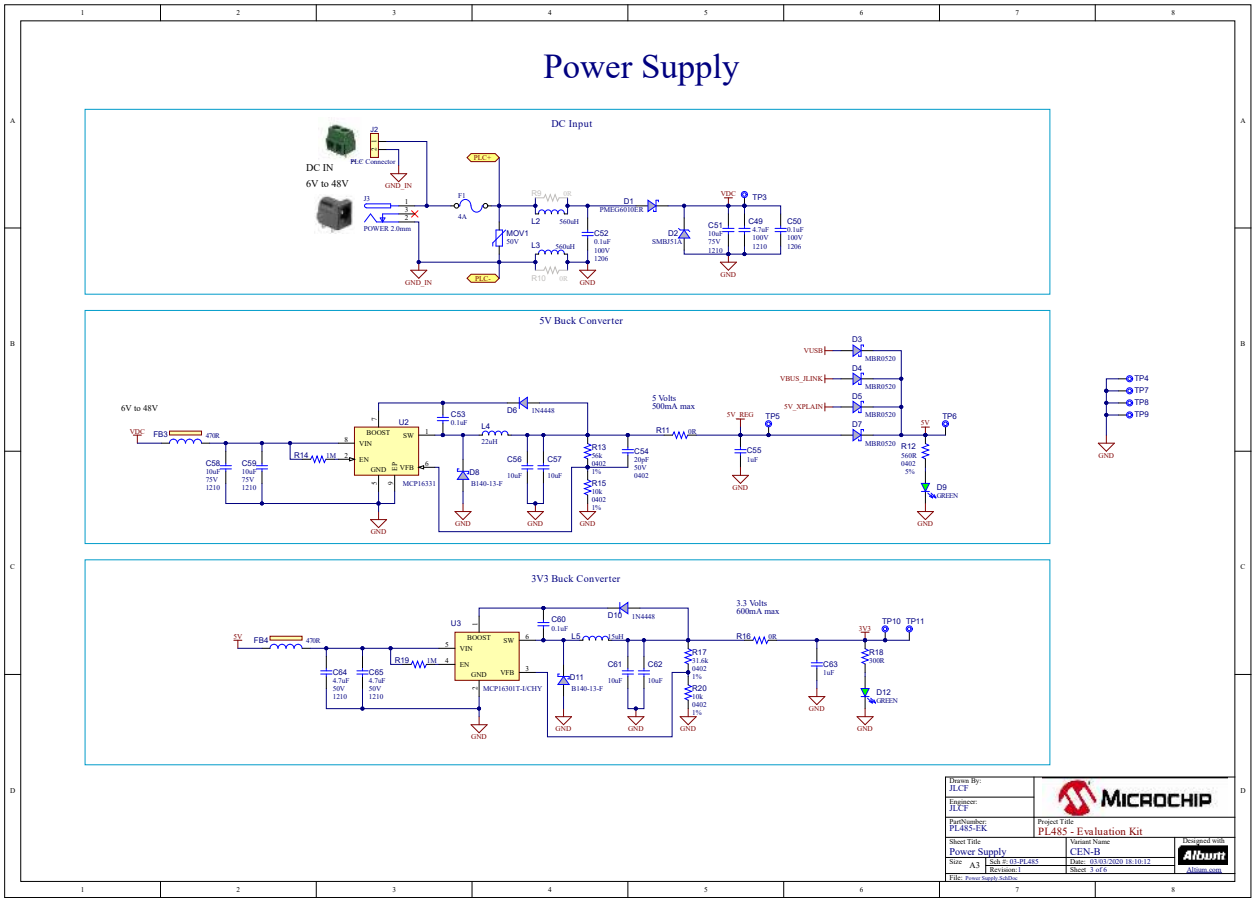


Figure 3-33. PLC Coupling Schematic

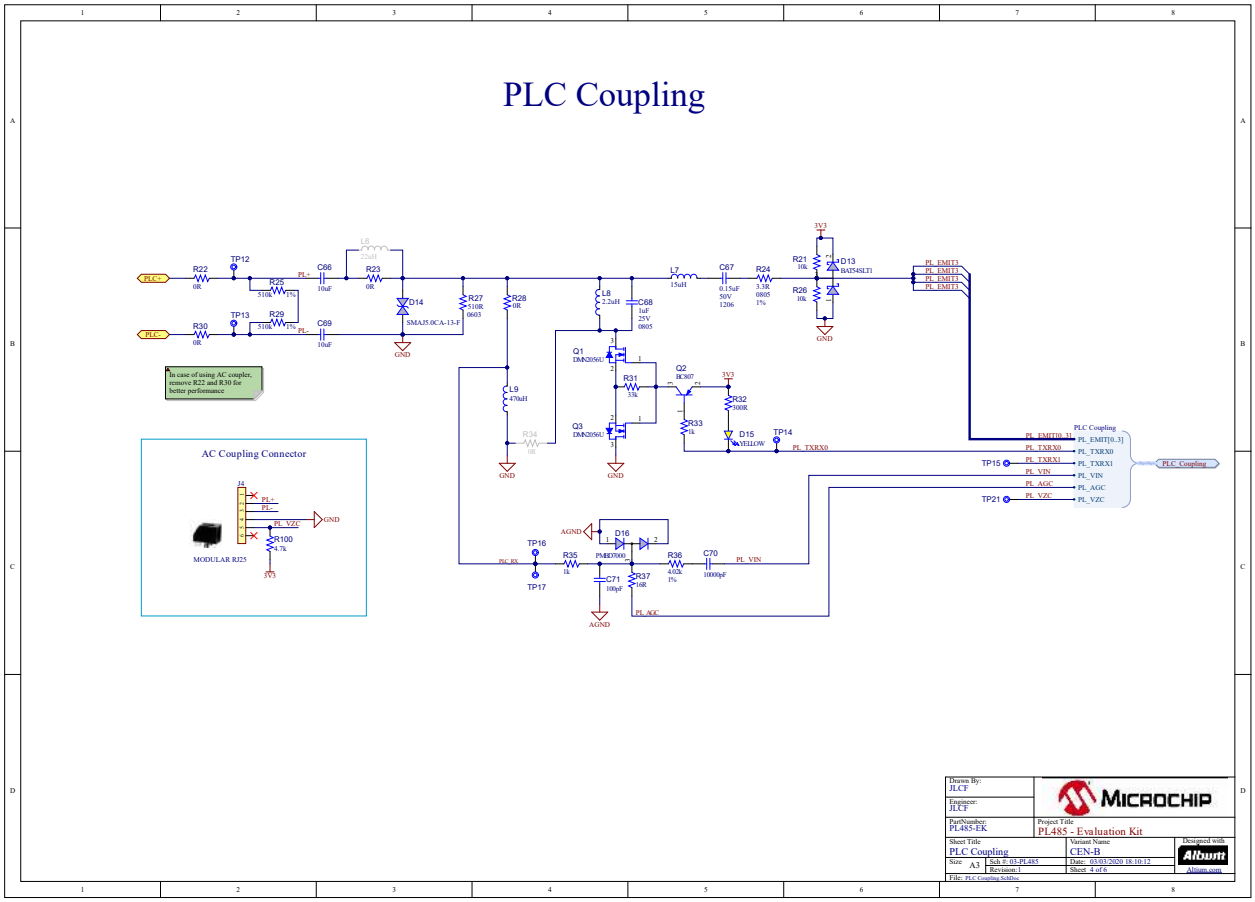
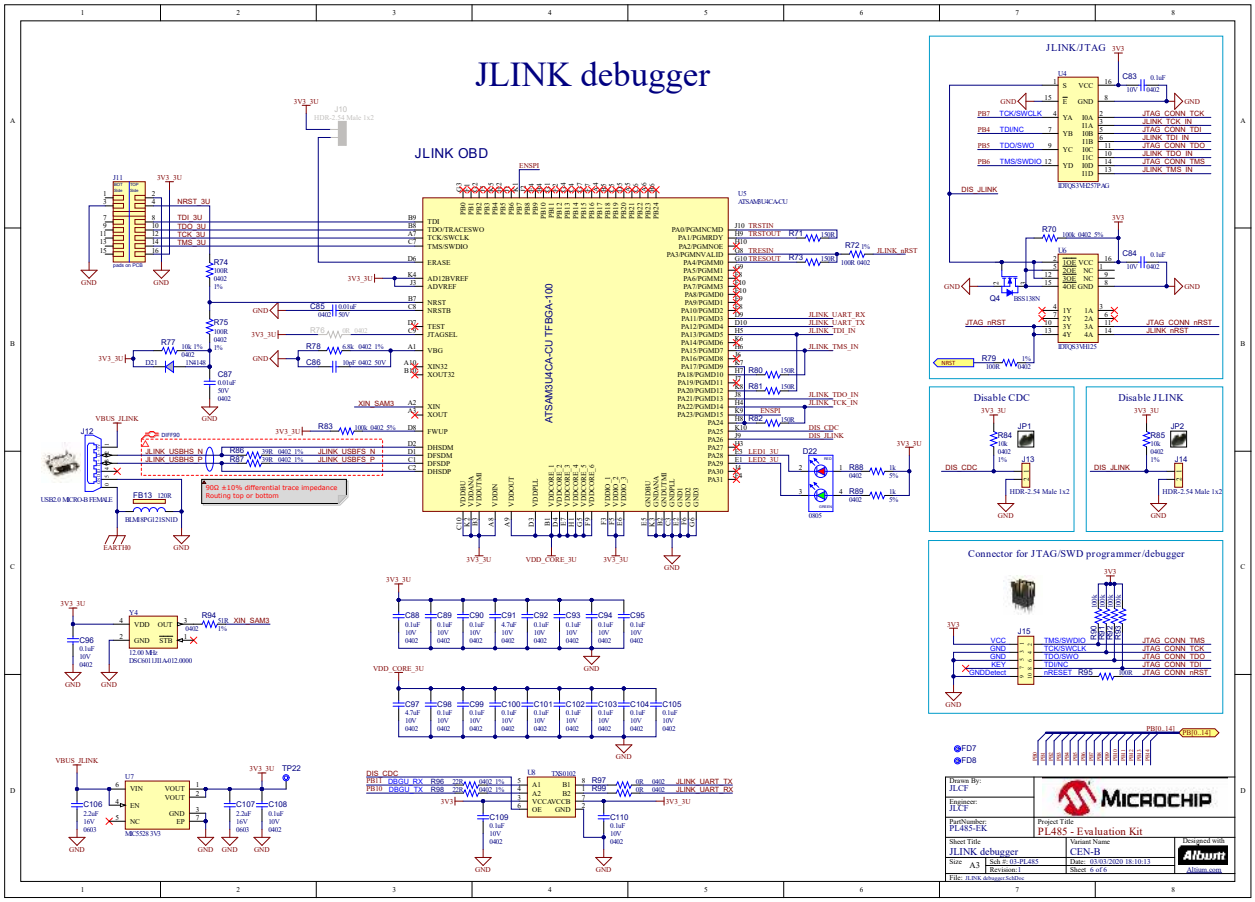


Figure 3-34. JLINK Debugger Schematic



3.8 PL485-EK Layout

This section contains the layout graphics for the PL485-EK board:

- Layer 1: Top Layer, Figure 3-35
- Layer 2: Mid Layer 1 (Ground), Figure 3-36
- Layer 3: Mid Layer 2 (Power Supplies), Figure 3-37
- Layer 4: Bottom Layer, Figure 3-38
- Top Components Placement, Figure 3-39
- Bottom Components Placement, Figure 3-40

Figure 3-35. PL485-EK rev1 Layout: Top Layer

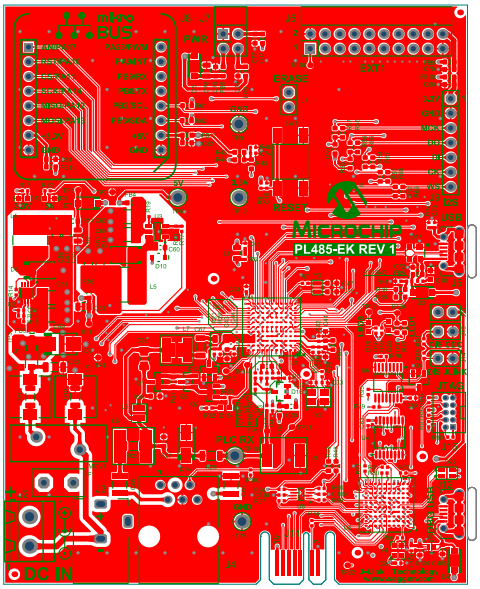


Figure 3-36. PL485-EK rev1 Layout: Mid Layer 1 (Ground)

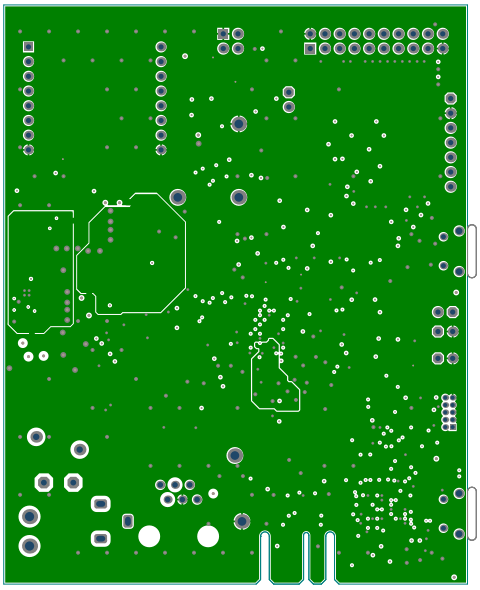


Figure 3-37. PL485-EK rev1 Layout: Mid Layer 2 (Power Supplies)

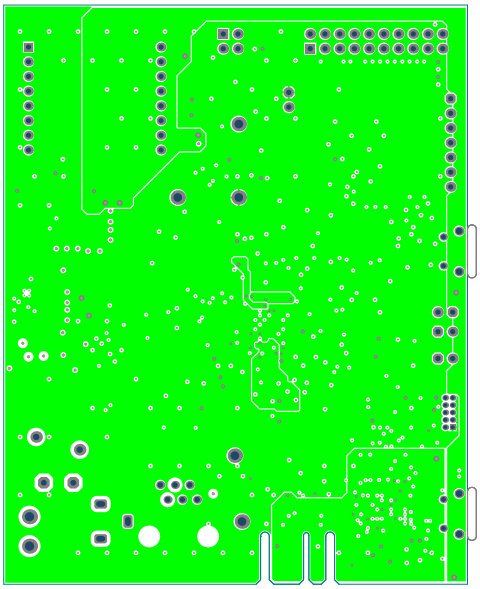


Figure 3-38. PL485-EK rev1 Layout: Bottom Layer

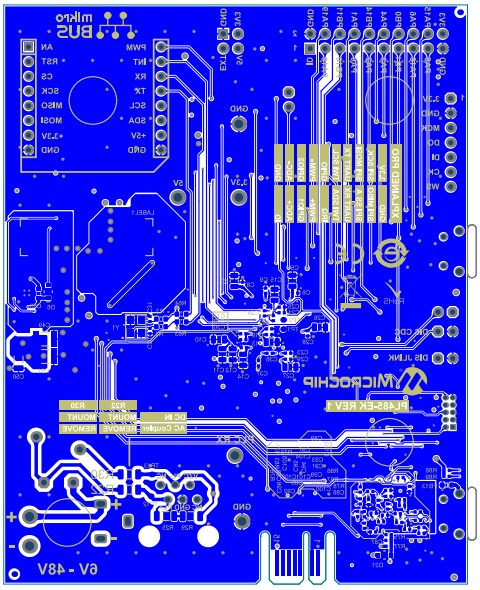


Figure 3-39. PL485-EK rev1 Layout: Top Silkscreen

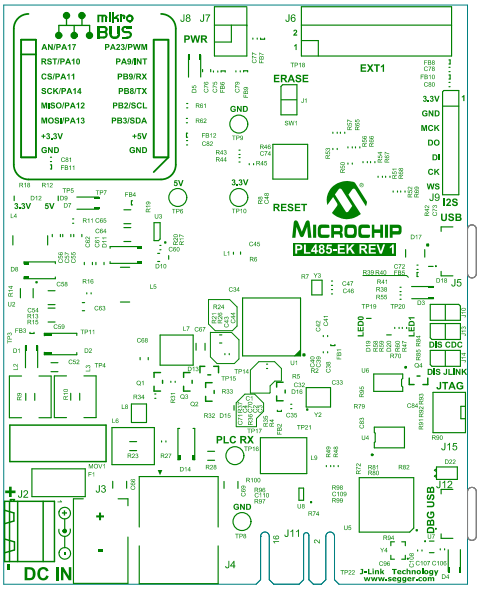
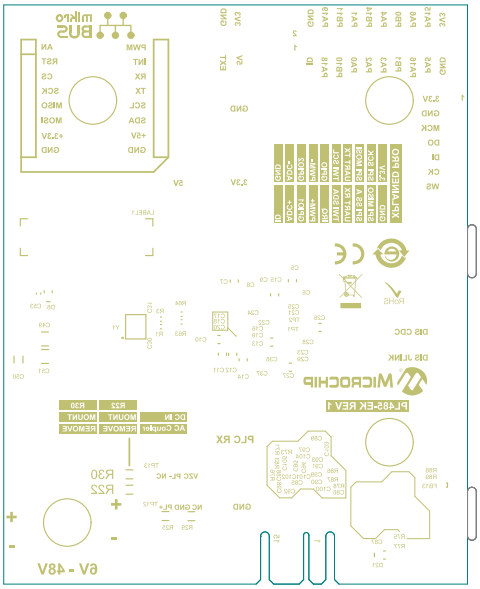


Figure 3-40. PL485-EK rev1 Layout: Bottom Silkscreen



4. Standards Compliance

This development/evaluation tool is designed to be used for research and development in a laboratory environment. This development/evaluation tool is neither intended to be a finished appliance, nor is it intended for incorporation into finished appliances that are made commercially available as single functional units to end users.

The PL485-EK board is a CE mark product which complies with EN 50065-1, EN 50065-2-3 and EN 50065-7 EMC standards. It also complies with the Pb-Free and ROHS directives.

5. References

- CENELEC, EN 50065. Signaling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz, 2002
- PL485 Datasheet, 2020
- PLC-AC-Coupler User Guide, 2020
- Using PL485 to implement a fully featured G3-PLC/PRIME modem Application Note, 2020
- MCP16331 High-Voltage Input Buck Converter Evaluation Board User's Guide, 2014
- MCP16331 Datasheet, 2016
- MCP16301/MCP16301H Data Sheet, 2015

6. Revision History

6.1 Rev A - 01/2020

Document	Initial release.

6.2 Rev B - 05/2020

Document	Minor changes of nomenclature.
Introduction	Added reference to PLC-AC-Coupler User Guide.
1. Evaluation Kit Specifications	Updated 1.1 Safety Recommendations section. Added Table 1-2 in 1.2 Electrical Characteristics section.
2. Getting Started	Updated 2.1 Running the Demo Application section.
3. PL485-EK Board	Updated Figure 3-1 in 3.1 Overview section. Updated Figure 3-2 in 3.2.1 PL485-EK Block Diagram section. Updated Figure 3-3 in 3.2.2 Interface Connection section. Updated Table 3-5, Table 3-6 and Table 3-8 in 3.2.2.1 Connectors section. Updated 3.3.1 PL485 section. Deleted note in 3.3.2 PLC Coupling Circuitry Description section. Added reference to PLC-AC-Coupler User Guide in 3.3.2.2 PLC Coupling Circuit section. Updated 3.3.3 Clock Circuitry section. Updated 3.3.5 Power Supply System section. Updated 3.3.5.1 PLC Rejection Filter section. Deleted note in 3.4.1 Voltage Monitor section. Updated 3.4.2 LEDs section. Updated 3.5.3 Xplained PRO Header section. Updated Figure 3-29, Figure 3-30, Figure 3-31, Figure 3-32, Figure 3-33 and Figure 3-34 in 3.7 PL485-EK Schematics section. Updated Figure 3-35, Figure 3-36, Figure 3-37, Figure 3-38, Figure 3-39 and Figure 3-40 in 3.8 PL485-EK Layout section.
5. References	Added *PLC-AC-Coupler* User Guide. Added *Using PL485 with external amplifier* Application Note.

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