HARRIS SEMICONDUCTOR

CD74HC354, CD74HCT354

High Speed CMOS Logic 8-Input Multiplexer/Register, Three-State

November 1997

Features

- CD74HC/HCT354
  - Transparent Data and Select Latches
- Buffered Inputs
- Three-State Complementary Outputs
- Bus Line Driving Capability
- Typical Propagation Delay: V_{CC} = 5V, C_L = 15pF, T_A = 25°C
  - Data to Output (354) = 18ns
  - Clock to Output (356) = 22ns
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The Harris CD74HC354 and CD74HCT354 are data selectors/multiplexers that select one of eight sources. In both types, the data select bits S0, S1 and S2 are stored in transparent latches that are enabled by a low latch enable input, $\overline{LE}$.

In the HC/HCT354 the data enable input, $\overline{E}$, controls transparent latches that pass data to the outputs when $\overline{E}$ is high and latches in new data when $\overline{E}$ is low.

In both types the three-state outputs are controlled by three output-enable inputs $\overline{OE1}$, $\overline{OE2}$, and OE3.

Ordering Information

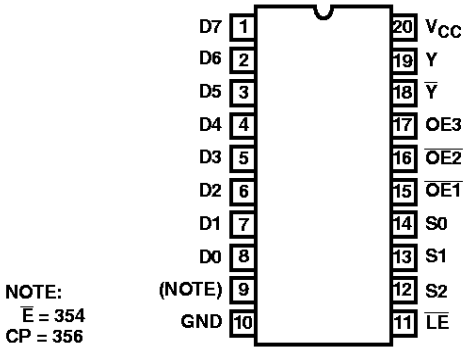
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC354E	-55 to 125	20 Ld PDIP	E20.3
CD74HCT354E	-55 to 125	20 Ld PDIP	E20.3

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

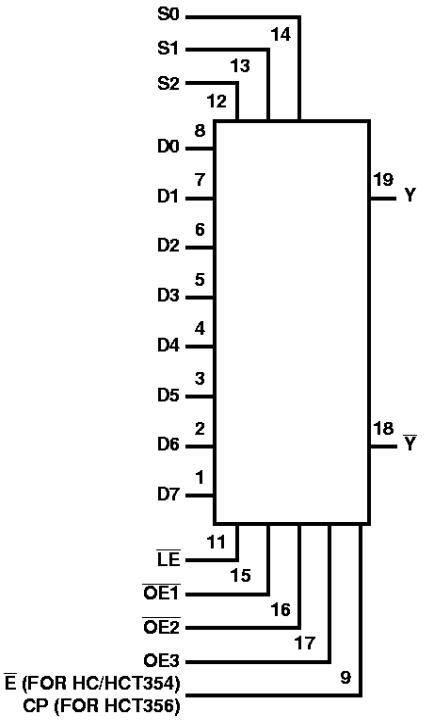
CD74HC354, CD74HCT354
(PDIP)
TOP VIEW



NOTE:
$\overline{E}$ = 354
CP = 356

File Number **1690.1**

Functional Diagram



TRUTH TABLE

INPUTS								OUTPUTS	
SELECT (NOTE 3)			ENABLE DATA HC354 HCT354	CLOCK HCT356	OUTPUT ENABLES				
S2	S1	S0	$\overline{E}$	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	$\overline{Y}$	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$

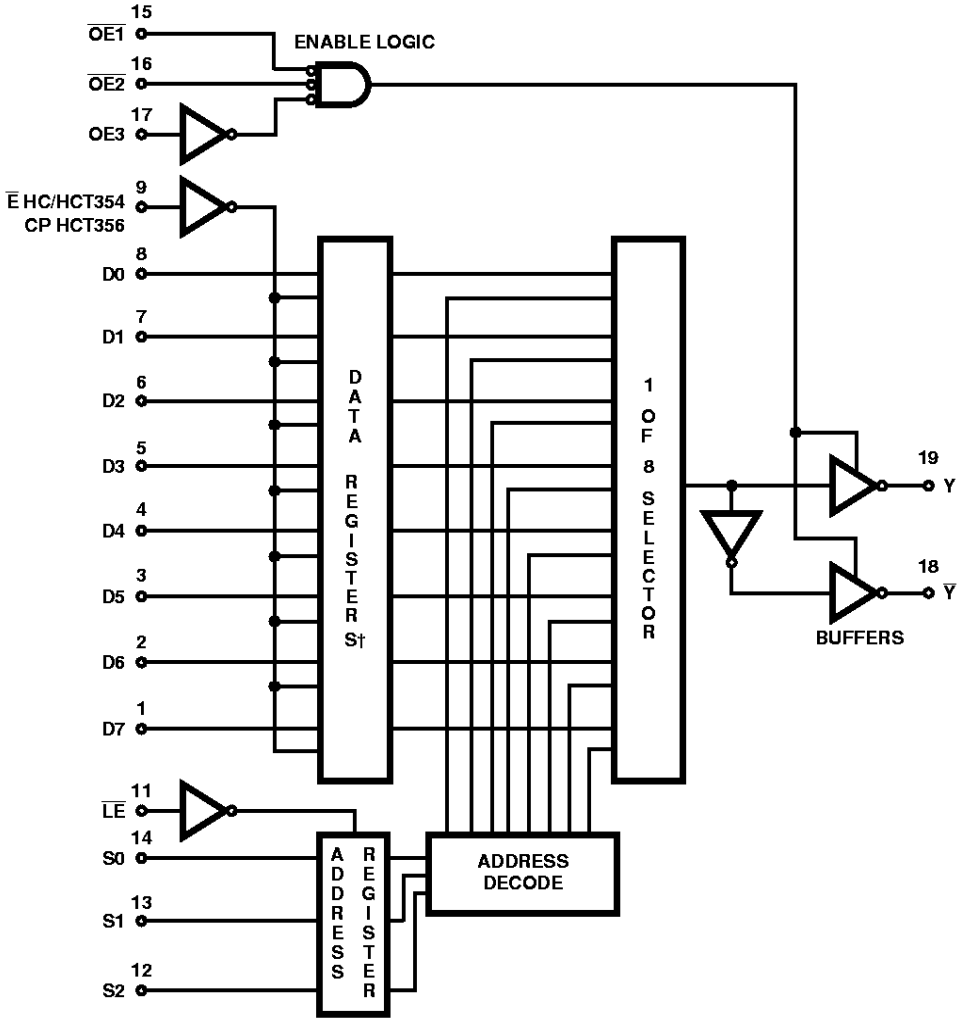
TRUTH TABLE (Continued)

INPUTS								OUTPUTS	
SELECT (NOTE 3)			ENABLE DATA HC354 HCT354	CLOCK HCT356	OUTPUT ENABLES				
S2	S1	S0	$\overline{E}$	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	$\overline{Y}$	Y
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

NOTE: H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); X = Don't Care; Z = High Impedance State (Off State); ↑ = Transition from Low to High Level; D0...D7 = Level of steady-state inputs at input D0 through D7, respectively, at the time of the low-to-high clock transition in the case of HC356; $D0_n$...$D7_n$ = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock.

3. This column shows the input address setup with $\overline{LE}$ low.

Block Diagram



†354 8-Latches, 356 8-F/Fs.

Logic Diagram

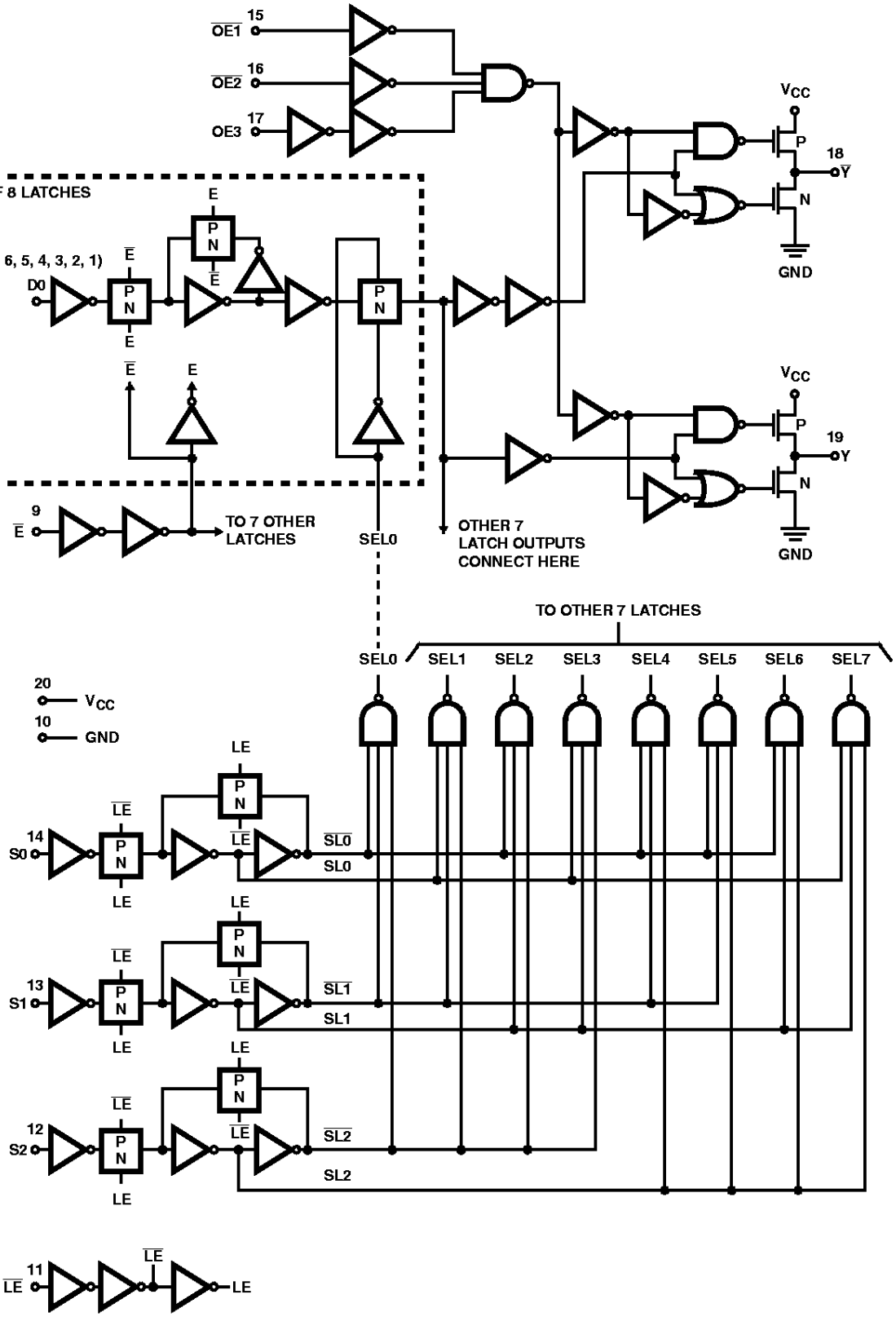


FIGURE 1. HC/HCT354 LOGIC DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V. . . . . ±35mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
PDIP Package 125
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads (Bus Driver)			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads (Bus Driver)			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	V_O = V_{CC} or GND	6	-	-	±0.5	-	±5.0	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 5)	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	V_O = V_{CC} or GND	5.5	-	-	±0.5	-	±5.0	-	±10	µA

NOTE:

5. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
HCT354	
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE1}$, $\overline{OE2}$	0.80
OE3	0.25
$\overline{LE}$	0.25
$\overline{E}$	0.60

HCT Input Loading Table (Continued)

INPUT	UNIT LOADS
HCT356	
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE1}$, $\overline{OE2}$	0.80
OE3	0.25
$\overline{LE}$	0.25
CP	0.60

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Prerequisite For Switching Specifications - HC/HCT354

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
$\overline{E}$ Pulse Width	t_{PLH}, t_{PHL}	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
$\overline{LE}$ Pulse Width	t_{PLH}, t_{PHL}	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Set-up Times Dn → $\overline{E}$	t_{SU}	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Set-up Times Sn → $\overline{LE}$	t_{SU}	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Hold Times Dn → $\overline{E}$	t_H	-	2	45	-	-	55	-	70	-	ns
			4.5	9	-	-	11	-	14	-	ns
			6	8	-	-	9	-	12	-	ns
Hold Times Sn → $\overline{LE}$	t_H	-	2	45	-	-	55	-	70	-	ns
			4.5	9	-	-	11	-	14	-	ns
			6	8	-	-	9	-	12	-	ns
HCT TYPES											
$\overline{E}$ Pulse Width	t_{PLH}, t_{PHL}	-	4.5	16	-	-	20	-	24	-	ns
$\overline{LE}$ Pulse Width	t_{PLH}, t_{PHL}	-	4.5	16	-	-	20	-	24	-	ns
Set-up Times Dn → $\overline{E}$	t_{SU}	-	4.5	10	-	-	13	-	15	-	ns
Set-up Times Sn → $\overline{LE}$	t_{SU}	-	4.5	10	-	-	13	-	15	-	ns
Hold Times Dn → $\overline{E}$	t_H	-	4.5	9	-	-	11	-	14	-	ns
Hold Times Sn → $\overline{LE}$	t_H	-	4.5	9	-	-	11	-	14	-	ns

Switching Specifications - HC/HCT354 Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, Dn → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	210	265	315	ns
			4.5	-	42	53	63	ns
			6	-	36	45	54	ns
		C_L = 15pF	5	18	-	-	-	ns
Propagation Delay, $\overline{E}$ → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	250	315	375	ns
			4.5	-	50	63	75	ns
			6	-	43	54	64	ns
		C_L = 15pF	5	21	-	-	-	ns

Switching Specifications - HC/HCT354 Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Propagation Delay, Sn → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	260	325	390	ns
			4.5	-	52	65	78	ns
			6	-	44	55	66	ns
		C_L = 15pF	5	22	-	-	-	ns
Propagation Delay, $\overline{LE}$ → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	290	365	435	ns
			4.5	-	58	73	87	ns
			6	-	49	62	74	ns
		C_L = 15pF	5	24	-	-	-	ns
Output Disabling Time, $\overline{OE}$n to Y, $\overline{Y}$	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	155	195	235	ns
			4.5	-	31	39	47	ns
			6	-	26	33	40	ns
		C_L = 15pF	5	13	-	-	-	ns
Output Disabling Time, OE3 to Y, $\overline{Y}$	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	155	195	235	ns
			4.5	-	31	39	47	ns
			6	-	26	33	40	ns
		C_L = 15pF	5	13	-	-	-	ns
Output Enabling Time, $\overline{OE}$n to Y, $\overline{Y}$	t_{PZL}, t_{PZH}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		C_L = 15pF	5	12, 13	-	-	-	ns
Output Enabling Time, OE3 to Y, $\overline{Y}$	t_{PZL}, t_{PZH}	C_L = 50pF	2	-	160	200	240	ns
			4.5	-	32	40	48	ns
			6	-	27	34	41	ns
		C_L = 15pF	5	12, 13	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	60	75	90	ns
			4.5	-	12	15	18	ns
			6	-	10	13	15	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Three-State Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 6, 7)	C_{PD}	-	5	90	-	-	-	pF
HCT TYPES								
Propagation Delay, Dn → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	47	59	71	ns
		C_L = 15pF	5	20	-	-	-	ns
Propagation Delay, $\overline{E}$ → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	54	68	81	ns
		C_L = 15pF	5	23	-	-	-	ns

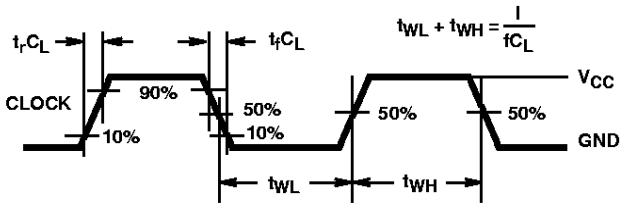
Switching Specifications - HC/HCT354 Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Propagation Delay, Sn → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	59	74	89	ns
		C_L = 15pF	5	25	-	-	-	ns
Propagation Delay, $\overline{LE}$ → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	63	79	94	ns
		C_L = 15pF	5	25	-	-	-	ns
Output Disabling Time, $\overline{OE}$n to Y, $\overline{Y}$	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	33	41	50	ns
		C_L = 15pF	5	13, 16	-	-	-	ns
Output Disabling Time, OE3 to Y, $\overline{Y}$	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	39	49	59	ns
		C_L = 15pF	5	13, 16	-	-	-	ns
Output Enabling Time, $\overline{OE}$n to Y, $\overline{Y}$	t_{PZL}, t_{PZH}	C_L = 50pF	4.5	-	34	43	51	ns
		C_L = 15pF	5	14	-	-	-	ns
Output Enabling Time, OE3 to Y, $\overline{Y}$	t_{PZL}, t_{PZH}	C_L = 50pF	4.5	-	34	43	51	ns
		C_L = 15pF	5	14	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	12	15	18	ns
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF
Three-State Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 6, 7)	C_{PD}	-	5	92	-	-	-	pF

NOTES:

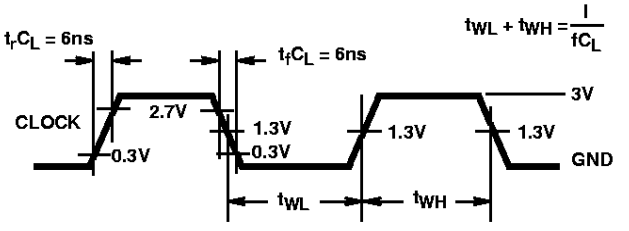
6. C_{PD} is used to determine the dynamic power consumption, per device.
7. $P_D = V_{CC}^2 (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 3. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

Test Circuits and Waveforms (Continued)

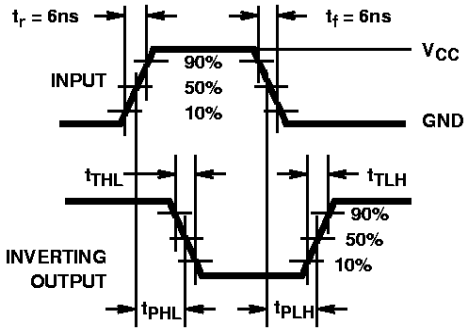


FIGURE 4. HC AND HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

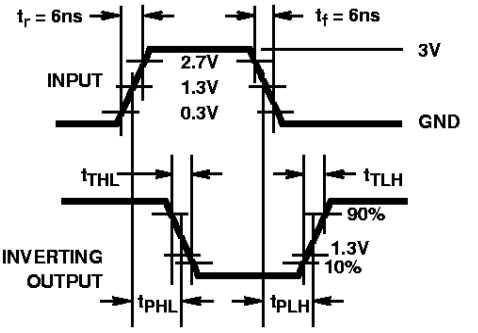


FIGURE 5. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

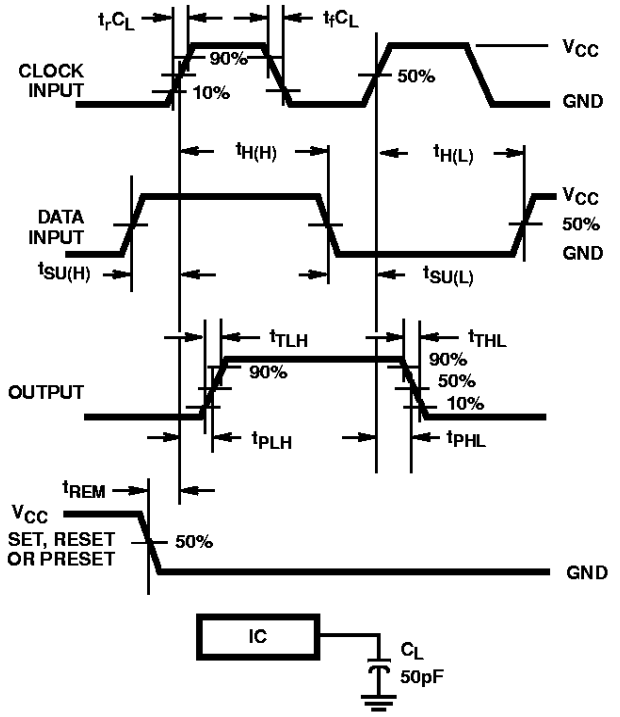


FIGURE 6. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

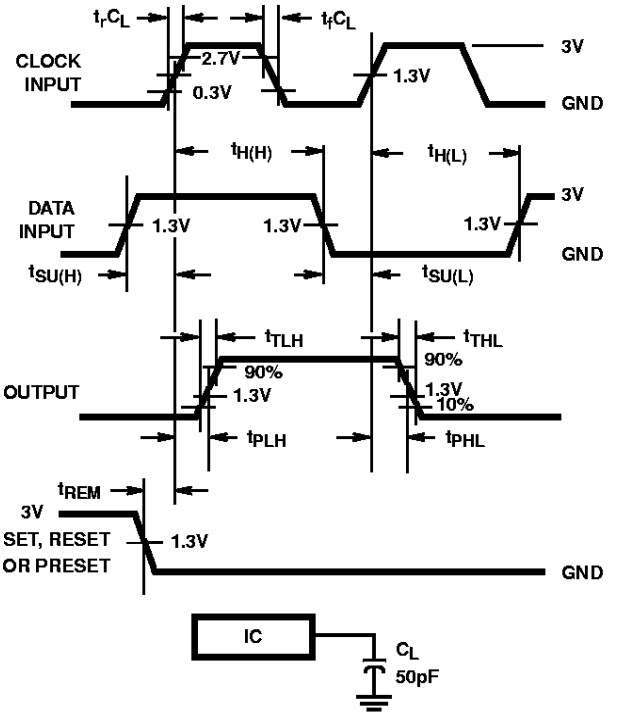


FIGURE 7. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

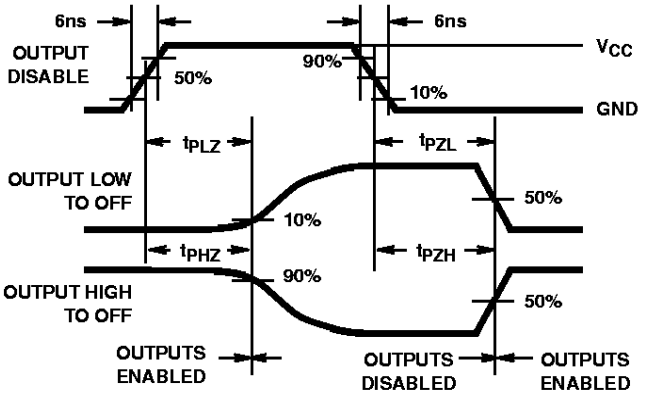


FIGURE 8. HC THREE-STATE PROPAGATION DELAY WAVEFORM

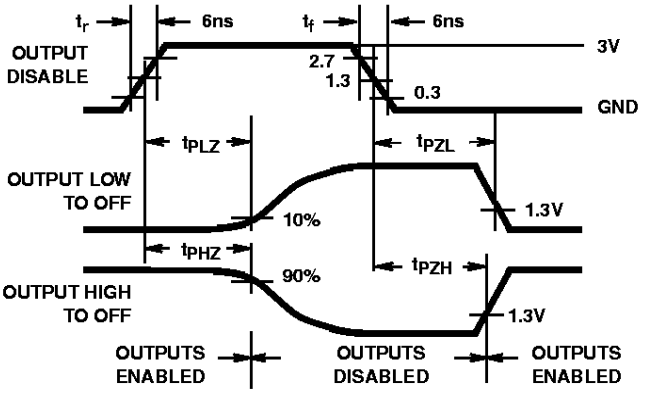
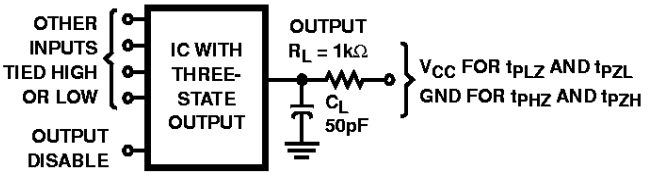


FIGURE 9. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 10. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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