# LMK1D210x Low Additive Jitter LVDS Buffer

## 1 Features

- High-performance LVDS clock buffer family: up to 2 GHz
  – Dual 1:6 differential buffer
  – Dual 1:8 differential buffer
- Supply voltage: 1.71 V to 3.465 V
- Low additive jitter: < 60 fs RMS maximum in 12-kHz to
  20-MHz at 156.25 MHz
  – Very low phase noise floor: -164 dBc/Hz (typical)
- Very low propagation delay: < 575 ps maximum
- Output skew: 20 ps maximum
- High-swing LVDS (boosted mode): 500-mV VOD typical when AMP_SEL = 1
- Bank enable/disable using the EN pin
- Fail-safe input operation
- Universal inputs accept LVDS, LVPECL, LVCMOS, HCSL and CML signal levels
- LVDS reference voltage, $V_{AC_REF}$, available for capacitive-coupled inputs
- Industrial temperature range: –40°C to 105°C
- Packaged in
  – LMK1D2106: 6-mm × 6-mm, 40-pin VQFN (RHA)
  – LMK1D2108: 7-mm × 7-mm, 48-pin VQFN (RGZ)

## 2 Applications

- Telecommunications and networking
- Medical imaging
- Test and measurement
- Wireless infrastructure
- Pro audio, video and signage

## 3 Description

The LMK1D210x clock buffer distributes two clock inputs (IN0 and IN1) to a total of 16 pairs of differential LVDS clock outputs (OUT0 to OUT15) in the LMK1D2108 and 12 pairs of clock outputs (OUT0 to OUT11) in the LMK1D2106 with minimum skew for clock distribution. Each buffer block consists of one input and a maximum of 6 (LMK1D2106) or 8 (LMK1D2108) LVDS outputs. The inputs can either be LVDS, LVPECL, HCSL, CML, or LVCMOS.

The LMK1D210x is specifically designed for driving 50-Ω transmission lines. When driving inputs in single-ended mode, apply the appropriate bias voltage to the unused negative input pin (see Figure 8-6).

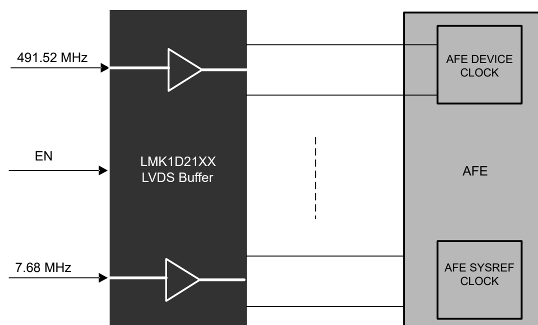
Using the control pin (EN), output banks can either be enable or disabled. If this pin is left open, both bank outputs are enabled. If the control pin is switched to a logic "0", both bank outputs are disabled (static logic "0"). If the control pin is switched to a logic "1", the outputs of one bank are disabled while the outputs of the other bank are enabled. The part also supports a fail-safe function. The device further incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

The device operates in a 1.8-V, 2.5-V, or 3.3-V supply environment and is characterized from –40°C to 105°C (ambient temperature).

**Device Information**

| PART NUMBER(1) | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LMK1D2106 | VQFN (40) | 6.00 mm × 6.00 mm |
| LMK1D2108 | VQFN (48) | 7.00 mm × 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Application Example**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision * (October 2021) to Revision A (January 2022)** **Page**

- Added Fail-safe input operation to the *Features* 1
- Added *Fail-Safe Input* section 15


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# 5 Pin Configuration and Functions

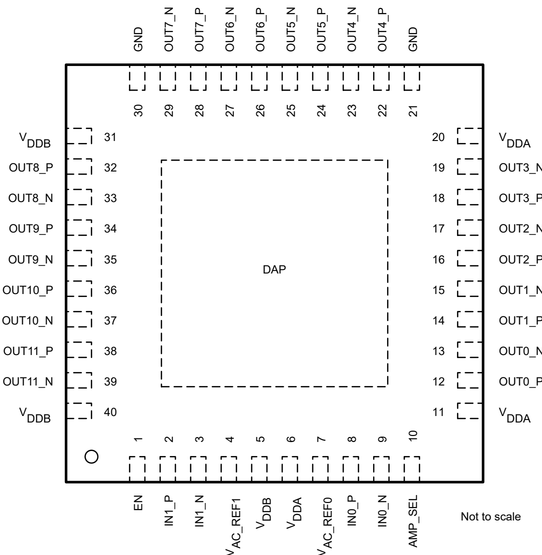


**Figure 5-1. LMK1D2106: RHA Package 40-Pin VQFN Top View**

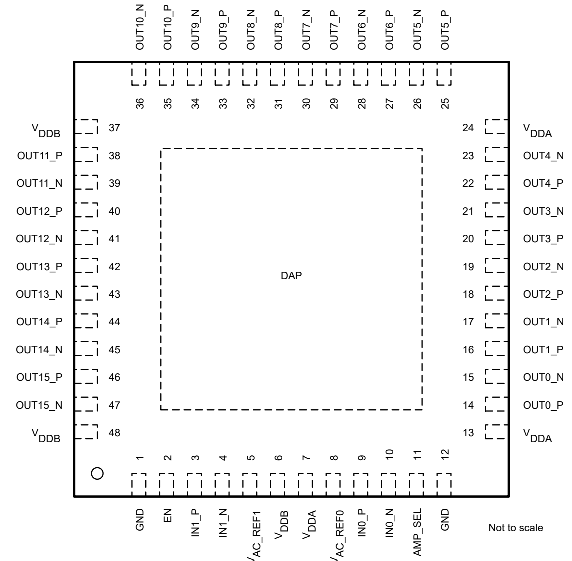


**Figure 5-2. LMK1D2108: RGZ Package 48-Pin VQFN Top View**

**Table 5-1. Pin Functions**

| PIN | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NAME | LMK1D2106 | LMK1D2108 | | |
| **DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT** | | | | |
| IN0_P, IN0_N | 8, 9 | 9, 10 | I | Primary: Differential input pair or single-ended input |
| IN1_P, IN1_N | 2, 3 | 3, 4 | I | Secondary: Differential input pair or single-ended input |
| | | | | Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N. |
| **BANK ENABLE** | | | | |
| EN | 1 | 2 | I | Output bank enable/disable with an internal 500-kΩ pullup and 320-kΩ pulldown. See Table 8-2. |
| **AMPLITUDE SELECT** | | | | |
| AMP_SEL | 10 | 11 | I | Output amplitude swing select with an internal 500-kΩ pullup and 320-kΩ pulldown. See Table 8-3. |
| **BIAS VOLTAGE OUTPUT** | | | | |
| $V_{AC_REF0}$,$V_{AC_REF1}$ | 7, 4 | 8, 5 | O | Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-µF capacitor to GND on this pin. |
| **DIFFERENTIAL CLOCK OUTPUT** | | | | |
| OUT0_P, OUT0_N | 12, 13 | 14, 15 | O | Differential LVDS output pair number 0 |
| OUT1_P, OUT1_N | 14, 15 | 16, 17 | O | Differential LVDS output pair number 1 |
| OUT2_P, OUT2_N | 16, 17 | 18, 19 | O | Differential LVDS output pair number 2 |
| OUT3_P, OUT3_N | 18, 19 | 20, 21 | O | Differential LVDS output pair number 3 |
| OUT4_P, OUT4_N | 22, 23 | 22, 23 | O | Differential LVDS output pair number 4 |
| OUT5_P, OUT5_N | 24, 25 | 25, 26 | O | Differential LVDS output pair number 5 |
| OUT6_P, OUT6_N | 26, 27 | 27, 28 | O | Differential LVDS output pair number 6 |
| OUT7_P, OUT7_N | 28, 29 | 29, 30 | O | Differential LVDS output pair number 7 |
| OUT8_P, OUT8_N | 32, 33 | 31, 32 | O | Differential LVDS output pair number 8 |

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**Table 5-1. Pin Functions (continued)**

| PIN | | | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|---|
| NAME | LMK1D2106 | LMK1D2108 | | |
| OUT9_P, OUT9_N | 34, 35 | 33, 34 | O | Differential LVDS output pair number 9 |
| OUT10_P, OUT10_N | 36, 37 | 35, 36 | O | Differential LVDS output pair number 10 |
| OUT11_P, OUT11_N | 38, 39 | 38, 39 | O | Differential LVDS output pair number 11 |
| OUT12_P, OUT12_N | — | 40, 41 | O | Differential LVDS output pair number 12 |
| OUT13_P, OUT13_N | — | 42, 43 | O | Differential LVDS output pair number 13 |
| OUT14_P, OUT14_N | — | 44, 45 | O | Differential LVDS output pair number 14 |
| OUT15_P, OUT15_N | — | 46, 47 | O | Differential LVDS output pair number 15 |
| **SUPPLY VOLTAGE** | | | | |
| $V_{DDA}$ | 6, 11, 20 | 7, 13, 24 | P | Device power supply (1.8 V, 2.5 V, or 3.3 V) for Bank 0 |
| $V_{DDB}$ | 5, 31, 40 | 6, 37, 48 | P | Device power supply (1.8 V, 2.5 V, or 3.3 V) for Bank 1 |
| **GROUND** | | | | |
| GND | 21, 30 | 1, 12 | G | Ground |
| **MISC** | | | | |
| DAP | DAP | DAP | G | Die Attach Pad. Connect to the printed circuit board (PCB) ground plane for heat dissipation. |

(1) G = Ground, I = Input, O = Output, P = Power

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.3 | 3.6 | V |
| $V_{IN}$ | Input voltage | –0.3 | 3.6 | V |
| $V_O$ | Output voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input current | –20 | 20 | mA |
| $I_O$ | Continuous output current | –50 | 50 | mA |
| $T_J$ | Junction temperature | | 135 | °C |
| $T_{stg}$ | Storage temperature [(2)] | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device unpowered

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)] | ±3000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[(2)] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core supply voltage | 3.3-V supply | 3.135 | 3.3 | 3.465 | V |
| | | 2.5-V supply | 2.375 | 2.5 | 2.625 | |
| | | 1.8-V supply | 1.71 | 1.8 | 1.89 | |
| Supply Ramp | Supply voltage ramp | Requires monotonic ramp (10-90 % of VDD) | 0.1 | | 20 | ms |
| $T_A$ | Operating free-air temperature | | –40 | | 105 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 135 | °C |

### 6.4 Thermal Information

| THERMAL METRIC[1] | | LMK1D2106 | LMK1D2108 | UNIT |
|---|---|---|---|---|
| | | RHA (VQFN) | RGZ (VQFN) | |
| | | 40 PINS | 48 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 30.3 | 30.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 21.6 | 21.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.1 | 12.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | 0.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 13 | 12.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.5 | 4.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 6.5 Electrical Characteristics

VDD = 1.8 V ± 5 %, –40°C ≤T_A ≤ 105°C. Typical values are at VDD = 1.8 V, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| $IDD_{STAT}$ | Core supply current, static (LMK1D2106) | All outputs enabled and unterminated, f = 0 Hz, AMP_SEL = Open (default) | | 75 | | mA |
| $IDD_{STAT}$ | Core supply current, static (LMK1D2108) | All outputs enabled and unterminated, f = 0 Hz, AMP_SEL = Open (default) | | 80 | | mA |
| $IDD_{100M}$ | Core supply current (LMK1D2106) | All outputs enabled, RL = 100 Ω, f =100 MHz, AMP_SEL = Open (default) | | 113 | 140 | mA |
| $IDD_{100M}$ | Core supply current (LMK1D2108) | All outputs enabled, RL = 100 Ω, f =100 MHz, AMP_SEL = Open (default) | | 134 | 160 | mA |
| $IDD_{STAT}$ | Core supply current, static (LMK1D2106) | All outputs enabled and unterminated, f = 0 Hz, AMP_SEL = 1 | | 75 | | mA |
| $IDD_{STAT}$ | Core supply current, static (LMK1D2108) | All outputs enabled and unterminated, f = 0 Hz, AMP_SEL = 1 | | 80 | | mA |
| $IDD_{100M}$ | Core supply current (LMK1D2106) | All outputs enabled, RL = 100 Ω, f =100 MHz, AMP_SEL = 1 | | 130 | 165 | mA |
| $IDD_{100M}$ | Core supply current (LMK1D2108) | All outputs enabled, RL = 100 Ω, f =100 MHz, AMP_SEL = 1 | | | 185 | mA |
| **EN/AMP_SEL CONTROL INPUT CHARACTERISTICS (Applies to $V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)** | | | | | | |
| $Vd_{I3}$ | Tri-state input | Open | | 0.4 × $V_{CC}$ | | V |

VDD = 1.8 V ± 5 %, –40°C ≤T_A ≤ 105°C. Typical values are at VDD = 1.8 V, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | Minimum input voltage for a logical "1" state in table 1 | 0.7 × $V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input low voltage | Maximum input voltage for a logical "0" state in table 1 | –0.3 | | 0.3 × $V_{CC}$ | V |
| $I_{IH}$ | Input high current | $V_{DD}$ can be 1.8V, 2.5V, or 3.3V with $V_{IH}$ = $V_{DD}$ | | | 30 | µA |
| $I_{IL}$ | Input low current | $V_{DD}$ can be 1.8V, 2.5V, or 3.3V with $V_{IH}$ = $V_{DD}$ | –30 | | | µA |
| $R_{pull-up}$ | Input pullup resistor | | | 500 | | kΩ |
| $R_{pull-down}$ | Input pulldown resistor | | | 320 | | kΩ |
| **SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to $V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)** | | | | | | |
| $f_{IN}$ | Input frequency | Clock input | DC | | 250 | MHz |
| $V_{IN_S-E}$ | Single-ended Input Voltage Swing | Assumes a square wave input with two levels | 0.4 | | 3.465 | V |
| dVIN/dt | Input Slew Rate (20% to 80% of the amplitude) | | 0.05 | | | V/ns |
| $I_{IH}$ | Input high current | $V_{DD}$ = 3.465 V, $V_{IH}$ = 3.465 V | | | 60 | µA |
| $I_{IL}$ | Input low current | $V_{DD}$ = 3.465 V, $V_{IL}$ = 0 V | –30 | | | µA |
| $C_{IN_SE}$ | Input capacitance | at 25°C | | 3.5 | | pF |
| **DIFFERENTIAL CLOCK INPUT (Applies to $V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)** | | | | | | |
| $f_{IN}$ | Input frequency | Clock input | | | 2 | GHz |
| $V_{IN,DIFF(p-p)}$ | Differential input voltage peak-to-peak {2 × ($V_{INP}$ – $V_{INN}$)} | $V_{ICM}$ = 1 V ($V_{DD}$ = 1.8 V) | 0.3 | | 2.4 | $V_{PP}$ |
| | | $V_{ICM}$ = 1.25 V ($V_{DD}$ = 2.5 V/3.3 V) | 0.3 | | 2.4 | |
| $V_{ICM}$ | Input common-mode voltage | $V_{IN,DIFF(P-P)}$ > 0.4 V ($V_{DD}$ = 1.8 V/2.5 V/3.3 V) | 0.25 | | 2.3 | V |
| $I_{IH}$ | Input high current | $V_{DD}$ = 3.465 V, $V_{INP}$ = 2.4 V, $V_{INN}$ = 1.2 V | | | 30 | µA |
| $I_{IL}$ | Input low current | $V_{DD}$ = 3.465 V, $V_{INP}$ = 0 V, $V_{INN}$ = 1.2 V | –30 | | | µA |
| $C_{IN_SE}$ | Input capacitance (Single-ended) | at 25°C | | 3.5 | | pF |
| **LVDS DC OUTPUT CHARACTERISTICS** | | | | | | |
| \|VOD\| | Differential output voltage magnitude \|$V_{OUTP}$ - $V_{OUTN}$\| | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω | 250 | 350 | 450 | mV |
| \|VOD\| | Differential output voltage magnitude \|$V_{OUTP}$ - $V_{OUTN}$\| | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω, AMP_SEL = 1 | 400 | 500 | 650 | mV |
| ΔVOD | Change in differential output voltage magnitude | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω | –15 | | 15 | mV |
| ΔVOD | Change in differential output voltage magnitude | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω, AMP_SEL = 1 | –20 | | 20 | mV |
| $V_{OC(SS)}$ | Steady-state, common-mode output voltage | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω ($V_{DD}$ = 1.8 V) | 1 | | 1.2 | V |
| | | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω ($V_{DD}$ = 2.5 V/3.3 V) | 1.1 | | 1.375 | |
| $V_{OC(SS)}$ | Steady-state, common-mode output voltage | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω ($_{VDD}$ = 1.8 V), AMP_SEL = 1 | 0.8 | | 1.05 | V |
| | | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω ($_{VDD}$ = 2.5 V/3.3 V), AMP_SEL = 1 | 0.9 | | 1.15 | |
| $\Delta_{VOC(SS)}$ | Change in steady-state, common-mode output voltage | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω | –15 | | 15 | mV |
| $\Delta_{VOC(SS)}$ | Change in steady-state, common-mode output voltage | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω, AMP_SEL = 1 | –20 | | 20 | mV |


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VDD = 1.8 V ± 5 %, –40°C ≤T_A ≤ 105°C. Typical values are at VDD = 1.8 V, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVDS AC OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{ring}$ | Output overshoot and undershoot | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω, $f_{OUT}$ = 491.52 MHz | –0.1 | | 0.1 | $V_{OD}$ |
| $V_{OS}$ | Output AC common-mode voltage | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω | | 50 | 100 | $mV_{pp}$ |
| $V_{OS}$ | Output AC common-mode voltage | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω, AMP_SEL = 1 | | 75 | 150 | $mV_{pp}$ |
| $I_{OS}$ | Short-circuit output current (differential) | $V_{OUTP}$ = $V_{OUTN}$ | –12 | | 12 | mA |
| $I_{OS(cm)}$ | Short-circuit output current (common-mode) | $V_{OUTP}$ = $V_{OUTN}$ = 0 | –24 | | 24 | mA |
| $t_{PD}$ | Propagation delay | $V_{IN,DIFF(P-P)}$ = 0.3 V, $R_{LOAD}$ = 100 Ω (1) | 0.3 | | 0.575 | ns |
| $t_{SK, O}$ | Output skew | Skew between outputs with the same load conditions (12 and 16 channels) (2) | | | 20 | ps |
| $t_{SK, b}$ | Output bank skew | Skew between the outputs within the same bank (2106/2108) (3) | | | 17.5 | ps |
| $t_{SK, PP}$ | Part-to-part skew | Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading. | | | 200 | ps |
| $t_{SK, P}$ | Pulse skew | 50% duty cycle input, crossing point-to-crossing-point distortion (4) | –20 | | 20 | ps |
| $t_{RJIT(ADD)}$ | Random additive Jitter (rms) | $f_{IN}$ = 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns, Integration range = 12 kHz to 20 MHz, with output load $R_{LOAD}$ = 100 Ω | | 45 | 60 | fs, RMS |
| Phase noise | Phase Noise for a carrier frequency of 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns with output load $R_{LOAD}$ = 100 Ω | $PN_{1kHz}$ | | –143 | | dBc/Hz |
| | | $PN_{10kHz}$ | | –150 | | |
| | | $PN_{100kHz}$ | | –157 | | |
| | | $PN_{1MHz}$ | | –160 | | |
| | | $PN_{floor}$ | | –164 | | |
| SPUR | Spurious suppression between dual banks | $F_{IN0}$ = 491.52 MHz, $F_{IN1}$ = 61.44 MHz; Measured between neighboring outputs | | –60 | | dB |
| | | $F_{IN0}$ = 491.52 MHz, $F_{IN1}$ = 15.36 MHz; Measured between neighboring outputs | | –70 | | |
| ODC | Output duty cycle | With 50% duty cycle input | 45 | | 55 | % |
| $t_R/t_F$ | Output rise and fall time | 20% to 80% with $R_{LOAD}$ = 100 Ω | | | 300 | ps |
| $t_R/t_F$ | Output rise and fall time | 20% to 80% with RLOAD = 100 Ω (AMP_SEL= 1) | | | 300 | ps |
| $V_{AC_REF}$ | Reference output voltage | VDD = 2.5 V, $I_{LOAD}$ = 100 µA | 0.9 | 1.25 | 1.375 | V |
| **POWER SUPPLY NOISE REJECTION (PSNR) $V_{DD}$ = 2.5 V/ 3.3 V** | | | | | | |
| PSNR | Power Supply Noise Rejection ($f_{carrier}$ = 156.25 MHz) | 10 kHz, 100 mVpp ripple injected on $V_{DD}$ | | –70 | | dBc |
| | | 1 MHz, 100 mVpp ripple injected on $V_{DD}$ | | –50 | | |

(1) Measured between single-ended/differential input crossing point to the differential output crossing point.
(2) For the dual bank devices, the inputs are phase aligned and have 50% duty cycle.
(3) Applies to the dual bank family.

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(4) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.


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### 6.6 Typical Characteristics

Figure 6-1 (LMK1D2106) and Figure 6-3 (LMK1D2108) capture the variation of the current consumption with input frequency and supply voltage when AMP_SEL = 0. Figure 6-2 (LMK1D2106) and Figure 6-4 (LMK1D2108) show the current consumption variation when AMP_SEL = 1. Figure 6-5 and Figure 6-6 portray the variation of the differential output voltage (VOD) swept across frequency.

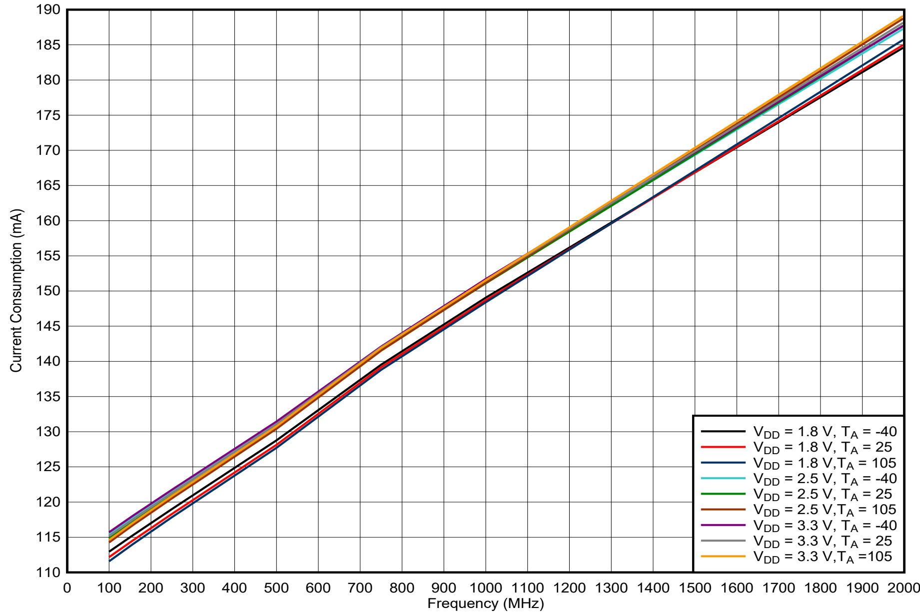


**Figure 6-1. LMK1D2106 Current Consumption vs. Frequency, AMP_SEL = 0**

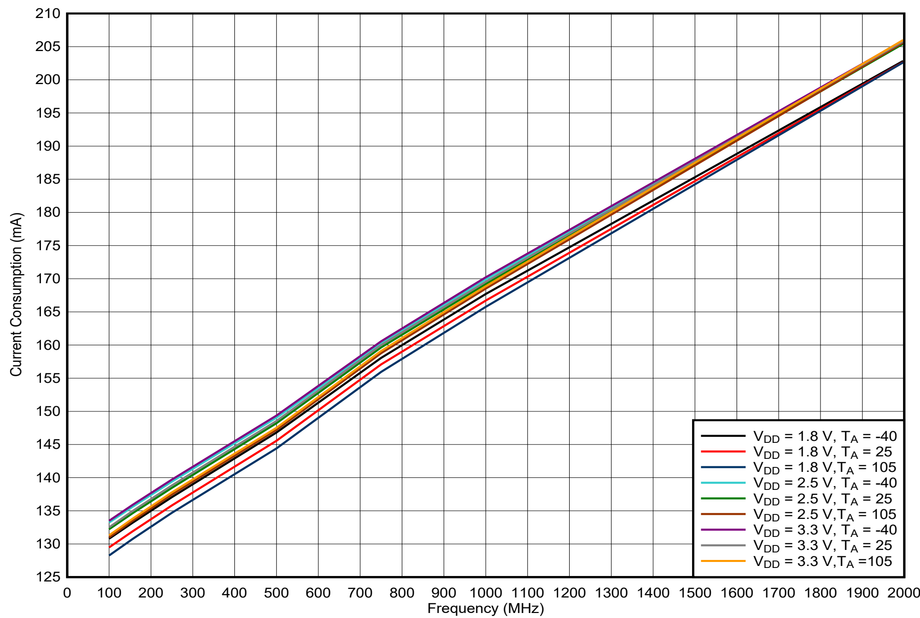


**Figure 6-2. LMK1D2106 Current Consumption vs. Frequency, AMP_SEL = 1**

## 6.6 Typical Characteristics

Figure 6-1 (LMK1D2106) and Figure 6-3 (LMK1D2108) capture the variation of the current consumption with input frequency and supply voltage when AMP_SEL = 0. Figure 6-2 (LMK1D2106) and Figure 6-4 (LMK1D2108) show the current consumption variation when AMP_SEL = 1. Figure 6-5 and Figure 6-6 portray the variation of the differential output voltage (VOD) swept across frequency.

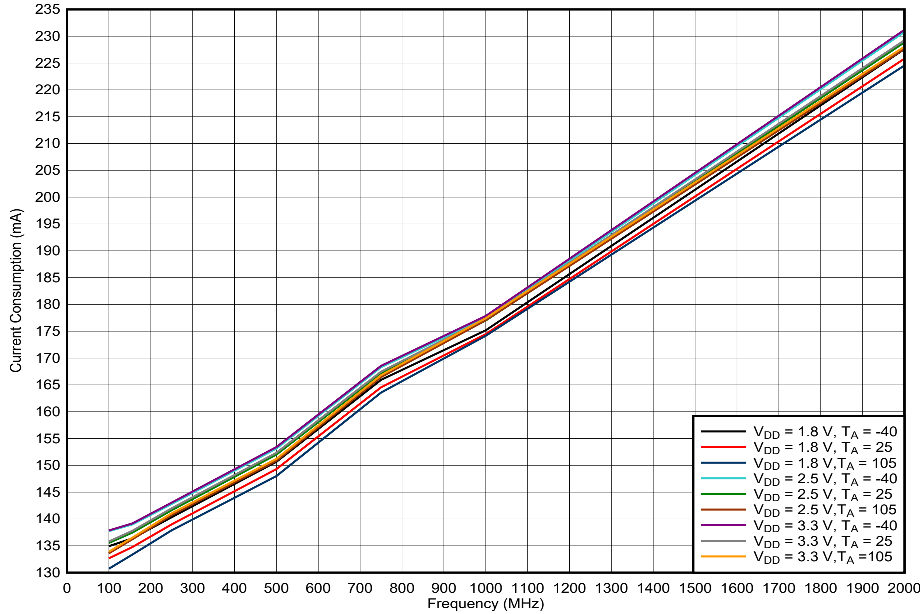


**Figure 6-3. LMK1D2108 Current Consumption vs. Frequency, AMP_SEL = 0**

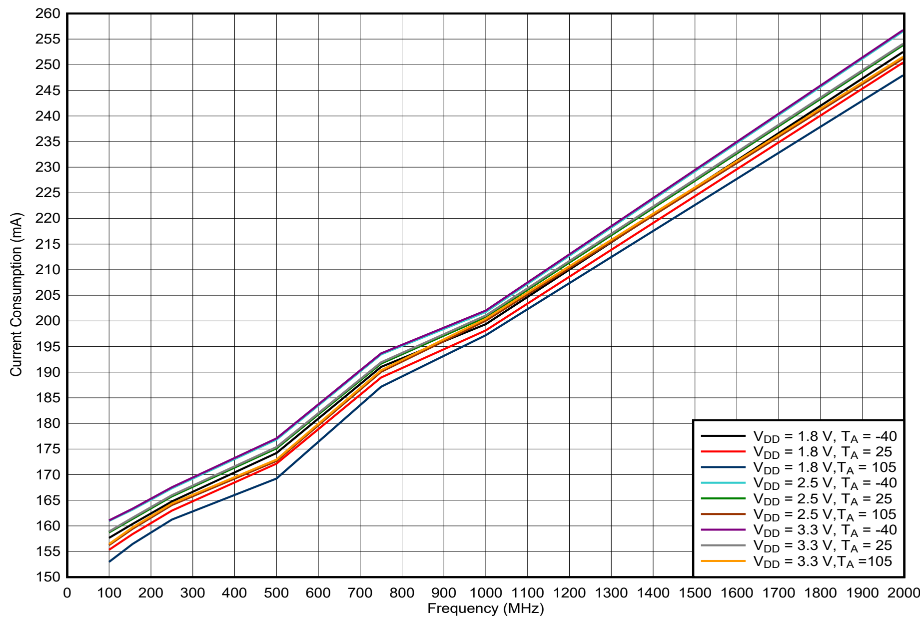


**Figure 6-4. LMK1D2108 Current Consumption vs. Frequency, AMP_SEL = 1**


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## 6.6 Typical Characteristics

Figure 6-1 (LMK1D2106) and Figure 6-3 (LMK1D2108) capture the variation of the current consumption with input frequency and supply voltage when AMP_SEL = 0. Figure 6-2 (LMK1D2106) and Figure 6-4 (LMK1D2108) show the current consumption variation when AMP_SEL = 1. Figure 6-5 and Figure 6-6 portray the variation of the differential output voltage (VOD) swept across frequency.

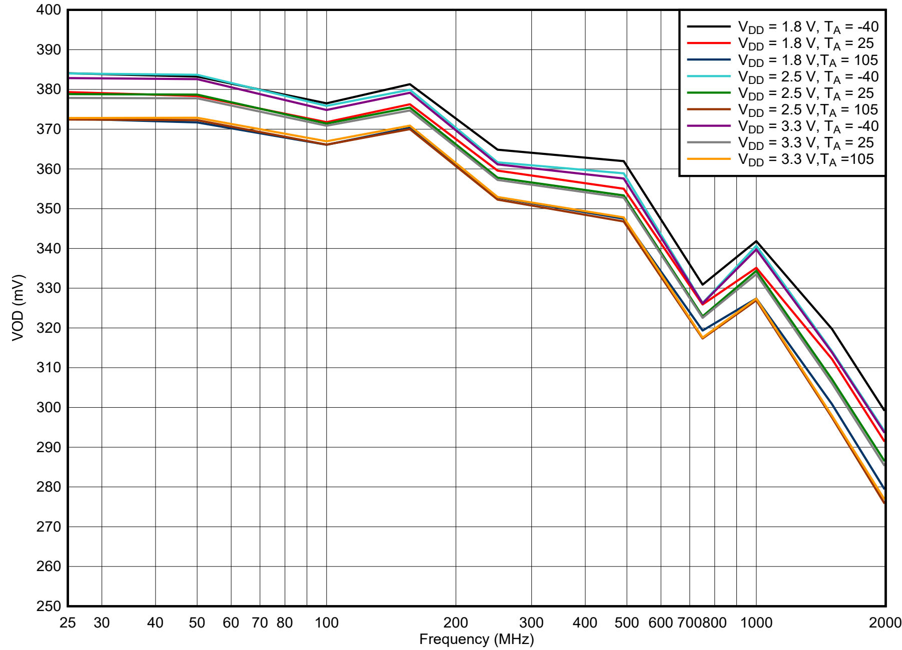


**Figure 6-5. LMK1D210x VOD vs. Frequency, AMP_SEL = 0**

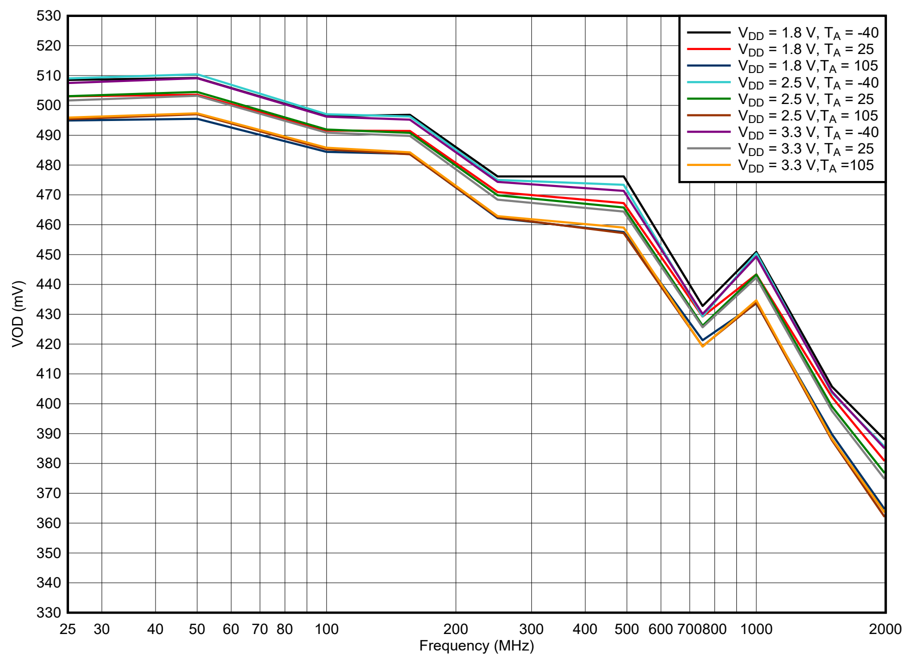


**Figure 6-6. LMK1D210x VOD vs. Frequency, AMP_SEL = 1**

# 7 Parameter Measurement Information

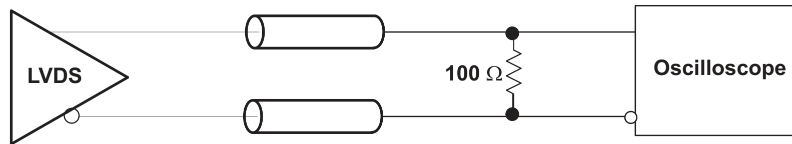


**Figure 7-1. LVDS Output DC Configuration During Device Test**

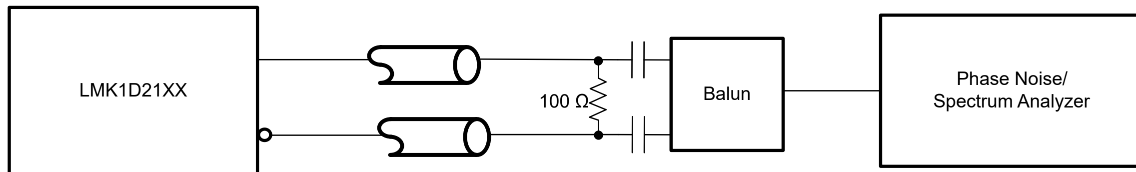


**Figure 7-2. LVDS Output AC Configuration During Device Test**

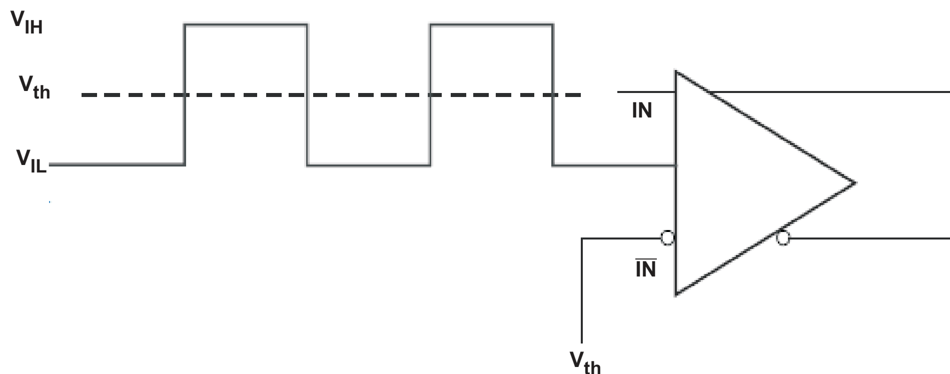


**Figure 7-3. DC-Coupled LVCMOS Input During Device Test**

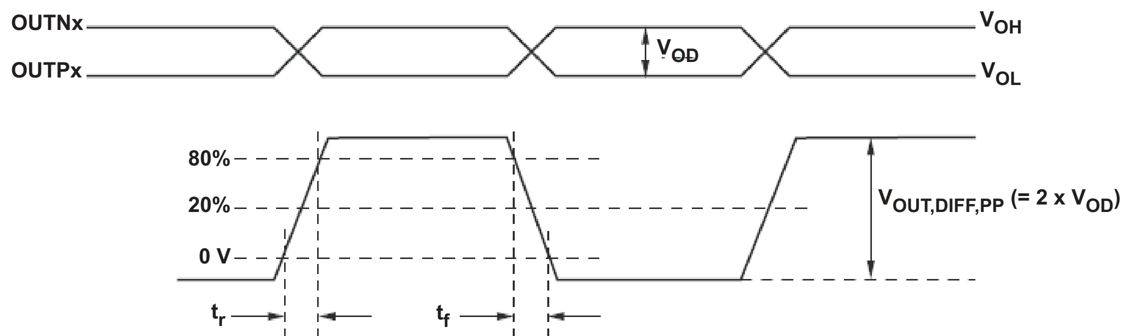


**Figure 7-4. Output Voltage and Rise/Fall Time**


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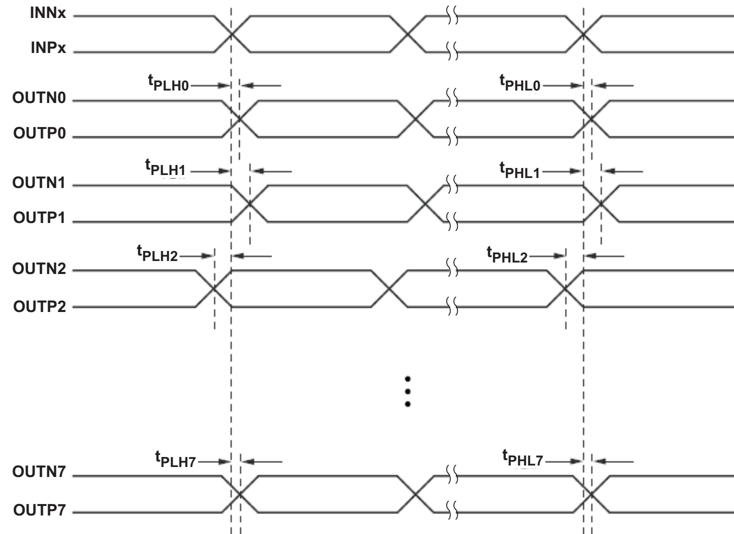


A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest $t_{PLHn}$ or the difference between the fastest and the slowest $t_{PHLn}$ (n = 0, 1, 2, ..7)

B. Part-to-part skew is calculated as the greater of the following: the difference between the fastest and the slowest $t_{PLHn}$ or the difference between the fastest and the slowest $t_{PHLn}$ across multiple devices (n = 0, 1, 2, ..7)

**Figure 7-5. Output Skew and Part-to-Part Skew**

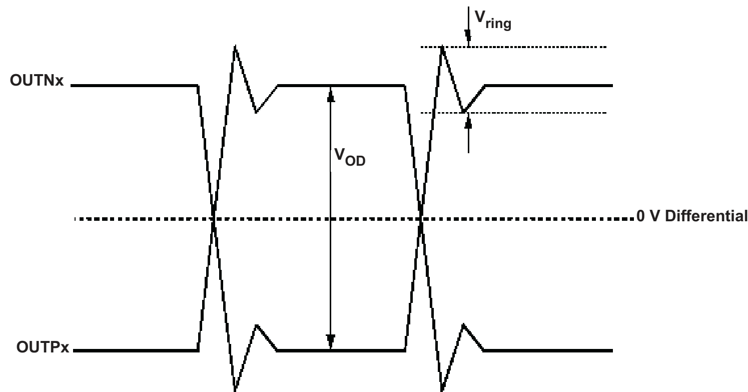


**Figure 7-6. Output Overshoot and Undershoot**

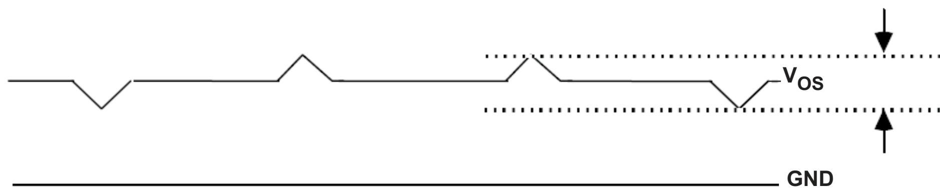


**Figure 7-7. Output AC Common Mode**

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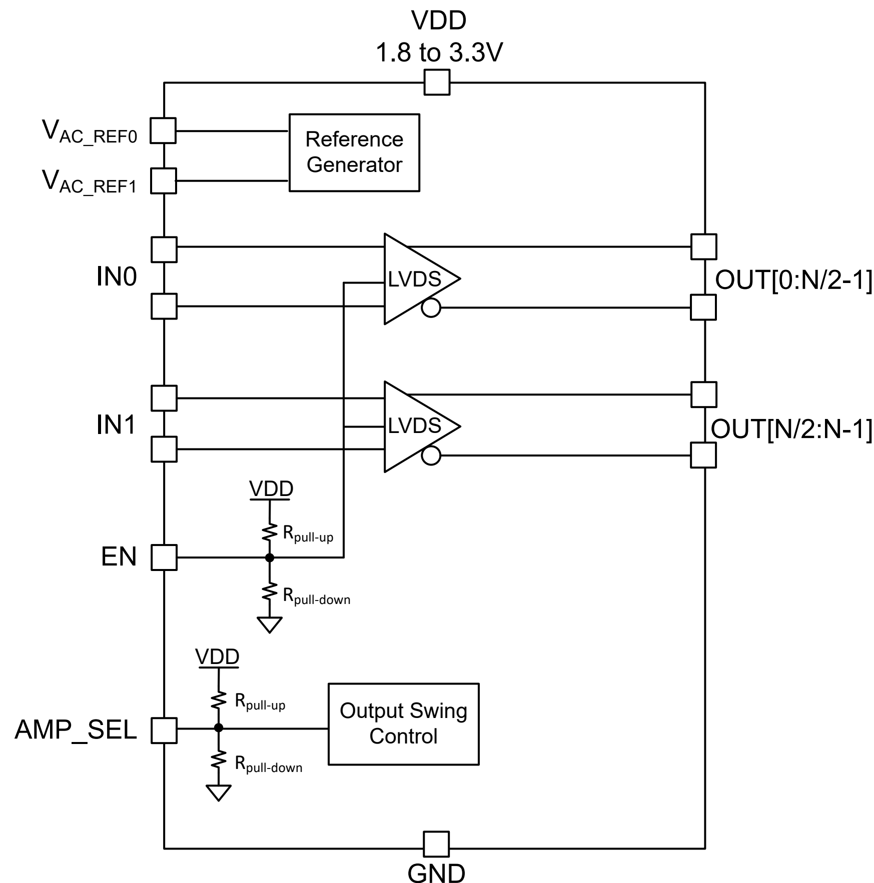
# 8 Detailed Description

## 8.1 Overview

The LMK1D210x LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D210x, AC coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

## 8.2 Functional Block Diagram





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## 8.3 Feature Description

The LMK1D210x is a low additive jitter LVDS fan-out buffer that can generate up to 6 (LMK1D2106) or 8 (LMK1D2108) LVDS copies of a single input that is either LVDS, LVPECL, HCSL, CML, or LVCMOS on each of its banks. The device has two banks, therefore this translates to a total of 12 (LMK1D2106) or 16 (LMK1D2108) pairs of outputs. Refer to the Table 8-1 for output bank mapping. The reference clock frequencies can go up to 2 GHz.

**Table 8-1. Output Bank**

| Bank | LMK1D2106 | LMK1D2108 |
|---|---|---|
| 0 | OUT0 to OUT5 | OUT0 to OUT7 |
| 1 | OUT6 to OUT11 | OUT8 to OUT15 |

Apart from providing a very low additive jitter and low output skew, the LMK1D210x has an output bank enable/disable control pin (EN) and an output amplitude control pin (AMP_SEL).

### 8.3.1 Fail-Safe Input

The LMK1D210x family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to the *Absolute Maximum Ratings* for more information on the maximum input supported by the device. The device also incorporates an input hysteresis, which prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

## 8.4 Device Functional Modes

The output banks of the LMK1D210x can be selected through the control pin (see Table 8-2). Unused inputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the LMK1D210x to provide greater system flexibility.

**Table 8-2. Output Control**

| EN | CLOCK OUTPUTS |
|---|---|
| 0 | All bank outputs disabled (static logic "0") |
| 1 | Bank 0 outputs enabled and Bank 1 outputs disabled |
| OPEN | All bank outputs enabled |

The output amplitude of the banks of the LMK1D210x can be selected through the amplitude selection pin (see Table 8-3). The higher output amplitude mode (boosted swing LVDS mode) can be used in applications which require higher amplitude either for better noise performance (higher slew rate) or if the receiver has swing requirements which the standard LVDS swing cannot meet.

**Table 8-3. Amplitude Selection**

| AMP_SEL | OUTPUT AMPLITUDE (mV) |
|---|---|
| 0 | Bank 0: boosted LVDS swing (500 mV)<br>Bank 1: standard LVDS swing (350 mV) |
| OPEN | Bank 0: standard LVDS swing (350 mV)<br>Bank 1: standard LVDS swing (350 mV) |
| 1 | Bank 0: boosted LVDS swing (500 mV)<br>Bank 1: boosted LVDS swing (500 mV) |

### 8.4.1 LVDS Output Termination

TI recommends unused outputs to be terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode $V_{OS}$) in the outputs being used.

The LMK1D210x can be connected to LVDS receiver inputs with DC and AC coupling as shown in Figure 8-1 and Figure 8-2, respectively.

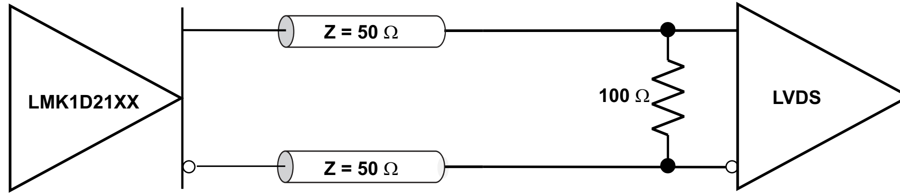


**Figure 8-1. Output DC Termination**

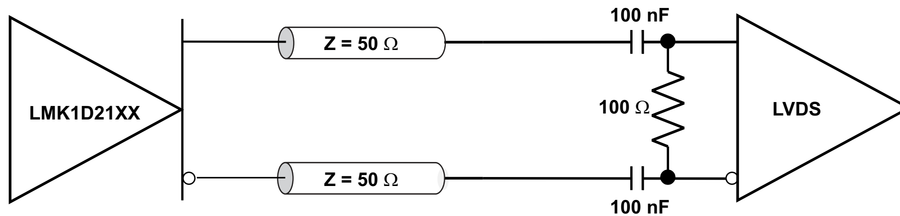


**Figure 8-2. Output AC Termination (With the Receiver Internally Biased)**

### 8.4.2 Input Termination

The LMK1D210x inputs can be interfaced with LVDS, LVPECL, HCSL, or LVCMOS drivers.

LVDS drivers can be connected to LMK1D210x inputs with DC and AC coupling as shown Figure 8-3 and Figure 8-4, respectively.

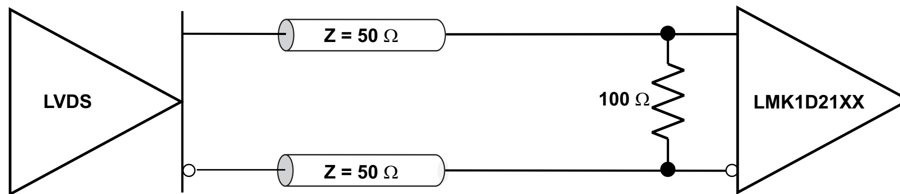


**Figure 8-3. LVDS Clock Driver Connected to LMK1D210x Input (DC-Coupled)**

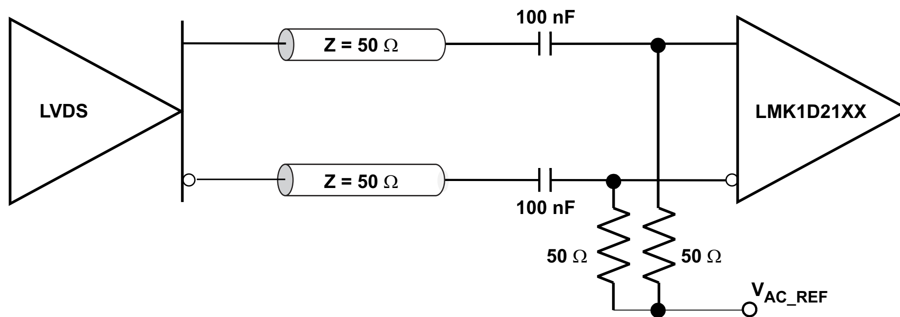


**Figure 8-4. LVDS Clock Driver Connected to LMK1D210x Input (AC-Coupled)**

Figure 8-5 shows how to connect LVPECL inputs to the LMK1D210x. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 $V_{PP}$.


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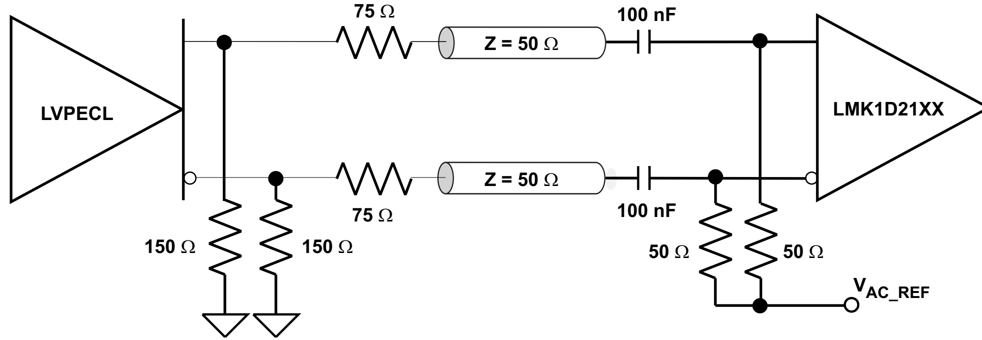


**Figure 8-5. LVPECL Clock Driver Connected to LMK1D210x Input**

Figure 8-6 shows how to couple a LVCMOS clock input to the LMK1D210x directly.

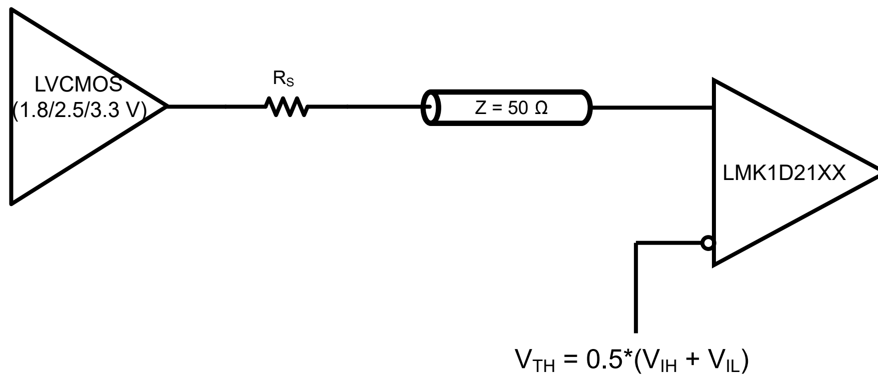


**Figure 8-6. 1.8-V, 2.5-V, or 3.3-V LVCMOS Clock Driver Connected to LMK1D210x Input**

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The LMK1D210x is a low additive jitter universal to LVDS fan-out buffer with dual inputs which fan-out to dual outputs banks. Each input can fan-out to six outputs in case of LMK1D2106 and eight outputs in case of LMK1D2108. The small package size, 1.8-V power supply operation, low output skew, and low additive jitter is desgined for applications that require high-performance clock distribution as well as for low-power and space-constraint applications.

## 9.2 Typical Application

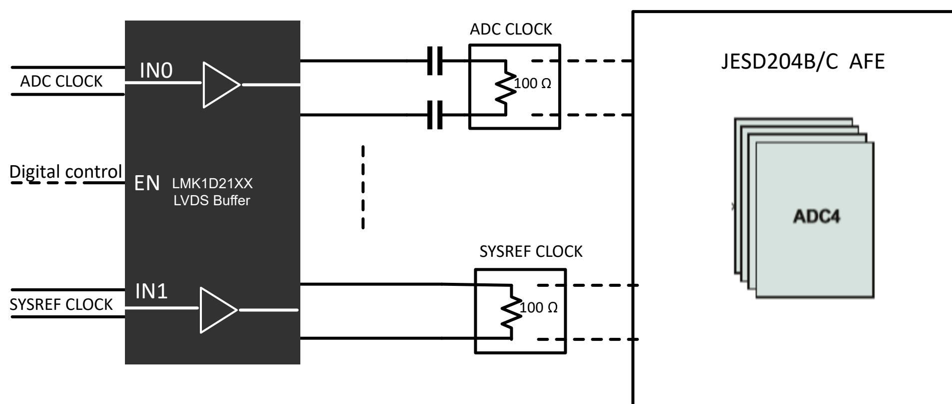


**Figure 9-1. Fan-Out Buffer for ADC Device Clock and SYSREF Distribution**

### 9.2.1 Design Requirements

The LMK1D210x shown in Figure 9-1 is configured to fan-out an ADC clock on the first output bank and SYSREF clock on the second output bank for a system using the JESD204B/C ADC. The low output-to-output skew, very low additive jitter and superior spurious suppression between dual banks makes the LMK1D210x a simple, robust and low-cost solution for distributing various clocks to JESD204B/C AFE systems. The configuration example can drive up to 4 ADC clocks and 4 SYSREF clocks for a JESD204B/C receiver with the following properties:

- The ADC clock receiver module is typically AC-coupled with an LVDS driver such as the LMK1D210x due to differences in common-mode voltage between the driver and receiver. Depending on the receiver, there maybe an option for internal 100-Ω differential termination in which case an external termination would not be required for the LMK1D210x.
- The SYSREF clock receiver module is typically DC-coupled provided the common-mode voltage of the LMK1D210x outputs match with the receiver. An external termination may not be needed in case of an internal termination in the receiver.
- Unused outputs of the LMK1D210x device are terminated differentially with a 100-Ω resistor for optimum performance.


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### 9.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

TI recommends unused outputs to be terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode $V_{OS}$) in the outputs being used.

In this application example, the ADC clock and SYSREF clocks require different output interfacing schemes. Power-supply filtering and bypassing is critical for low-noise applications.

In case of common-mode mismatch between the output voltage of the LMK1D210x and the receiver, one can use AC coupling to get around this. It might not be possible in certain applications, however, to AC-couple the LMK1D210x outputs to the receiver due to the settling time associated with this AC-coupling network (High-pass filter), which can result in non-deterministic behavior during the initial transients. For such applications, DC-coupling the outputs is necessary and thus requires a scheme which can overcome the inherent mismatch between the common-mode voltage of the driver and receiver.

The application report *Interfacing LVDS Driver With a Sub-LVDS Receiver* discusses how to interface between a LVDS driver and sub-LVDS receiver. The same concept can be applied to interface the LMK1D210x outputs to a receiver which has a lower common-mode voltage.

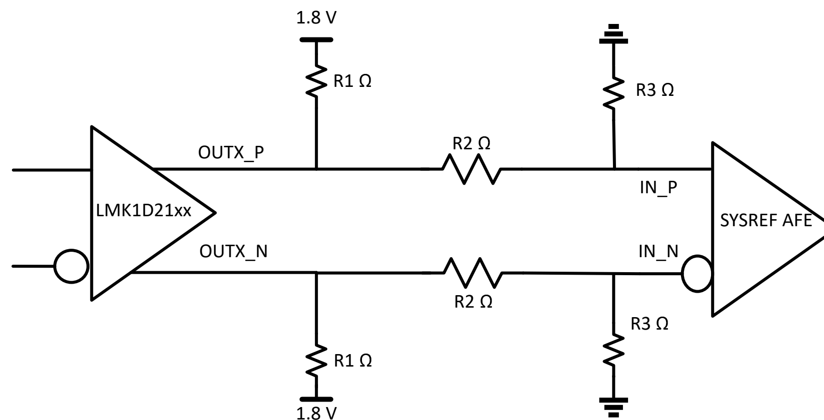
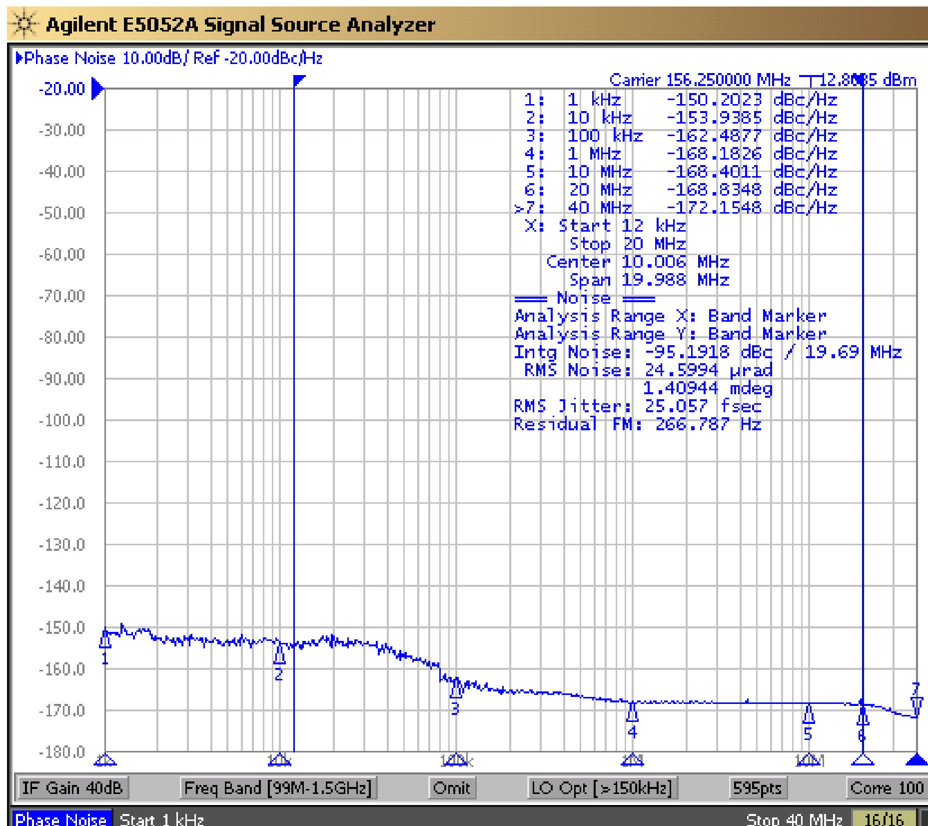



**Figure 9-2. Schematic for DC-Coupling LMK1D21xx With Lower Common-Mode Receiver**

Figure 9-2 shows the resistor divider network for stepping down the common-mode voltage as explained in the above application report. The resistors R1, R2 and R3 are chosen according to the input common-mode voltage requirements of the receiver. As highlighted before, make sure that the reduced swing is able to meet the requirements of the receiver. Higher swing mode (boosted LVDS swing mode) can be selected using the AMP_SEL pin highlighted in Table 8-3 to compensate for the reduced swing as the result of the resistor voltage divider.

### 9.2.3 Application Curves

The low additive noise of the LMK1D2108. The low noise 156.25-MHz source with 25-fs RMS jitter, shown in Figure 9-3, drives the LMK1D2108, resulting in 46.9-fs RMS when integrated from 12 kHz to 20 MHz (Figure 9-4). The resultant additive jitter is a low 39.7-fs RMS for this configuration. Note that this result applies to the LMK1D2106 device as well.




Note: Reference signal is a low-noise Rhode and Schwarz SMA100B

**Figure 9-3. LMK1D2108 Reference Phase Noise, 156.25 MHz, 25-fs RMS (12 kHz to 20 MHz)**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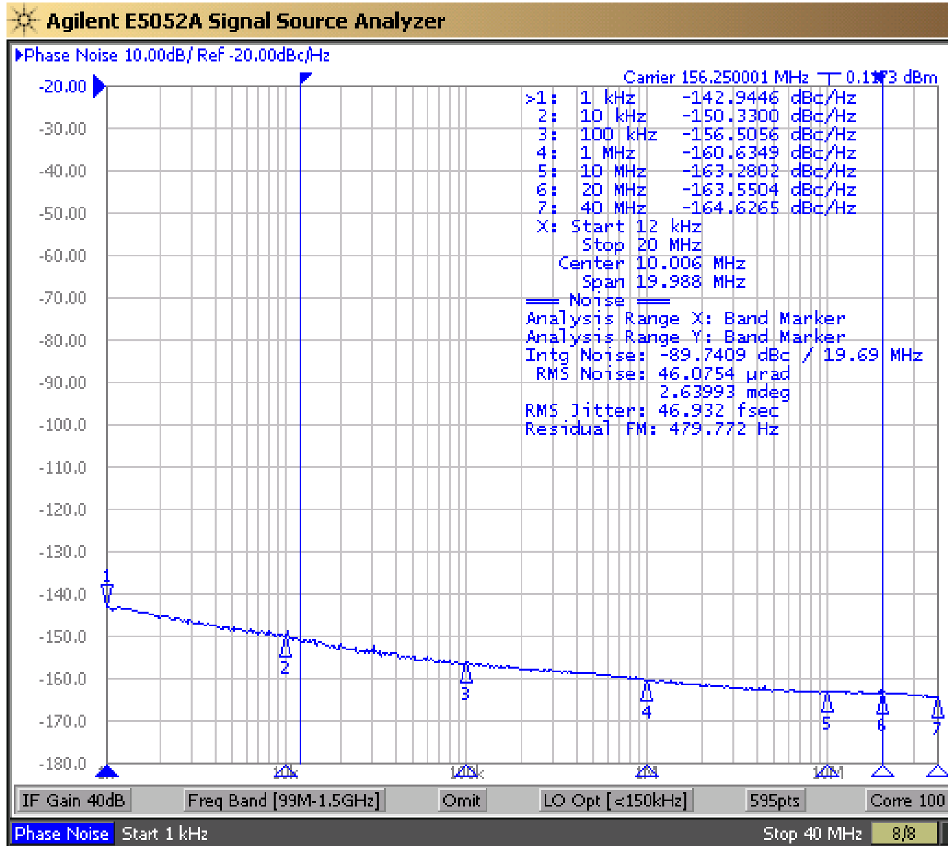


**Figure 9-4. LMK1D2108 Output Phase Noise, 156.25 MHz, 46.9-fs RMS (12 kHz to 20 MHz)**

## 10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-μF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver. These ferrite beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 10-1 shows this recommended power-supply decoupling method.

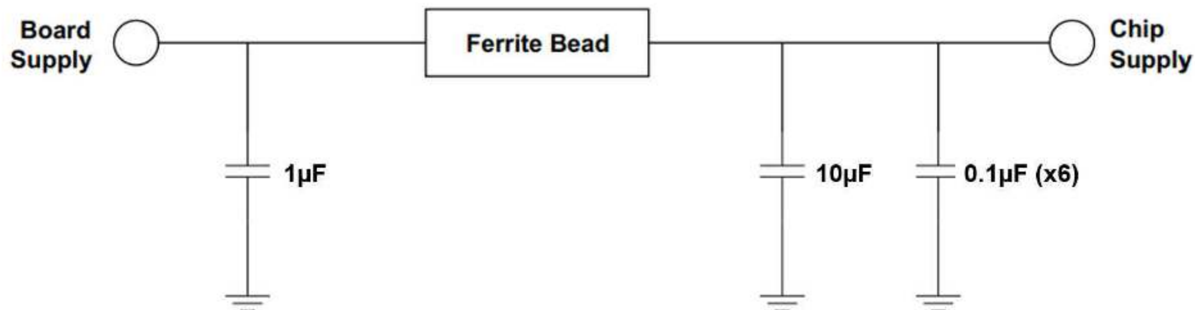


**Figure 10-1. Power Supply Decoupling**


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# 11 Layout

## 11.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Figure 11-1 and Figure 11-2 show the recommended top layer and via patterns for the 40-pin package (LMK1D2106).

## 11.2 Layout Examples

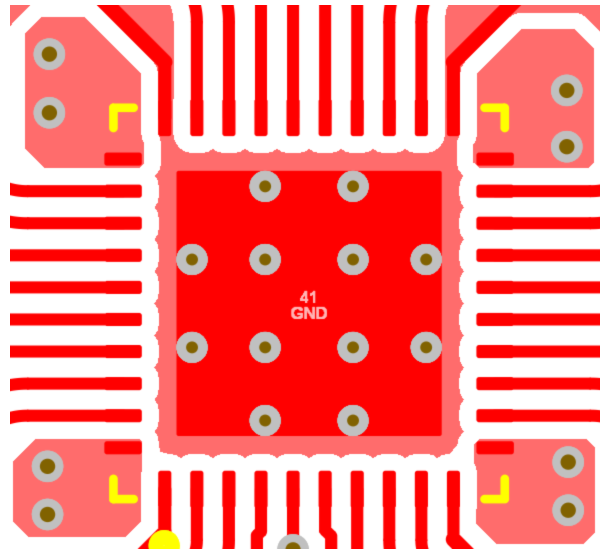


**Figure 11-1. PCB layout example for LMK1D2106, Top Layer**

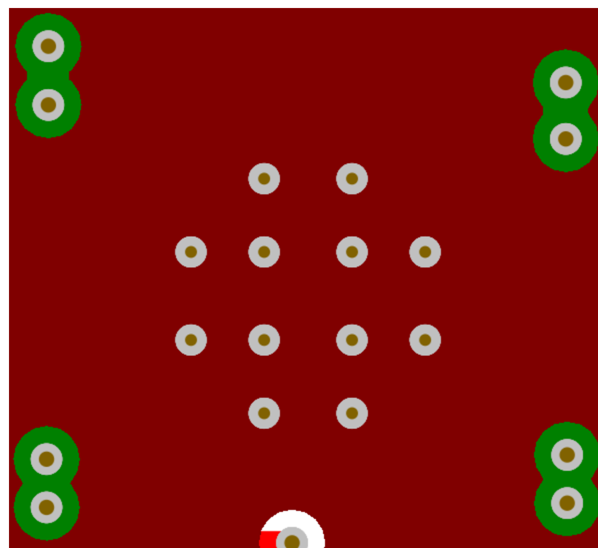

**Figure 11-2. PCB Layout Example for LMK1D2106, GND layer**

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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* user's guide
- Texas Instruments, *Power Consumption of LVPECL and LVDS* Analog design journal
- Texas Instruments, *Using Thermal Calculation Tools for Analog Components* application report

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 12.4 Trademarks

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## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMK1D2106RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2106 | Samples |
| LMK1D2106RHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2106 | Samples |
| LMK1D2108RGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | LMK1D 2108 | Samples |
| LMK1D2108RGZT | ACTIVE | VQFN | RGZ | 48 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | LMK1D 2108 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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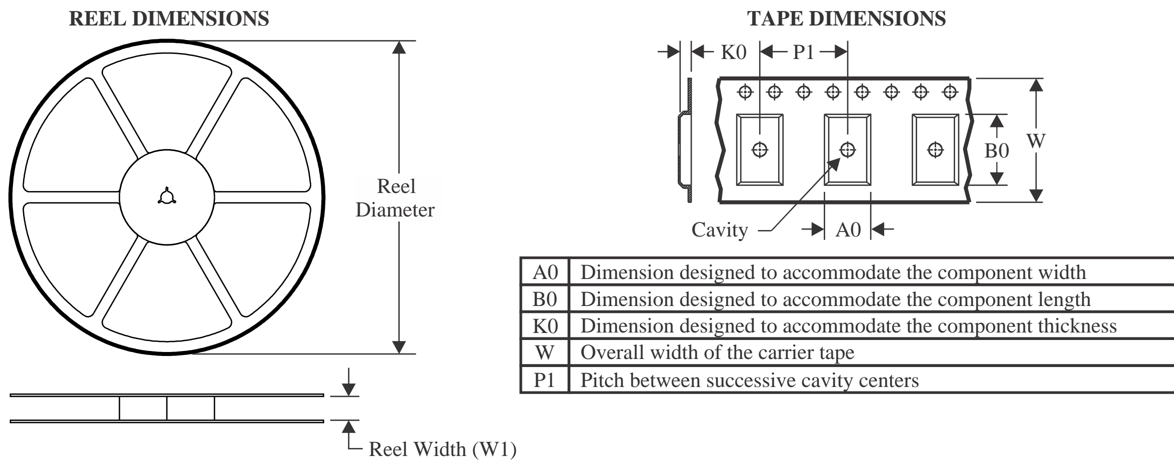
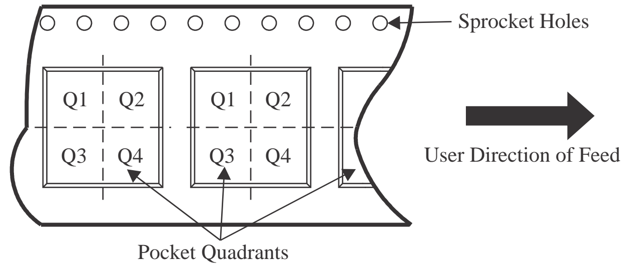
## TAPE AND REEL INFORMATION

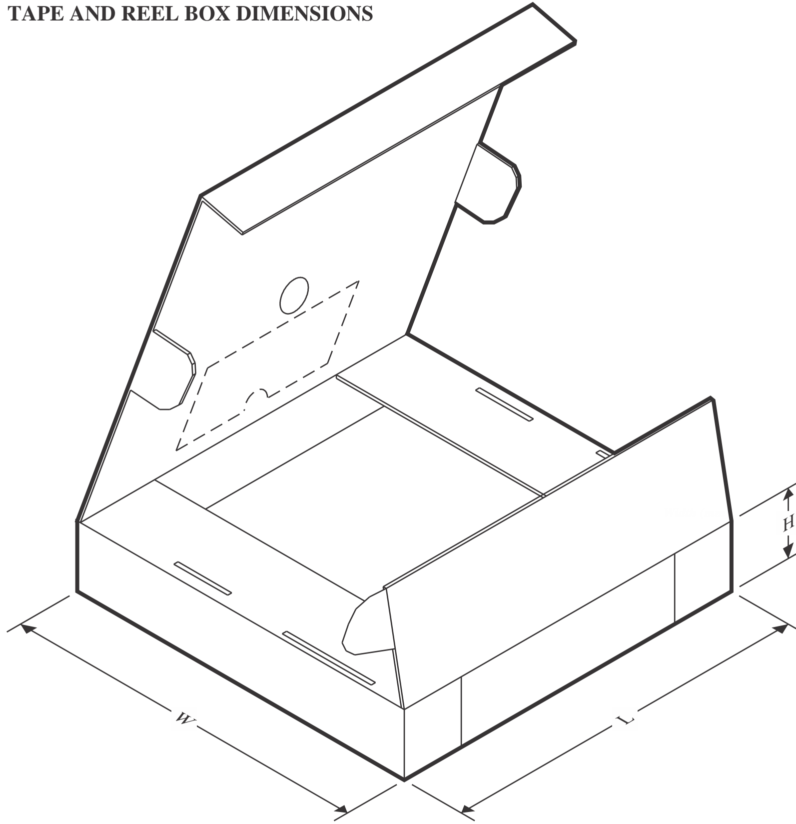



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMK1D2106RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| LMK1D2106RHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| LMK1D2108RGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| LMK1D2108RGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |

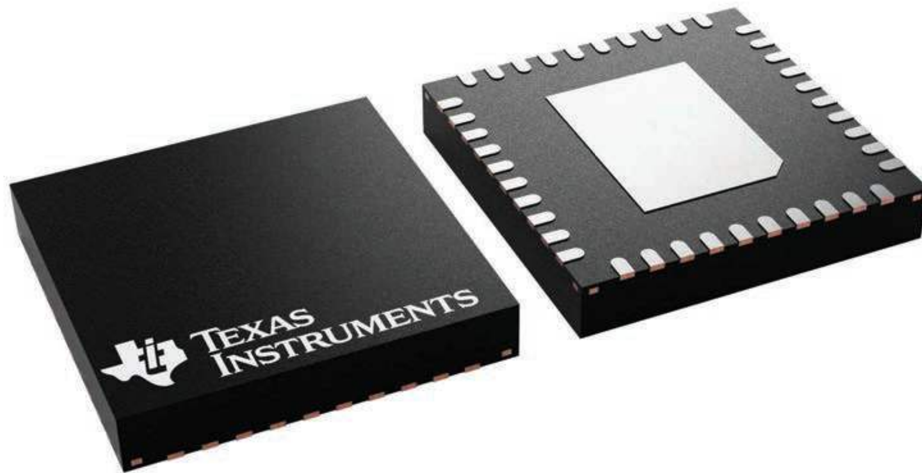
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

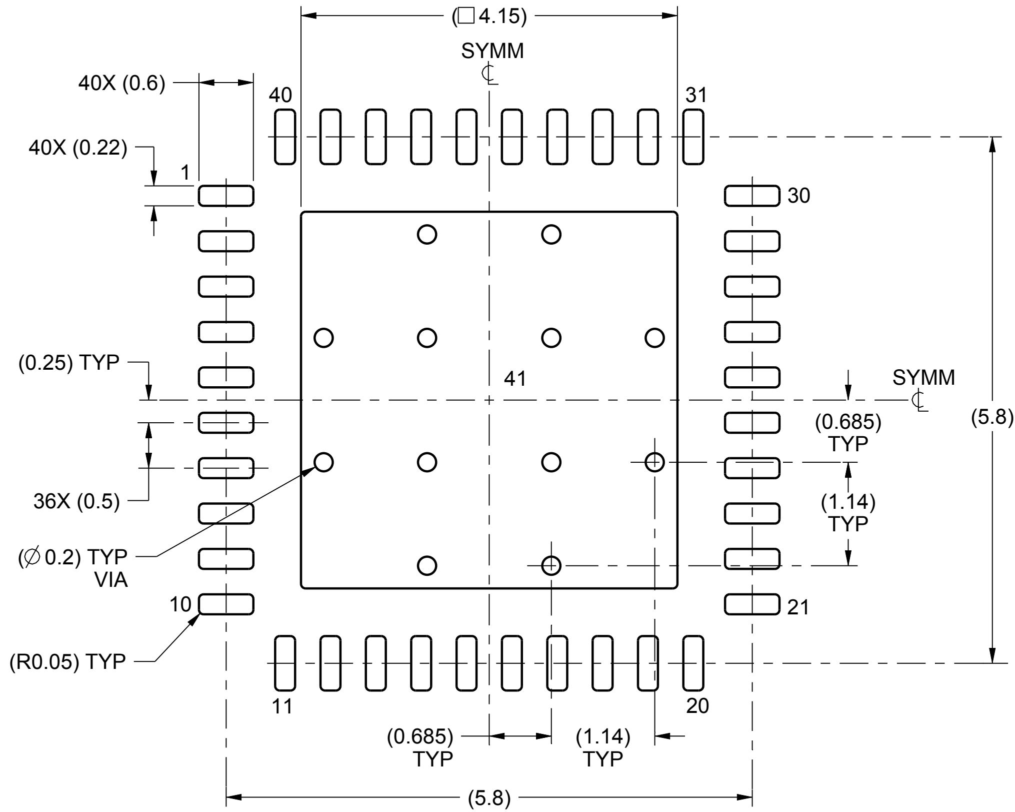
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMK1D2106RHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK1D2106RHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| LMK1D2108RGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK1D2108RGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

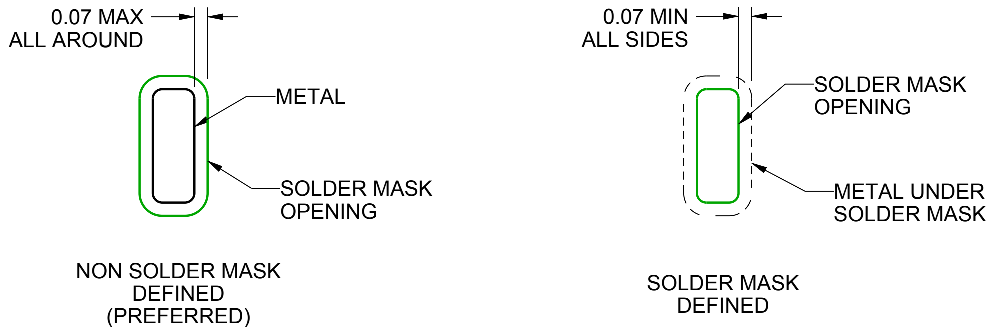


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:12X




NON SOLDER MASK
DEFINED
(PREFERRED)

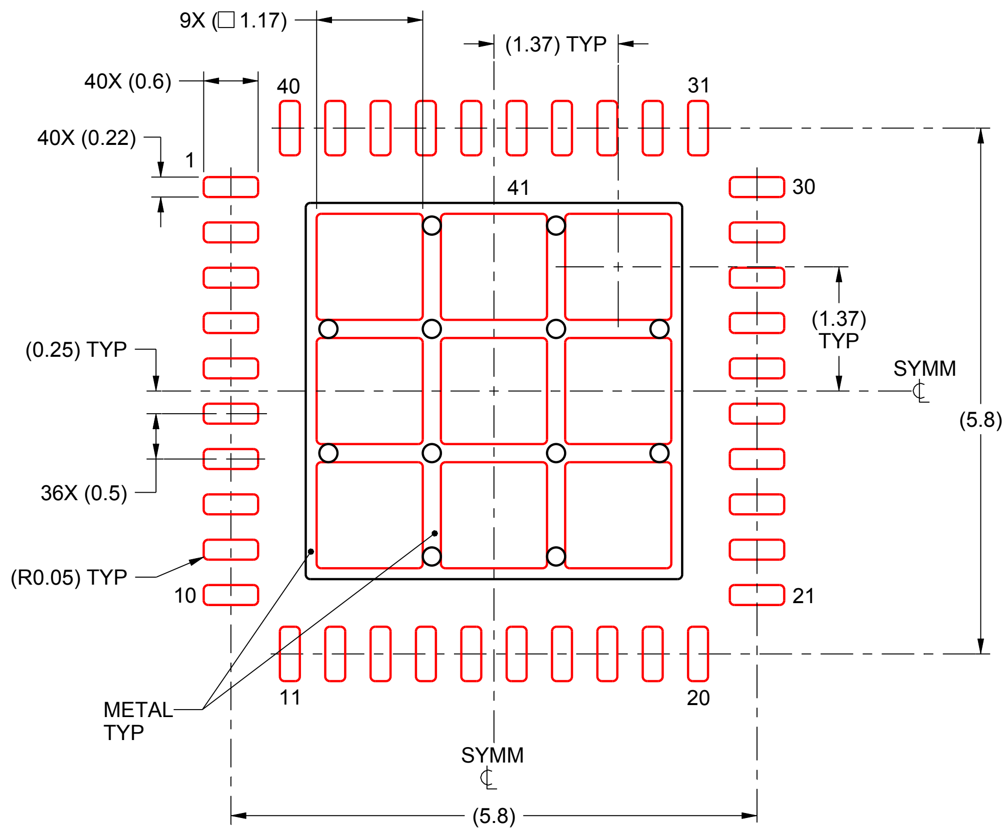
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



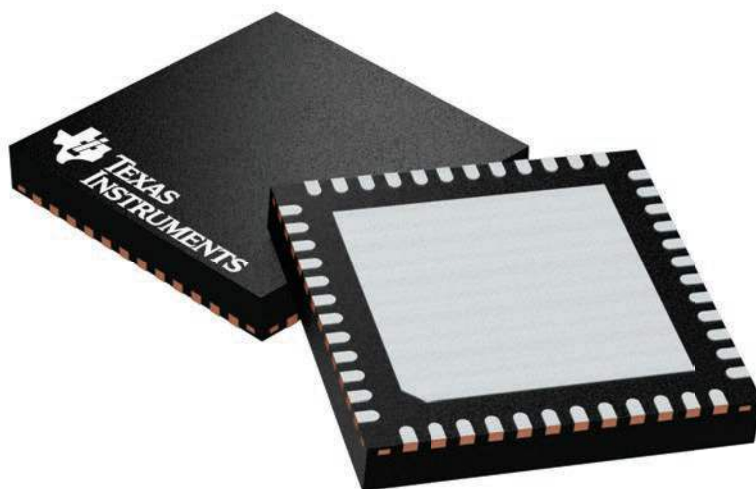

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

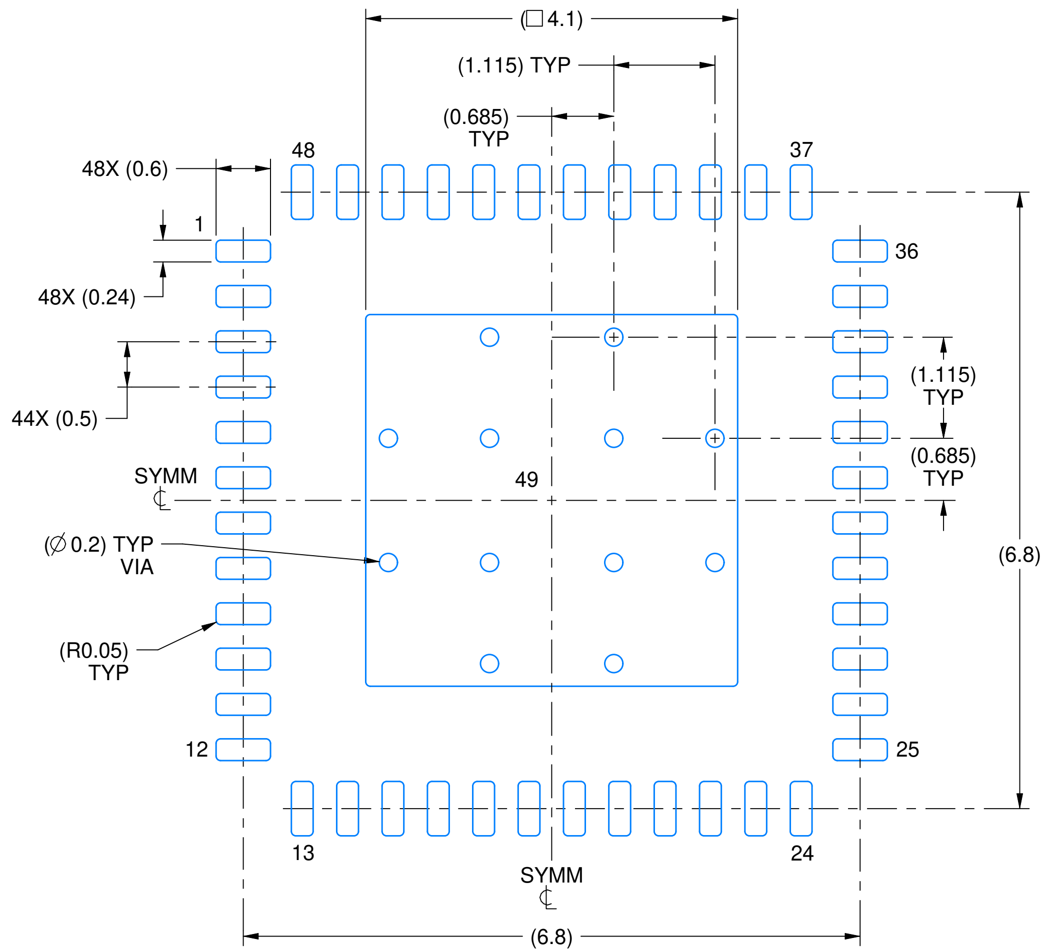



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

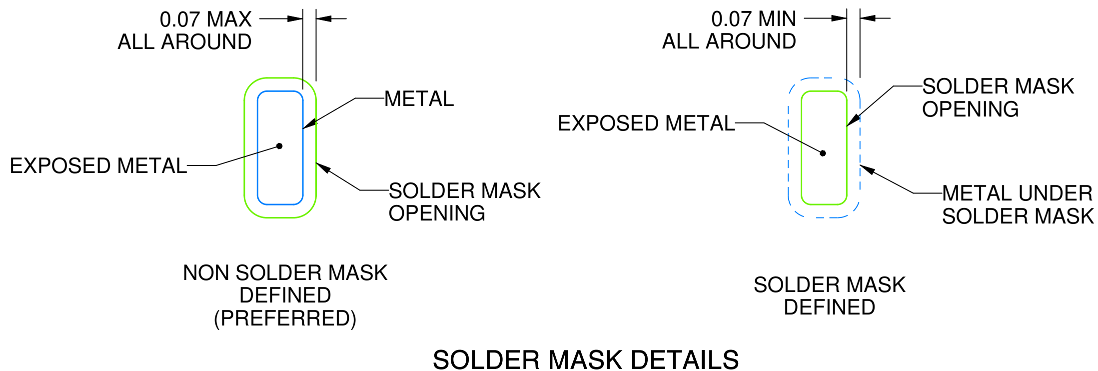
4224671/A

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

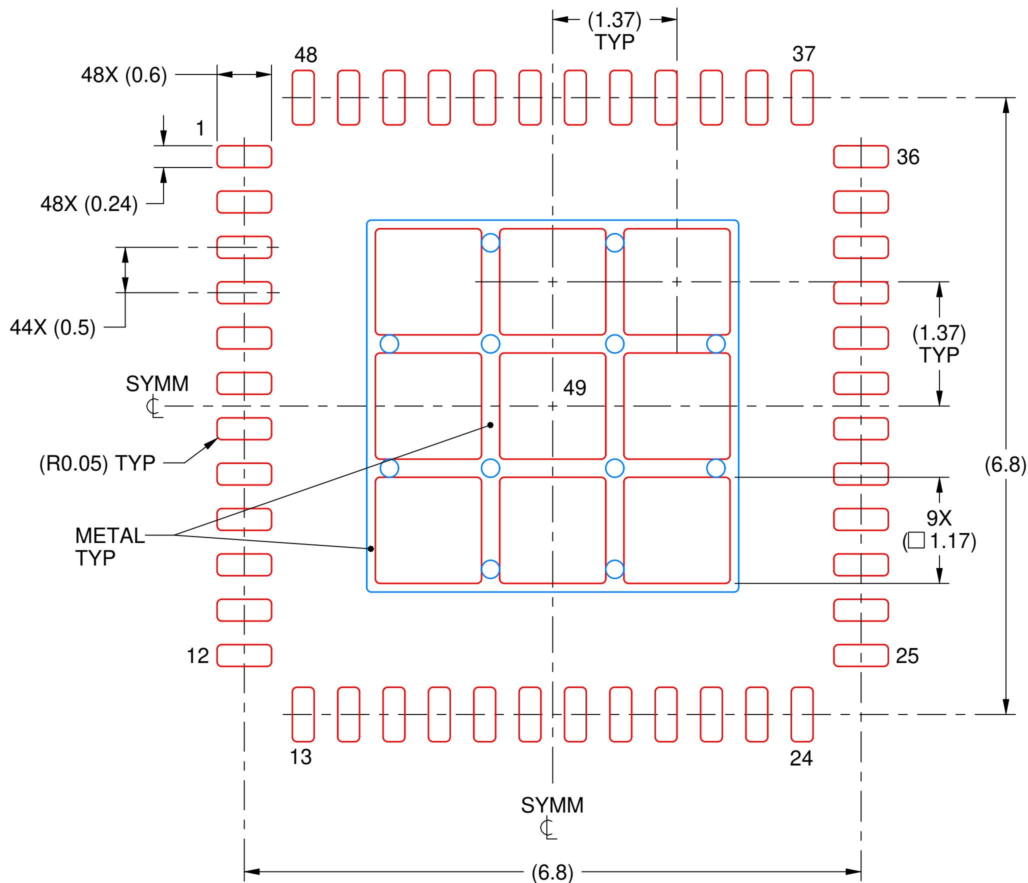



SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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