MSC8154/MSC8154E Application Development System

For 3G-LTE, TDD-LTE, WiMAX, 3GPP-HSPA and TD-SDCMA Using MSC8154 DSPs

Overview

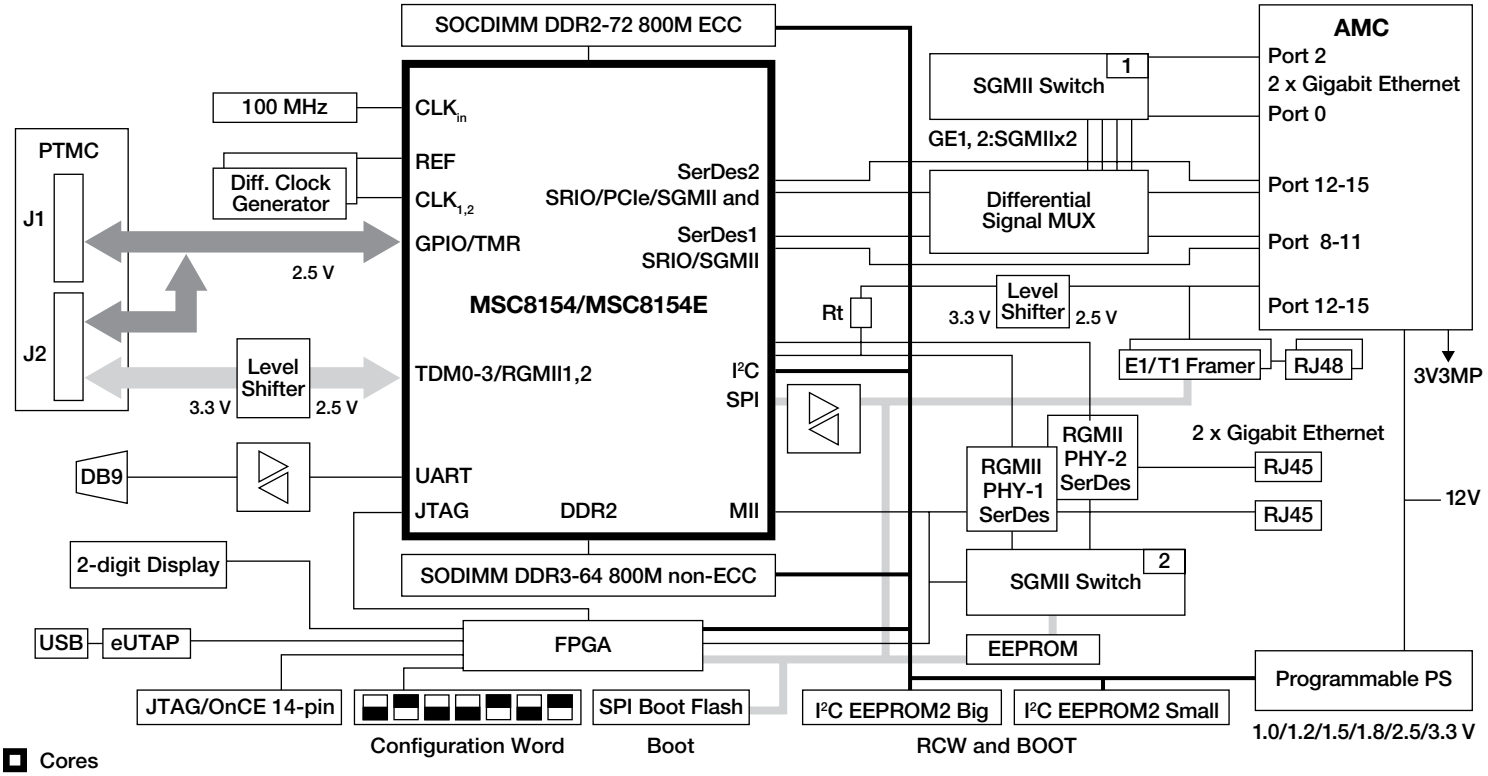
The MSC8154/MSC8154E application development system (MSC8154ADS) is a complete debugging environment intended for engineers developing applications for the MSC8154/MSC8154E Freescale digital signal processor (DSP). The MSC8154 and the MSC8154E devices are highly integrated DSP processors that contain four StarCore® SC3850 DSP subsystems (48 GMACS at 1 GHz). These devices target high-bandwidth, highly computational DSP applications and are optimized for 3GPP, TD-SCDMA, 3G-LTE and WiMAX applications. The MSC8154ADS is intended to serve as a platform for software and hardware development in the MSC8154/MSC8154E processor environment. On-board resources and the associated debugger enable developers to perform a variety of tasks, including:

- Download and run code
- Set breakpoints
- Display memory and registers
- Connect proprietary hardware via an expansion connector

The MSC8154ADS supports two working configurations:

- Stand-Alone Mode. The MSC8154ADS can run in a stand-alone mode like other application development systems, with direct connections to debuggers, power supply and other external connections.
- AMC Mode. The MSC8154ADS is inserted in a standard MicroTCA® backplane that allows testing of the high-speed Serial RapidIO® and PCI Express® ports against other platforms. By using a proprietary B2B adaptor card, the AMC-X-Over, the MSC8154 can work with a second MSC8154 device on an additional ADS board. The AMC edge connector carries all interface signals at high speed between the devices. The ADS is compatible with standard MicroTCA chassis, such as a Schroff® or TUNDRA® development platform.

MSC8154/MSC8154E Application Development System



Features

- Supports the MSC8154 1 GHz with core voltages of 1V
- The first DDR controller (DDRC1) is configured in DDR2 mode: 200-pin SOCDIMM with ECC support, 64-bit @ 800 Mbps, 1 GB of memory
- The second DDR controller (DDRC2) is configured in DDR3 mode: 204-pin SODIMM, 64-bit @ 800 Mbps, No-ECC, 1 GB of memory
- The MSC8154 RGMII (at ports GE1 and GE2) connects to two single Marvell® 88E1111 GETH PHYs for regular board configuration
- A Marvell 10-port SGMII switch 88E6182 links the MSC8154 SGMII lines to 2xRJ-45 copper connectors and to the 1000Base-X over AMC MicroTCA connector ports 0 and 2
- Pericom® PI2DBS212ZHE Diff Signal Switch parts support programmable SerDes lines multiplexing to AMC edge connector or to the SGMII the switch
- Two Dallas E1/T1 framers connect to the four MSC8154 TDM ports
- P1 and P3 connectors carry MSC8154 GPIO and TDM signals
- The MSC8154 configuration and boot support includes reset configuration source three-bit set by appropriate DIP switches, parallel load of programmable reset configuration word from FPGA registers sampled previously from DIPswitch array, serial configuration and boot from a large (64 KB) or small (1 KB) I^2C EEPROM, boot from serial 8 MB SPI flash, boot from communications ports (from SerDes Serial RapidIO interface or from Ethernet SGMII or RGMII ports)
- Two available debug interfaces, including onboard USB TAP controller (eUTAP) or OnCE 14-pin header for any external TAP controller
- FPGA logic: board control and status register (BCSR), JTAG controller allows full board programming, multiplexing of JTAG source signals, I^2C master and slave controllers, MII controller to program RGMII PHY, SPI controller, boot sequencer configures ADS peripherals for boot over Ethernet, generation of TDM clock and sync, two-digit, 14-segment LED display provides current board settings
- 100 MHz clock oscillator for MSC8154 clock in
- An external pulse generator as clock source connects to the CLKIN connector. The MSC8154 clock output signal may be measured on CLKOUT test point.
- Can function in various main supply configurations (configurable via DIP switches or BCSR) in stand-alone mode with an external power 12 VDC @ 5A when S1 switch is on, or as an AMC card in the MicroTCA system or interconnection with AMC-X-Over card. If the ADS is fed outside, the S1 power switch should be off.
- Onboard power system is comprised of two regulator steps:
  - Primary power system is a Power-One Power Manager with 1.0V POL regulator for MSC8154 loads, including cores, MAPLE and M3, 2.5V for I/O and 3.3V for onboard peripherals, DDR switching power supplies for DDRC1 and DDRC2 ports, LDOs for onboard peripherals are fed from 2.5V and 3.3V POLs and 12V input voltage, voltage supervisor monitors all the ADS power supplies. Power Good (PG) signal and dedicated LED LD14 indicate power system status. Any failures cause nPRST signal be continuously low.
  - Push buttons: main power-on-reset (SW8), hard reset (SW9), soft reset (SW11), NMI (SW10)

Development Support

Freescale supplies a complete set of CodeWarrior™ DSP development tools for the MSC8154 device. The tools provide easier and more robust ways for designers to develop optimized DSP systems. Whether the application targets a 3G-LTE, TD-SCDMA or WiMAX system, the development environment gives designers everything they need to exploit the advanced capabilities of the MSC8154 architecture. In addition to the ADS board, support tools include:

- Eclipse-based integrated development environment (IDE)
- C and C++ compiler with in-line assembly
- Librarian
- Multicore debugger
- Royalty-free RTOS
- Software simulator
- Profiler
- High-speed run control
- Host platform support

Contact your local sales office or representative for availability.

Visit **www.freescale.com/8154DSP** for more information.

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

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