INA826SEVM

This user's guide describes the characteristics, operation, and use of the evaluation module (EVM) for the INA826S. The EVM is designed to evaluate the performance of the device in both single and dual-supply configurations. This document also includes the schematic, printed circuit board (PCB) layouts, and a complete bill of materials (BOM). Throughout this document the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the INA826SEVM.

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1 Introduction and Overview

1.1 INA826S

The INA826S is a low-power, wide-supply voltage instrumentation amplifier that can operate in both single and dual supply configurations. A single external resistor sets the gain from 1 to 1000. The input voltage range extends from the negative power supply to 1.0 V below the positive power supply. The rail-to-rail output allows for use in low-voltage applications. The device operates with a supply voltage between 3 V and 36 V and draws a maximum quiescent current of 300 µA. The device is available in a DFN-10 package.

1.2 INA826SEVM

The INA826SEVM is intended to provide basic functional evaluation of the INA826S. It provides the following features:

- Easy access to nodes with surface-mount test points
- Flexible configuration of the Enable function
- Reference voltage source flexibility
- Convenient input and output filtering

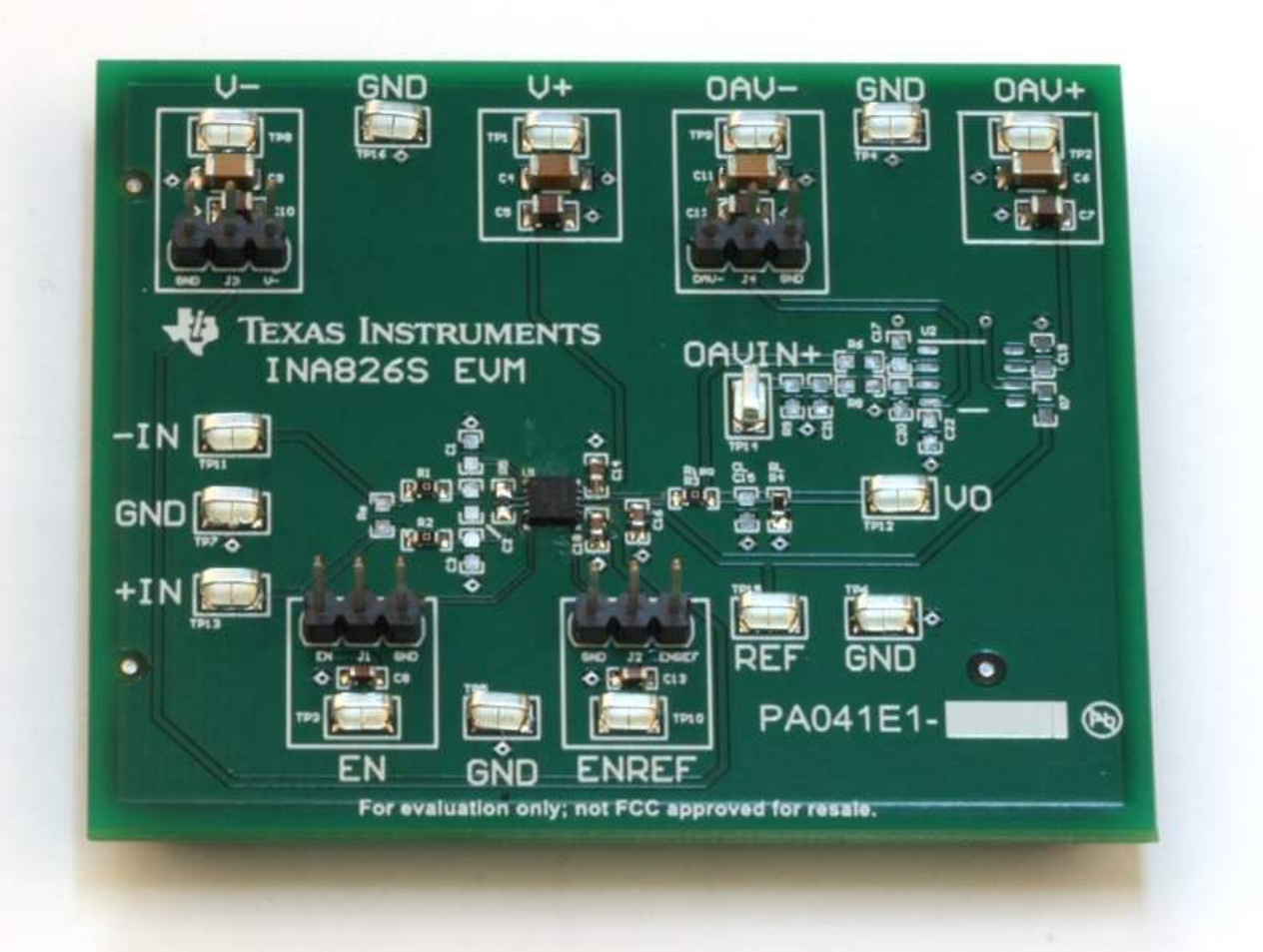

Figure 1. INA826SEVM Board

2 Quick Start

The procedures presented in this section describe how to quickly set up and use the INA826SEVM for evaluation in dual-supply and single-supply configurations.

2.1 Dual Supply

Make the following connections to set up the INA826SEVM for dual-supply operation.

1. 15 V to V+ test point
2. –15 V to V– test point
3. Ground to REF test point or replace C16 with a 0-Ω resistor
4. Differential input (for example, a 1-V_{PP} sine wave) to –IN and +IN test points.

NOTE: If using a signal generator there may not be a return path for bias current. In this case, install 100-kΩ resistors at the C1 and C3 footprints.

5. Oscilloscope to VO test point
6. Set J2 to ENREF position
7. Connect ENREF TP to V +
8. Connect EN TP to V+
9. Set J1 to GND position

Figure 2 depicts a proper dual-supply configuration.

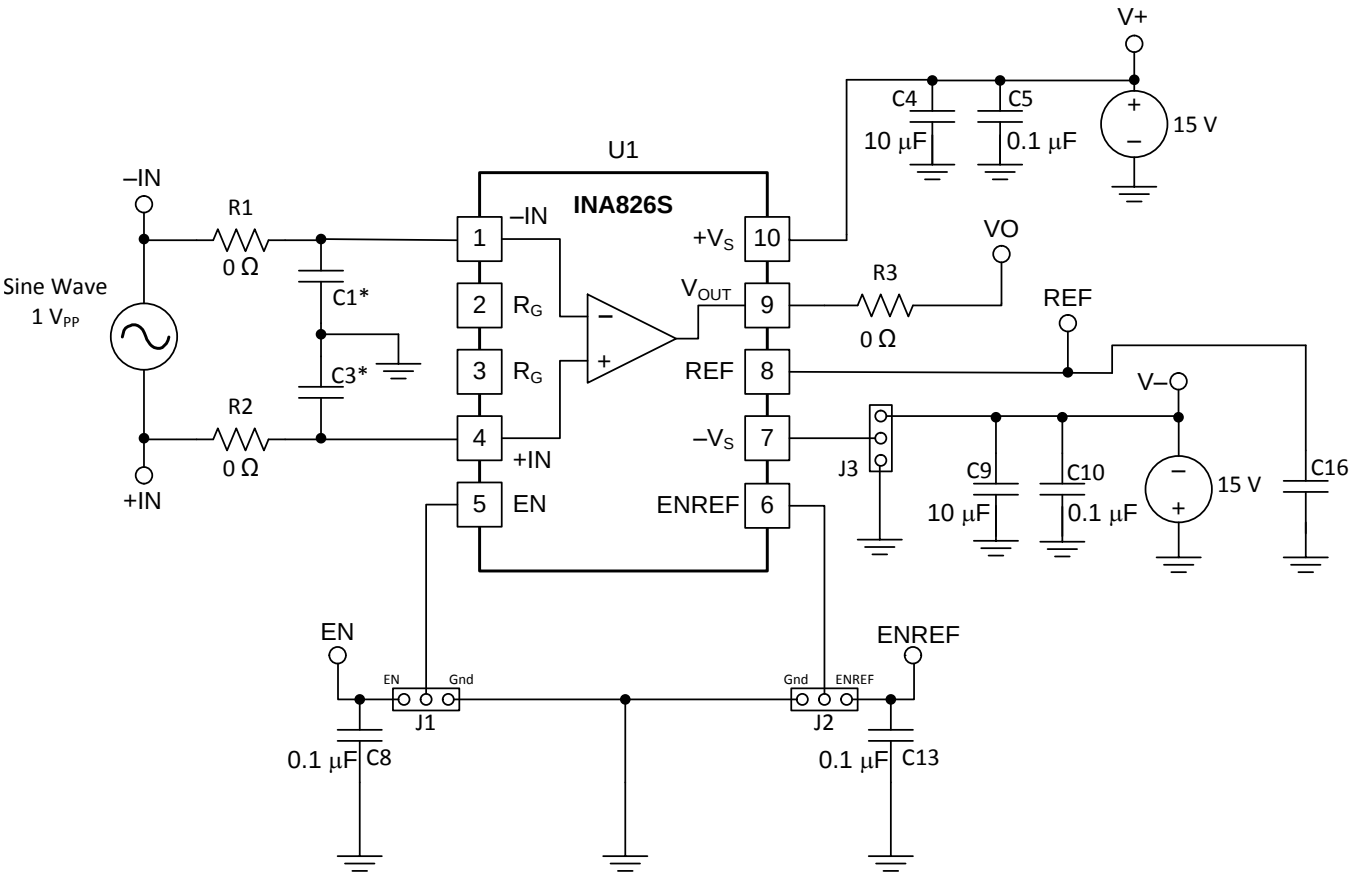

Figure 2. INA826SEVM: Dual-Supply Configuration

2.2 Single Supply

Make the following connections to set up the INA826SEVM for single-supply operation with a direct connection for the reference voltage.

1. 5 V to V+ test point
2. Set J3 to GND position
3. 2.5 V to REF test point
4. Differential input (for example, a 1-V_{PP} sine wave) to –IN and +IN test points.

NOTE: If using a signal generator there may not be a return path for bias current. In this case, install 100-kΩ resistors at the C1 and C3 footprints.

5. Oscilloscope to VO test point
6. Set J2 to ENREF position
7. Connect ENREF TP to V+
8. Connect EN TP to V+
9. Set J1 to GND position

Figure 3 depicts a proper single-supply configuration with a direct REF connection.

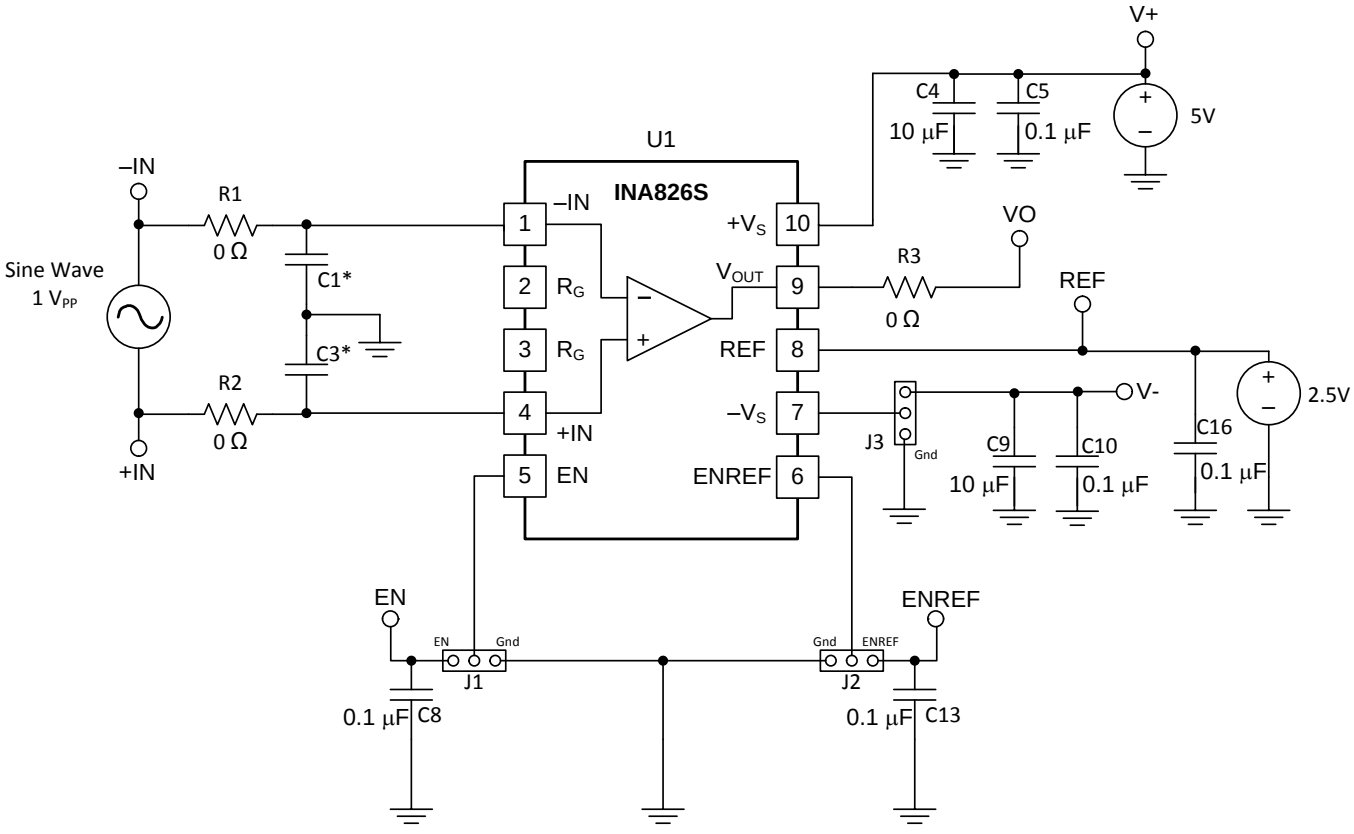

Figure 3. INA826SEVM: Single-Supply Configuration, Direct REF Connection

Make the following connections to set up the INA826SEVM for single-supply operation with a buffered reference voltage. This example uses an OPA376 as the buffer operational amplifier. Depending on the application, alternate single-supply buffer operational amplifiers include the OPA330 and OPA378. The OPA277 is a good choice for high-voltage applications. The buffered configuration is useful when the source impedance is high (for example, a voltage divider). Buffering a high-impedance source with an operational amplifier provides a low-impedance source, which preserves common-mode rejection.

1. 5 V to V+ and OAV+ test points
2. Set J3 and J4 to GND
3. 2.5 V to OAVIN+ test point
4. Populate the C17 footprint with a 0-Ω resistor
5. Differential input (for example, a 1-V_{PP} sine wave) to –IN and +IN test points.

NOTE: If using a signal generator there may not be a return path for bias current. In this case, install 100-kΩ resistors at the C1 and C3 footprints.

6. Oscilloscope to VO test point
7. Set J2 to ENREF position
8. Connect ENREF TP to V+
9. Connect EN TP to V+
10. Set J1 to GND position

Figure 4 depicts a proper dual-supply configuration with a buffered REF voltage.

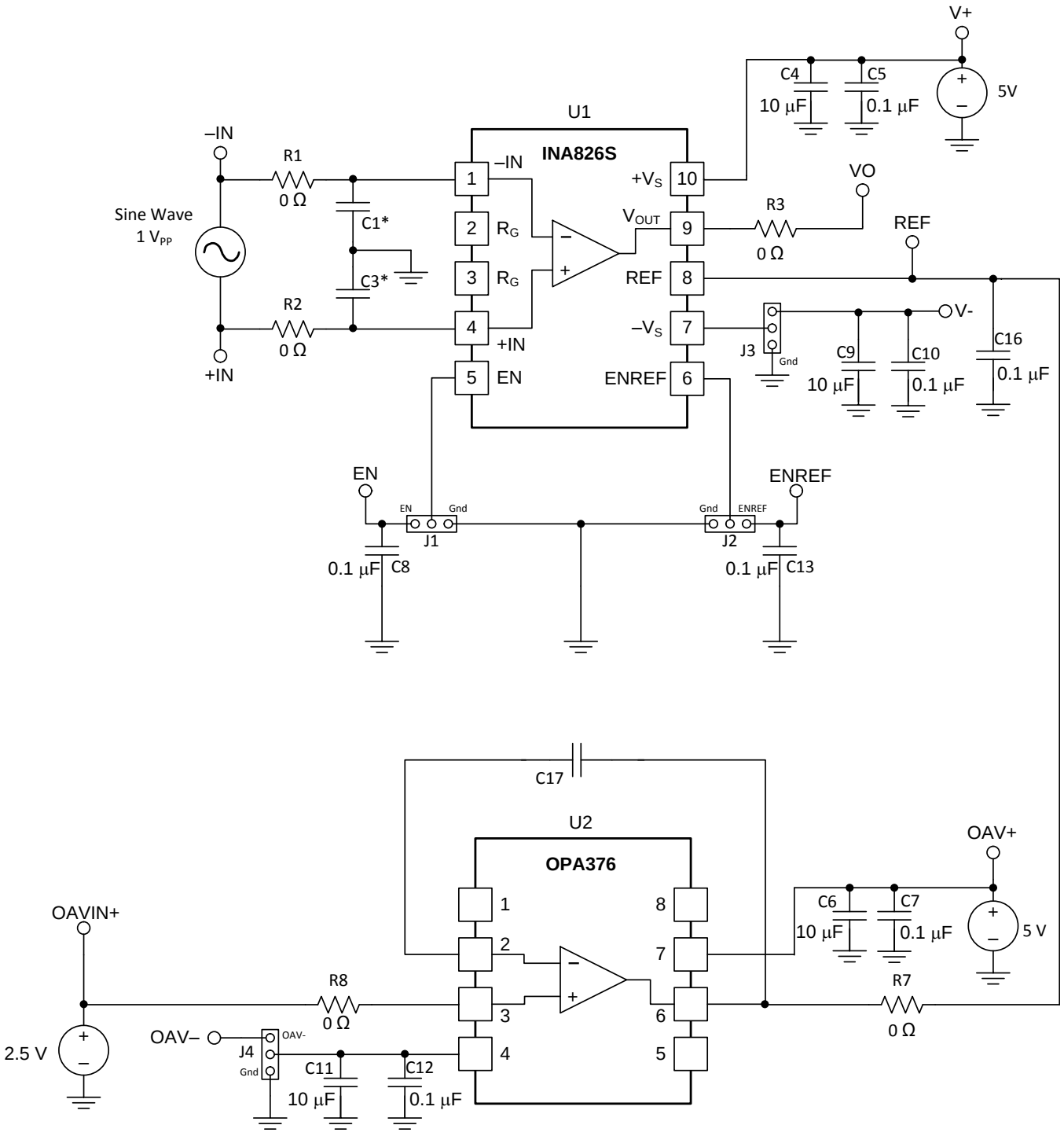

Figure 4. INA826SEVM: Single-Supply Configuration, Buffered REF Connection

3 EVM Components

This section summarizes the INA826SEVM components.

3.1 Power

Power is applied to the INA826S with test points V+ and V–. For the unpopulated device (U2), power is applied using test points OAV+ and OAV–.

3.2 Inputs

Inputs are applied to the INA826S using test points +IN and –IN. The input for U2 is applied via test point OAVIN+.

3.2.1 Input Filtering

R1, R2, and C1 through C3 provide the ability to apply common-mode and differential-mode filtering to the inputs. The cutoff frequencies for the filters are shown in Equation 1 and Equation 2. It is recommended to make C2 approximately ten times larger than C1 and C3. These calculations presume R1 = R2 and C1 = C3.

Common-mode cutoff frequency:

$$f_{c-cm} = \frac{1}{2\pi \times R1 \times C1} \quad (1)$$

Differential-mode cutoff frequency:

$$f_{c-dm} = \frac{1}{2\pi (R1 + R2)\left(C2 + \frac{C1}{2}\right)} \quad (2)$$

3.3 Outputs

The output of the INA826S can be accessed with test point VO.

3.3.1 Output Filtering

R3 and C15 provide the ability to apply a single-pole RC output filter. The cutoff frequency of the output filter can be calculated as shown in Equation 3.

$$f_{c-o} = \frac{1}{2\pi \times R3 \times C15} \quad (3)$$

3.4 Reference

There are multiple methods of applying a reference voltage to the INA826S. A straightforward approach is to apply a voltage to the REF test point with U2 not populated. If a buffered voltage is desired, U2 can be populated with an operational amplifier in an appropriate SO-8 package and pinout.

4 Schematic

4.1 Schematic

Figure 5 shows the schematic for the INA826SEVM PCB.

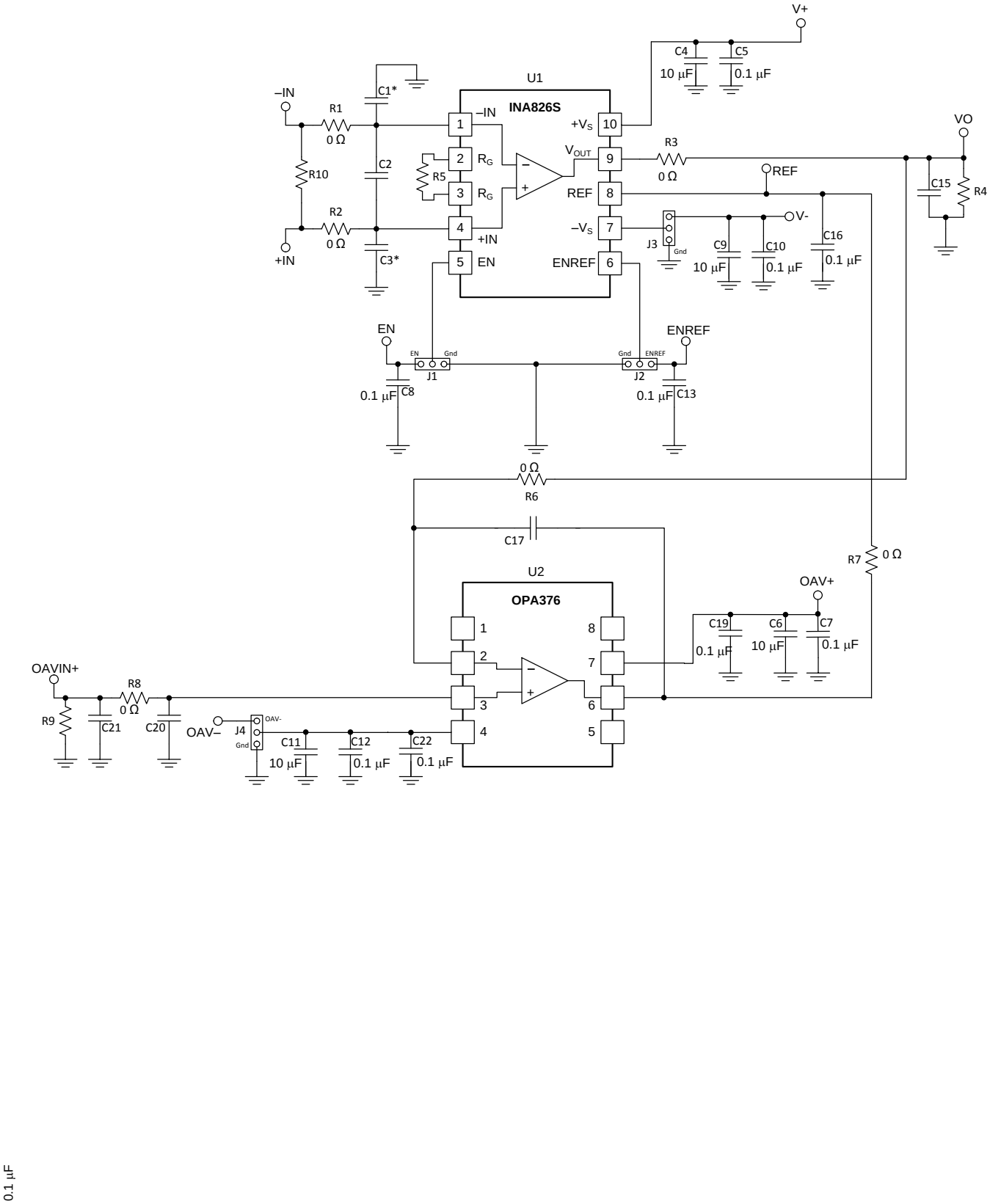

Figure 5. INA826SEVM Schematic

5 Bill of Materials

Table 1 provides the parts list for the INA826SEVM.

Table 1. INA826SEVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C4, C6, C9, C11	4	10uF	CAP, CERM, 10 µF, 50 V, ±10%, X5R, 1206	1206	GRM31CR61H106KA12L	Murata		
C5, C7, C10, C12	4	1uF	CAP, CERM, 1 µF, 100 V, ±10%, X7S, 0805	0805	C2012X7S2A105K125AB	TDK		
C8, C13, C14, C16, C18	5	0.1uF	CAP, CERM, 0.1 µF, 100 V, ±10%, X7S, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7S2A104K080AB	TDK		
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.25 X 0.075, Clear	75x250 mil	SJ5382	3M		
J1, J2, J3, J4	4		Header, 2.54mm, 3x1, Tin, TH	Header, 2.54mm, 3x1, TH	68001-403HLF	FCI		
R1, R2, R3	3	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America		
R4	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic		
SH-J1, SH-J2, SH-J3, SH-J4	4	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	16		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone		
U1	1		Precision, 200uA Supply Current, 36V Supply Instrumentation Amplifier with Shutdown, DRC0010J (VSON-10)	DRC0010J	INA826SIDRCR	Texas Instruments	INA826SIDRCT	Texas Instruments

6 Related Documentation from Texas Instruments

The following documents provide information regarding TI's integrated circuits and support tools for the INA826SEVM.

Related Documentation

Document	Literature Number
INA826S Product Data Sheet	SBOS770
OPA376 Product Data Sheet	SBOS406
OPA277 Product Data Sheet	SBOS079
OPA330 Product Data Sheet	SBOS432
OPA378 Product Data Sheet	SBOS417
REF3225 Product Data Sheet	SBVS058

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

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