Datasheet Brief

MCDP6200

USB Type-C Switching Retimer

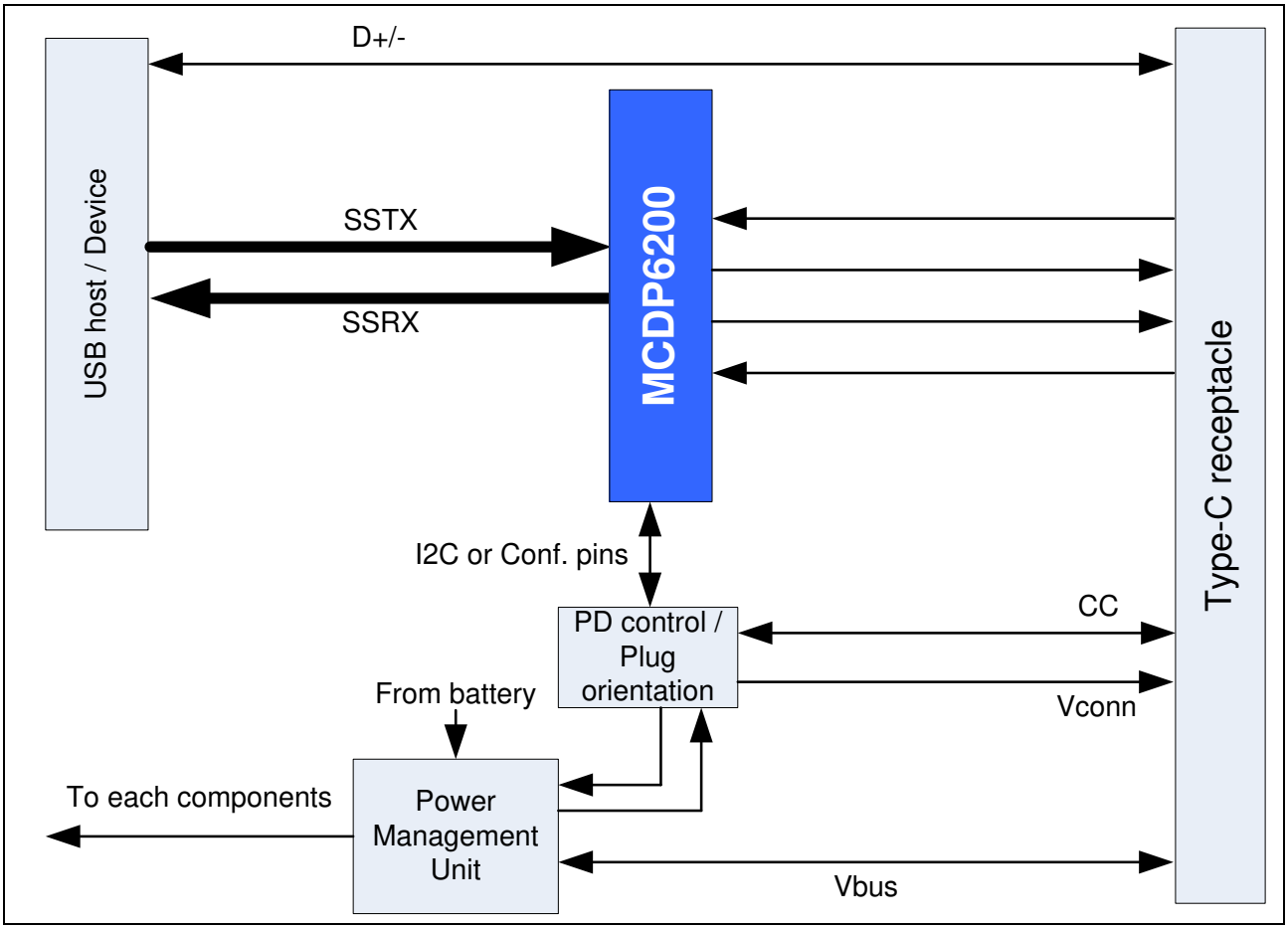
Features

- Integrated USB Type-C lane switch to support
  - Flip-ability of USB Type-C
  - USB 3.2 x1 Gen1 / Gen2 retiming
- Power Supply Voltages
  - 1.8 V for I/O, 1.2 V for core
- USB3.2 Appendix.E x1 Compliant Retimer
  - 5 Gbps and 10 Gbps support
  - Link training participation
  - Spread-spectrum clocking as per USB 3.2 standard
  - LFPS polling and processing
  - LFPS Based PWM support
  - Pass-Through / Local loopback
  - Loopback BERT for USB 3.2 SS
  - Lane polarity inversion
  - BLR (Bit-Level Retimer) for SS mode
    - Low latency data path
    - Link layer snooping
      - 8b/10b coding
      - De-scrambler
      - Link power management support
  - SRIS (Separate Reference clock Independent SSC) for SSP mode
    - 128b/132b coding
    - Scrambler / De-scrambler
    - Link power management support
    - SKP OS handling / Elastic buffer for USB for clock offset compensation
    - DC balance tracking / control
    - Error correction
  - Transmitter Emphasis
    - 3-tap FIR TXEQ for SSP
    - 2-tap TXEQ for SS
  - Adaptive Receiver Equalization
    - DFE + CTLE for SSP to support -23dB insertion loss compensation @5GHz
    - CTLE for SS to support -20dB insertion loss compensation @2.5GHz
  - Support of custom PHY configuration through TWI (Two Wire Interface)
- TWI slave to configure the integrated lane mapping and operation mode
  - Compatible with I2C master
  - Support up to 4 unique TWI device ID
- Configuration pins for the integrated lane switch and operation mode
- Low Power Operation
  - 270mW in USB 3.2 x1 Gen2 mode with 1.2 V and 1.8 V power supply
  - 180mW in USB 3.2 x1 Gen1 mode with 1.2 V and 1.8 V power supply
  - 850 uW in low power state
- ESD Specification
  - 2kV HBM, ±500V CDM
- Package
  - 46 Ex-VQFN (6.5 mm x 4.5 mm)

Applications

- Desktop PC / Notebook / Tablet / Smartphone motherboard enabling USB Type-C
- USB device to drive longer USB Type-C cable

Figure 1. MCDP6200 System Block Diagram



1. Description

The MCDP6200 is a low power USB 3.2 x1 retimer with an integrated USB Type-C switch targeted for desktop / mobile PC motherboard-down and USB Type-C device application.

The USB 3.2 x1 retimer supports both SuperSpeed (SS) bit rate (5 Gbps), and SuperSpeedPlus (SSP) data rate (10 Gbps). The USB 3.2 x1 retimer includes the link layer function and LTSSM and RTSSM to participate in the link training. The MCDP6200 supports SS mode with a BLR (Bit-Level Retimer) and SSP mode with a SRIS (Separate Reference clock Independent SSC). The MCDP6200 supports link power management with Ux entry and exits in both SS and SSP modes. In addition, the MCDP6200 supports the link state and link quality maintenance, compensates the clock offset between the downstream port and the upstream port, detects errors, and corrects single symbol errors in framing order sets, single bit block header errors, and single or double-bit SKP symbol errors in SSP mode. It also supports spread spectrum clocking (SSC) to minimize EMI and the low frequency periodic signaling (LFPS). The transmitter employs 3-tap FIR-based transmitter equalizer for SSP operation and fixed transmitter equalizer ranging from 3 dB to 4 dB for SS operation. The receiver employs an adaptive Continuous Time Linear Equalizer (CTLE) and a Decision Feedback Equalizer (DFE). Both the transmitter equalizer and the receiver equalizer are configurable through the TWI register. Proper settings to comply with USB 3.2 electrical requirements are provided by default.

The MCDP6200 operating mode can be configured through the DIS_N and P_POL pins. It can be optionally configured through TWI by enabling the feature through TWI. These interfaces can be controlled from an external Power Delivery (PD) controller or microcontroller to set the plug orientation and the pin mapping of the USB Type-C. The MCDP6200 operates at 1.8 V and 1.2 V.

The power consumption is:

280 mW in Gen2 operation and 190 mW in Gen1 operation.
850 µW in stand-by state

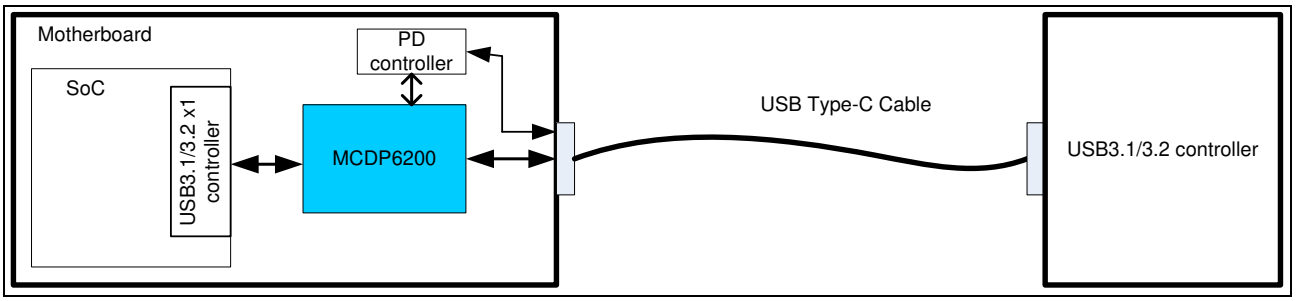
The MCDP6200 is offered in a 46-pin, 6.5 mm x 4.5 mm Ex-VQFN package.

2. Application Overview

The target application of MCDP6200 is the Desktop PC / Notebook / Tablet / Smartphone motherboard and USB Type-C device enabling USB Gen2 bit rate over USB Type-C.

The MCDP6200 resides next to the USB 3.x host or dual-role device, and the Power Delivery (PD) controller on a same PCB with copper tracks connecting directly to these devices. High speed serial interface tracks are typical microstrip lines with controlled impedance of 100 ohm. The MCDP6200 communicates with these devices through either TWI or 2 configuration pins. By default, the operating mode and the plug orientation are controlled by the PD controller or the Embedded Controller (EC) through the two configuration pins.

Figure 2. MCDP6200 Motherboard-Down Use Case



3. Ordering Information

Part Number	Operating Temperature	Package
MCDP6200C1	0°C to +70°C	Ex-VQFN46