Ordering number : ENA2351

LC823425

CMOS LSI

Low Power Consumption 1 chip Audio LSI for Portable Sound Solution

ON Semiconductor®

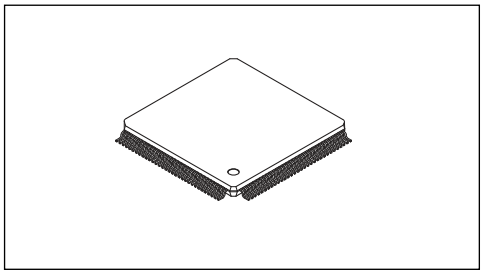
http://onsemi.com

Overview

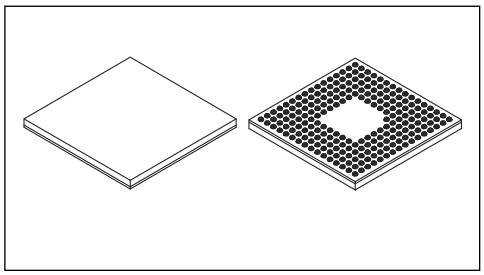
LC823425 is an audio processing solution for portable devices such as IC recorders. This product features a built-in hardwired MP3 encoder/decoder system, enabling the industry's lowest power consumption of 5mW and supporting advanced functionality via a built-in digital signal processor (DSP).

Function

- ARM7TDMI-S™[1], AMBA® (AHB/APB) system
- Internal SRAM(512kbyte), Internal ROM(128kbyte).
  Boot code and built-in standard function
- MultiPort Memory Controller (one CS),
  External Memory Controller (two CS)
- DMA controller (2ch), Interrupt controller
  (external 5ch + enhancing 16ch, and internal 31ch factor)
- SIO(2ch), UART(2ch),
  I^2C (1ch Single Master and Full/Standard conforming)
- General-purpose port (I/O 40ch+1ch (FBGA221J is selected)).
- Plain timer (1ch) and multiple timer (2ch×3), Watch dog timer (1ch)
- 10bit A/D converter (6ch)
- SD card IF(2ch) (w/o CPRM), MemoryStick IF(1ch)
- USB2.0(480Mbps/12Mbps) device IF. Built-in PHY
- RTC (real time clock)
- MP32 hard wired encoder/decoder
- DSP system
  WMA3 (Microsoft WMA Decoder Profile Level3 conforming)
  AAC (MPEG4 LC-AAC)
  Variable speed playback (×0.5-2.0)
- Six band equalizer (EQ3), Highband replication circuit(YY filter), Surround (+EQ2) circuit
- 16/24bit PCM interface, Sampling rate converter, BEEP circuit, Digital mic interface
- DA converter and 16bit audio D class amplifier (LC LPF necessity in the outside)



TQFP128 14x14 / TQFP128L



LFBGA211 11x11 / FBGA221J

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[2] MPEG Layer-3 audio coding technology licensed from Fraunhofer IIS and Thomson.
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* I^2C Bus is a trademark of Philips Corporation.

ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

July, 2014

70914HK 20130617-S00001, 20130425-S00003 No.A2351-1/29

Specifications

Absolute Maximum Ratings at V_{SS}=0V

Item	Symbol	Condition	Ratings	Unit
Maximum power supply voltage	Vdd1 VddRTC VddXT1 AVddUSBPHY1 AVddPLL1		−0.5 to 1.8	V
	AVddDAMPL AVddDAMPR		−0.5 to 2.5	V
	Vdd2 VddSD0 VddSD1 AVddADC AVddPLL2 AVddUSBPHY2		−0.5 to 4.6	V
Input voltage	V_I		−0.5 to V_{DD}+0.5	V
	V_{IUSB}	USBDDP, USBDDM terminal	−0.5 to AVddUSBPHY2+0.5	V
Operating ambient temperature	Topr		−20 to +75	°C
Ambient temperature of preservation	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta=−20°C to +75°C

Item	Symbol	Condition	Low voltage operation			High voltage operation			Unit
			Min	Typ	Max	Min	Typ	Max	
Power-supply voltage	Vdd1		0.93	1.0	1.1	1.1	1.2	1.3	V
	VddXT1		0.93	1.0	1.1	1.1	1.2	1.3	V
	AVddPLL1		0.93	1.0	1.1	1.1	1.2	1.3	V
	AVddPLL2		2.7	3.3	3.6	2.7	3.3	3.6	V
	VddRTC		0.9	1.0	1.3	0.9	1.0	1.3	V
	Vdd2		2.7	3.3	3.6	2.7	3.3	3.6	V
			1.7	1.8	1.95	1.7	1.8	1.95	V
	VddSD0		2.7	3.3	3.6	2.7	3.3	3.6	V
			1.7	1.8	1.95	1.7	1.8	1.95	V
	VddSD1		2.7	3.3	3.6	2.7	3.3	3.6	V
			1.7	1.8	1.95	1.7	1.8	1.95	V
	AVddADC		2.7	3.3	3.6	2.7	3.3	3.6	V
	AVddUSBPHY1		0.93	1.0	1.1	1.1	1.2	1.3	V
	AVddUSBPHY2		2.7(*2)	3.3	3.6	2.7(*2)	3.3	3.6	V
	AVddDAMPL		0.93	1.2	1.65	0.93	1.2	1.65	V
	AVddDAMPR		0.93	1.2	1.65	0.93	1.2	1.65	V
Input voltage range	V_{IN}		0		V_{DD}	0		V_{DD}	V

(*1) Follow the operating frequency specifications because the operating frequency ranges are specified according to the operating voltage ranges.

(*2) When USB is used (include USB suspend state), this should be 3.0V(MIN).

(*3) At any state

-Vdd1=AVddUSBPHY1=AVddPLL1=VddXT1

-Vdd2, VddSD0, VddSD1, AVddPLL2, AVddADC, AVddUSBPHY2, and AVddDAMPL=AVddDAMPR can be supplied with different voltages.
However, whenever Vdd1=AVddUSBPHY1=AVddPLL1=VddXT1Vdd2 is supplied, Vdd2, VddSD0, VddSD1,AVddPLL2, AVddADC, AVddUSBPHY2, and AVddDAMPL=AVddDAMPR must be supplied.

-When only RTC operates, VddRTC can be supplied while *Vdd*=0V(exclude VddRTC) and the BACKUPB=Low input.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Item	Symbol	Condition	Low voltage operation			High voltage operation			Unit
			Min	Typ	Max	Min	Typ	Max	
Oscillation input frequency	Fxin1	ARM7TDMI-S Surrounding of ARM	48MHz±200ppm			The same left			MHz
	FxinRTC	RTC		32.768		The same left			kHz
	Frc	RC	0.4	1	2	The same left			MHz
Time to stabilize of oscillation	Txin1				20[4]	The same left			ms
	TxinRTC				20[5]	The same left			ms
Internal operation frequency	Farm	ARM7TDMI-S	0		55	0		80	MHz
	Fahb	ARM AHB	0		55	0		80	MHz
	Fapb	ARM APB	0		55	0		80	MHz
	Fdsp	DSP	0		110.592	0		110.592	MHz
	Faud(*1)	AUDIO(768fs)	0	33.8688	73.728	The same left			MHz
	Fdec	MP3 Decoder	0	16.9344	36.864	The same left			MHz
	Fenc	MP3 Encoder	0	16.9344	18.432	The same left			MHz

(*1) Almost all of audio functions operate on 256*Fs (sampling frequency) clock,
while SRC(sampling rate converter) and D class amplifier operate on 384*Fs clock.
256*Fs and 384*Fs clocks are generated from 768*Fs base clock.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

[4] Reference value @Ta=25 celsius degree and Vdd1=1.0V, and depends on circumstances.

[5] Reference value @Ta=25 celsius degree and VddRTC =1.0V, and depends on circumstances.

Electrical Characteristics

at Vdd2=2.7V to 3.6V, VddRTC=0.9V to 1.3V, VddSD0=2.7V to 3.6V, VddSD1=2.7V to 3.6V,
Ta=−20°C to +75°C

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H level voltage	V_{IH}	(1)		0.7×Vdd2			V
		(2)		0.7×VddSD0			V
		(3)		0.7×VddSD1			V
		(4)	Schmidt	0.75×Vdd2			V
		(5)		0.7×VddRTC			V
		(6)	Schmidt	0.7×VddRTC			V
Input L level voltage	V_{IL}	(1)				0.3×Vdd2	V
		(2)				0.3×VddSD0	V
		(3)				0.3×VddSD1	V
		(4)	Schmidt			0.25×Vdd2	V
		(5)				0.2×VddRTC	V
		(6)	Schmidt			0.2×VddRTC	V
Output H level voltage	V_{OH}	(7)	I_{OH}=−2mA	Vdd2−0.4			V
		(8)		VddSD0−0.4			V
		(9)		VddSD1−0.4			V
		(10)	I_{OH}=−4mA	Vdd2−0.4			V
		(12)		VddSD0−0.4			V
		(13)		VddSD1−0.4			V
		(11)	I_{OH}=−8mA	Vdd2−0.4			V
		(12)	I_{OH}=−12mA	VddSD0−0.4			V
		(13)		VddSD1−0.4			V
Output L level voltage	V_{OL}	(7)	I_{OL}=2mA			0.4	V
		(8)				0.4	V
		(9)				0.4	V
		(10)	I_{OL}=4mA			0.4	V
		(12)				0.4	V
		(13)				0.4	V
		(11)	I_{OL}=8mA			0.4	V
		(12)	I_{OL}=12mA			0.4	V
		(13)				0.4	V
		(14)	I_{OL}=0.3mA			0.3	V
Pull-up resistor	Rup	(15)		50	80	170	kΩ
		(16)		50	80	170	kΩ
		(17)		25	50	75	kΩ
Pull-down resistor	Rdn	(16)		10	17	40	kΩ
		(17)		10	17	40	kΩ
		(18)		10	17	40	KΩ
Input Leake current	I_{IL}	(1)(2) (3)(4) (5)(6)	V_I=V_{DD}*=V_{SS}	−10		10	μA
Output leakage current	I_{OZ}	(7)(8) (9)(10) (11)(12) (13)(14)	When Hi-Z is output	−10		10	μA

at Vdd2=1.7V to 1.95V, VddSD0=1.7V to 1.95V, VddSD1=1.7V to 1.95V,
Ta=−20°C to +75°C

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H level voltage	V_{IH}	(1)		0.7×Vdd2			V
		(2)		0.7×VddSD0			V
		(3)		0.7×VddSD1			V
		(4)	Schmidt	0.75×Vdd2			V
Input L level voltage	V_{IL}	(1)				0.3×Vdd2	V
		(2)				0.3×VddSD0	V
		(3)				0.3×VddSD1	V
		(4)	Schmidt			0.25×Vdd2	V
Output H level voltage	V_{OH}	(7)	I_{OH}=−1mA	Vdd2−0.4			V
		(8)		VddSD0−0.4			V
		(9)		VddSD1−0.4			V
		(10)	I_{OH}=−2mA	Vdd2−0.4			V
		(12)		VddSD0−0.4			V
		(13)		VddSD1−0.4			V
		(11)	I_{OH}=−4mA	Vdd2−0.4			V
		(12)	I_{OH}=−6mA	VddSD0−0.4			V
		(13)		VddSD1−0.4			V
Output L level voltage	V_{OL}	(7)	I_{OL}=1mA			0.4	V
		(8)				0.4	V
		(9)				0.4	V
		(10)	I_{OL}=2mA			0.4	V
		(12)				0.4	V
		(13)				0.4	V
		(11)	I_{OL}=4mA			0.4	V
		(12)	I_{OL}=6mA			0.4	V
		(13)				0.4	V
Pull-up resistor	Rup	(15)		90	175	350	kΩ
		(16)		90	175	350	kΩ
		(17)		10	50	100	kΩ
Pull-down resistor	Rdn	(16)		20	40	100	kΩ
		(17)		20	40	100	kΩ
		(18)		20	40	100	KΩ
Input Leake current	I_{IL}	(1)(2) (3)(4) (5)(6)	V_I=V_{DD}*=V_{SS}	−10		10	μA
Output leakage current	I_{OZ}	(7)(8) (9)(10) (11)(12) (13)(14)	When Hi-Z is output	−10		10	μA

(1) TDI, TMS, TCK, PHI, SDI0, SDO0, DIN, DOUT, MPMCDATA[15:0], MPMCADDR14, EXD[15:0]
(2) SDCMD0, SDAT00, SDAT01, SDAT02, SDAT03, SDWP0, SDCD0
(3) SDCLK1, SDCMD1, SDAT10, SDAT11, SDAT12, SDAT13, SDWP1, SDCD1
(4) TEST, BMODE[2:0], NRES, NTRST, MCLK, BCK, LRCK, EXTFIQ, EXTINT00, EXTINT01, EXTINT02, EXTINT03, EXTINT04, SCK0, SCK1, SDI1, SDO1, TXD1, RXD1, TXD2, RXD2, SCL, SDA, TIOCA0, TIOCA1, TIOCB0, TIOCB1, TCLKA, TCLKB
(5) VDET
(6) BACKUPB
(7) RTCK, TDO, EXTFIQ, EXTINT00, EXTINT01, EXTINT02, EXTINT03, EXTINT04, SCK0, SDI0, SDO0, SCK1, SDI1, SDO1, SCL, SDA, TXD1, RXD1, TXD2, RXD2, TIOCA0, TIOCA1, TIOCB0, TIOCB1, BCK, LRCK, DIN, DOUT, NCS0, NCS1, NRD, NWRENWRL, NHBNWRH, NLBEXA0, EXA[20:1], EXD[15:0]
(8) SDWP0, SDCD0
(9) SDWP1, SDCD1
(10) MCLK, MPMCCKE, MPMCCS, MPMCWE, MPMCCAS, MCMCRAS, MPMCDQM[1:0], MPMCADDR14, MPMCADDR13, MPMCADDR[10:0], MPMCDATA[15:0], TCLKA, TCLKB
(11) MPMCCLK, PHI
(12) SDCLK0, SDCMD0, SDAT00, SDAT01, SDAT02, SDAT03
(13) SDCLK1, SDCMD1, SDAT10, SDAT11, SDAT12, SDAT13
(14) RTCINT
(15) NTRST, TDI, TMS, TCK
(16) EXTFIQ, EXTINT00, EXTINT01, EXTINT02, EXTINT03, EXTINT04, SCK0, SDI0, SDO0, SCK1, SDI1, SDO1, SCL, SDA, TXD1, RXD1, TXD2, RXD2, TIOCA0, TIOCA1, TIOCB0, TIOCB1, TCLKA, TCLKB, MCLK, BCK, LRCK, DIN, DOUT, MPMCADDR14, SDWP0, SDCD0, SDWP1, SDCD1, PHI
(17) SDCMD0, SDAT00, SDAT01, SDAT02, SDAT03, SDCLK1, SDCMD1, SDAT10, SDAT11, SDAT12, SDAT13
(18) EXD[15:0], MPMCDATA[15:0]

(note 1)
Because the following pins can switch the drive ability when it outputs it by the register setting
VOH and two kinds of VOL are provided for. SDCMD0, SDAT00, SDAT01, SDAT02, SDAT03, SDCLK0, SDCMD1, SDAT10, SDAT1, SDAT12, SDAT13, SDCLK1

(note 2)
It is not included in the DC characteristic about the following pins.
VR, VRH, VRL, USBDDM, USBDDP, USBDEXT12, VCNT1, VCNT2, AN0, AN1, AN2, AN3, AN4, AN5, XIN1, XIN32K, XOUT1, XOUT32K, LOUT, ROUT

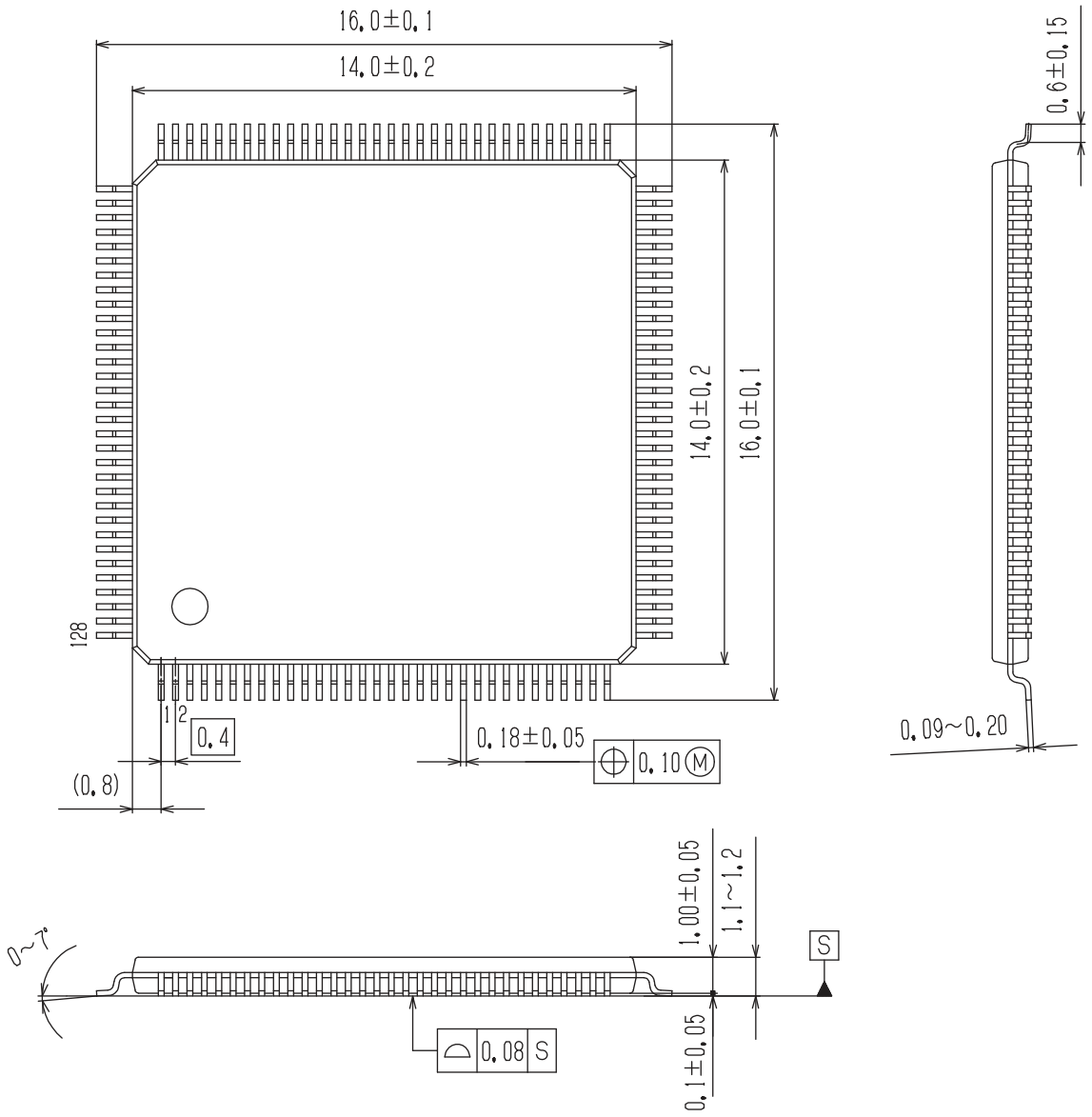
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Package Dimensions

unit : mm

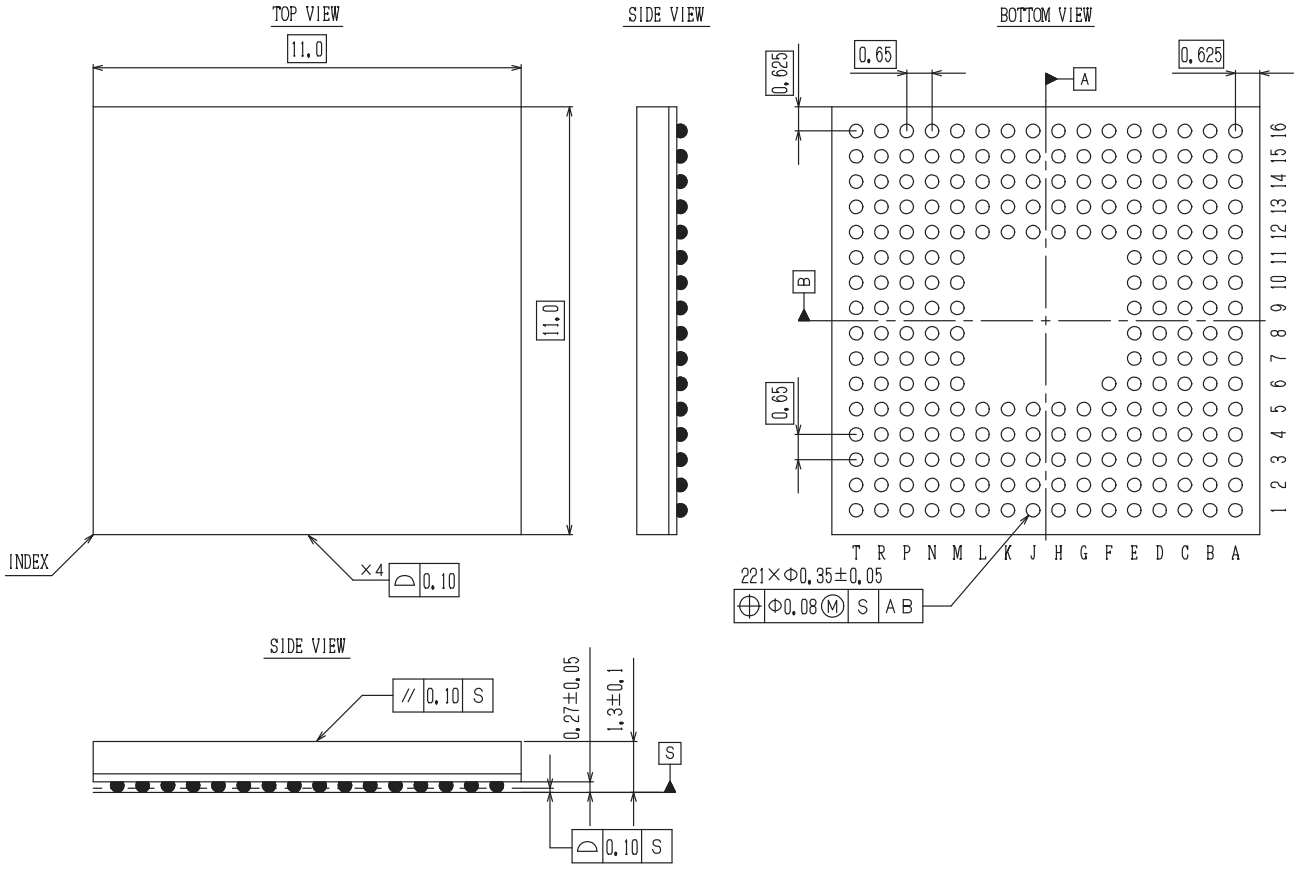
LC823425-12G1-H : TQFP128L

TQFP128 14x14 / TQFP128L
CASE 932BA
ISSUE O



LC823425-13W1-E : FBGA221J

LFBGA221 11x11 / FBGA221J
CASE 566DJ
ISSUE O



Pin Assignment

I/O		Terminal characteristic			
I	Input pin	3IC	3.3 V CMOS input	1IC	1.0 V CMOS input
O	Output pin	3IS	3.3V Schmidt input	1IS	1.0V Schmidt input
B	Interactive pin	3ICU	3.3 V CMOS input pull-up	OD3	0.3mA open drain output
P	Power supply pin	3ISU	3.3V Schmidt input pull-up		
NC	Non Connect	3ICUD	3.3 V CMOS input pull-down Pull-up both correspondences	X	Oscillation amplifier
		3ISUD	3.3V Schmidt input pull-down Pull-up both correspondences	3A	3.3V analogue
		3O4	3.3 V 4mA output	1A	1.0V analogue
		3O8	3.3 V 8mA output		
		3T2	3.3 V 2mA tristate output	3R	3.6V tolerant
		3T4	3.3 V 4mA tristate output		
		3T4(12)	3.3 V 4mA/12mA switch tristate output		

FBGA221J		TQFP128L No.	Pin Name	I/O	Characteristic	Tolerant	IO Power supply	Function
No.	Ball							
1	C3	-	MPMCDATA0	B	3ICD/3T4	3R	b	SDRAM data bus bit0
2	A1	1	BMODE0	I	3IS	3R	b	Boot mode selector bit0
3	D3	-	MPMCDATA1	B	3ICD/3T4	3R	b	SDRAM data bus bit1
4	E4	-	MPMCDATA2	B	3ICD/3T4	3R	b	SDRAM data bus bit2
5	B2	2	BMODE1	I	3IS	3R	b	Boot mode selector bi1
6	E3	-	V_{SS}	P				Digital ground
7	B1	-	MPMCDATA3	B	3ICD/3T4	3R	b	SDRAM data bus bit3
8	C1	-	MPMCDATA4	B	3ICD/3T4	3R	b	SDRAM data bus bit4
9	C2	3	EXTFIQ/GPIO2A	I/B	3ISUD/3T2	3R	b	External FIQ interrupt/general-purpose port
10	D2	-	MPMCADDR0	O	3O4		b	SDRAM address bit0 output
11	F4	4	V_{SS}	P				Digital ground
12	F5	-	Vdd2	P			b	Digital IO power supply
13	E2	-	MPMCADDR1	O	3O4		b	SDRAM address bit1 output
14	D1	-	MPMCADDR2	O	3O4		b	SDRAM address bit2 output
15	F3	5	EXTINT00/GPIO2B	I/B	3ISUD/3T2	3R	b	External interrupt 0-bit0/general-purpose port
16	G4	6	EXTINT01/GPIO2C	I/B	3ISUD/3T2	3R	b	External interrupt 0-bit1/general-purpose port
17	E1	-	MPMCADDR3	O	3O4		b	SDRAM address bit3 output
18	F2	7	EXTINT02/GPIO2D	I/B	3ISUD/3T2	3R	b	External interrupt 0-bit2/general-purpose port
19	F1	-	MPMCADDR4	O	3O4		b	SDRAM address bit4 output
20	G5	-	V_{SS}	P				Digital ground
21	G3	-	MPMCADDR5	O	3O4		b	SDRAM address bit5 output
22	H4	8	EXTINT03/GPIO2E	I/B	3ISUD/3T2	3R	b	External interrupt 0-bit3/general-purpose port
23	G2	-	MPMCADDR6	O	3O4		b	SDRAM address bit6 output
24	G1	-	MPMCADDR7	O	3O4		b	SDRAM address bit7 output
25	H3	9	EXTINT04/GPIO2F	I/B	3ISUD/3T2	3R	b	External interrupt 0-bit4/general-purpose port
26	H1	-	MPMCADDR8	O	3O4		b	SDRAM address bit8 output
27	H2	-	MPMCADDR9	O	3O4		b	SDRAM address bit9 output
28	H5	10	Vdd2	P			b	Digital IO power supply
29	J5	11	V_{SS}	P				Digital ground
30	J1	-	MPMCADDR10	O	3O4		b	SDRAM address bit10 output
31	J4	-	MPMCADDR13	O	3O4		b	SDRAM address bit13 output

32	J2	12	SDCD1/GPIO20	I/B	3ICUD/3T2	3R	s1	SD card Ch1 detecting /general-purpose port
33	J3	13	SDWP1/INS /GPIO21	I/I/B	3ICUD/3T2	3R	s1	SD card Ch1 write-protection /Memory Stick INS/general-purpose port
34	K1	14	SDCMD1/BS /GPIO23	B/I /B	3ICUD /3T4(12)	3R	s1	SD card Ch1 command line /Memory Stick BS/general-purpose port
35	K2	15	SDAT10/DATA0 /GPIO24	B/B /B	3ICUD /3T4(12)	3R	s1	SD card Ch1 data bit0 /Memory Stick data bit0/general-purpose port
36	K3	16	SDAT11/DATA1 /GPIO25	B/B /B	3ICUD /3T4(12)	3R	s1	SD card Ch1 data bit1 /Memory Stick data bit1/general-purpose port
37	K4	17	VddSD1	P			s1	Digital IO power supply (SDI/F Ch1 exclusive use)
38	L1	18	SDAT12/DATA2 /GPIO26	B/B /B	3ICUD /3T4(12)	3R	s1	SD card Ch1 data bit2 /Memory Stick data bit2/general-purpose port
39	L2	19	SDAT13/DATA3 /GPIO27	B/B /B	3ICUD /3T4(12)	3R	s1	SD card Ch1 data bit3 /Memory Stick data bit3/general-purpose port
40	L3	20	SDCLK1/SCLK /GPIO22	O/O /B	3ICUD /3T4(12)	3R	s1	SD card Ch1 clock output /Memory Stick clock /general-purpose port
41	K5	21	V_{SS}	P				Digital ground
42	L4	22	Vdd1	P				Digital internal power supply
43	M1	23	SDCLK0	O	3T4(12)		s0	SD card I/FCh0 clock output
44	M2	24	SDCMD0	B	3ICUD /3T4(12)	3R	s0	SD card I/FCh0 command line
45	M3	25	SDAT00	B	3ICUD /3T4(12)	3R	s0	SD card I/FCh0 data bit0
46	N1	26	SDAT01	B	3ICUD /3T4(12)	3R	s0	SD card I/FCh0 data bit1
47	M4	27	VddSD0	P			s0	Digital IO power supply (SDI/F Ch0 exclusive use)
48	N2	28	SDAT02	B	3ICUD /3T4(12)	3R	s0	SD card I/FCh0 data bit2
49	N3	29	SDAT03	B	3ICUD /3T4(12)	3R	s0	SD card I/FCh0 data bit3
50	P1	30	SDCD0/GPIO29	I/B	3ICUD/3T2	3R	s0	SD card I/FCh0 detecting /general-purpose port
51	P2	31	SDWP0/GPIO28	I/B	3ICUD/3T2	3R	s0	SD card I/FCh0 write-protection /general-purpose port
52	R1	32	V_{SS}	P				Digital ground
53	T1	33	AVddUSBPHY1	P			u1	1.0V power supply for USB-PHY
54	R3	34	AVssUSBPHY	P				Ground for USB-PHY
55	P4	35	AVssUSBPHY	P				Ground for USB-PHY
56	T2	36	USBDDM	B	3A		u2	USB D-
57	T3	37	USBDDP	B	3A		u2	USB D+
58	R4	38	AVddUSBPHY2	P			u2	3.3V power supply for USB-PHY
59	T4	39	AVssUSBPHY	P				Ground for USB-PHY
60	R5	40	AVssUSBPHY	P				Ground for USB-PHY
61	T5	41	USBDEXT12	O	3A		u2	USB-PHY reference resistance
62	P3	42	AVddUSBPHY2	P			u2	3.3V power supply for USB-PHY
63	N4	43	AVddUSBPHY1	P			u1	1.0V power supply for USB-PHY
64	R2	44	AVssUSBPHY	P				Ground for USB-PHY
65	P5	45	VddXT1	P			x1	Power supply for oscillation amplifier
66	M5	46	XOUT1	O	X		x1	48MHz oscillation amplifier output for system
67	N5	47	VssXT1	P				Ground for oscillation amplifier
68	L5	48	XIN1	I	X		x1	48MHz oscillation amplifier input for system
69	T6	49	AVddPLL1	P			p1	Analog power supply for PLL1
70	P6	50	VCNT1	O	1A		p1	VCO control for PLL1
71	R6	51	AVssPLL1	P				Analog ground for PLL1
72	M6	52	Vdd2	P			b	Digital IO power supply
73	M7	-	MPMCDATA5	B	3ICD/3T4	3R	b	SDRAM data bus bit5
74	N8	53	TCLKA/GPIO00 /MPMCADDR11 /EXTINT10	I/B /O /I	3ISUD/3T4	3R	b	MTM external clock A/general-purpose port /SDRAM address bit11 /external interrupt 1- bit0

75	P7	-	MPMCDATA6	B	3ICD/3T4	3R	b	SDRAM data bus bit6
76	R7	54	TCLKB/GPIO01 /MPMCADDR12 /EXTINT11	I/B /O /I	3ISUD/3T4	3R	b	MTM external clock B/general-purpose port /SDRAM address bit12 /external interrupt 1- bit1
77	T7	-	MPMCDATA7	B	3ICD/3T4	3R	b	SDRAM data bus bit7
78	N7	-	MPMCDATA8	B	3ICD/3T4	3R	b	SDRAM data bus bit8
79	T8	55	PHI/GPIO06 /EXTINT16	O/B /I	3ICUD/3T8	3R	b	System clock output/general-purpose port /external interrupt 1- bit6
80	N6	-	V_{SS}	P				Digital ground
81	P8	56	RTCK	O	3O2		b	JTAG test returned clock
82	N9	-	MPMCDATA9	B	3ICD/3T4	3R	b	SDRAM data bus bit9
83	R8	-	MPMCDATA10	B	3ICD/3T4	3R	b	SDRAM data bus bit10
84	M8	57	TDO	O	3O2		b	JTAG test data output
85	T9	-	MPMCCAS	O	3O4		b	SDRAMCAS output
86	R9	-	MPMCRAS	O	3O4		b	SDRAMRAS output
87	M9	58	V_{SS}	P				Digital ground
88	P9	-	MPMCWE	O	3O4		b	SDRAM write enable output
89	T10	59	NTRST	I	3ISU	3R	b	JTAG test reset input
90	N10	-	Vdd2	P			b	Digital IO power supply
91	M10	60	Vdd1	P				Digital internal power supply
92	R10	-	MPMCCKE	O	3O4		b	SDRAM clock enable output
93	P10	-	MPMCDQM0	O	3O4		b	SDRAM data mask byte lane selector bit0
94	M11	61	NRES	I	3IS	3R	b	External reset input
95	T11	-	MPMCDQM1	O	3O4		b	SDRAM data mask byte lane selector bit1
96	R11	-	MPMCCS	O	3O4		b	SDRAM chip selection output
97	T12	-	MPMCCLK	O	3O8		b	SDRAM clock output
98	N11	-	V_{SS}	P				Digital ground
99	P11	-	MPMCDATA11	B	3ICD/3T4	3R	b	SDRAM data bus bit11
100	T13	62	TDI	I	3ICU	3R	b	JTAG test data input
101	R12	-	MPMCDATA12	B	3ICD/3T4	3R	b	SDRAM data bus bit12
102	M12	-	MPMCDATA13	B	3ICD/3T4	3R	b	SDRAM data bus bit13
103	N12	-	MPMCDATA14	B	3ICD/3T4	3R	b	SDRAM data bus bit14
104	P12	63	TMS	I	3ICU	3R	b	JTAG test mode selection
105	R14	-	MPMCDATA15	B	3ICD/3T4	3R	b	SDRAM data bus bit15
106	R13	-	MPMCADDR14 /GPIO17	O /B	3ICUD/3T4	3R	b	SDRAM address bit14/general-purpose port
107	P13	-	NHBNWRH	O	3T2	3R	b	External memory high byte selection/external memory write
108	P14	64	TCK	I	3ICU	3R	b	JTAG test clock
109	P15	-	NCS1	O	3T2		b	External memory chip selection bit1
110	T15	65	V_{SS}	P				Digital ground
111	R15	66	Vdd2	P			b	Digital IO power supply
112	R16	67	VddRTC	P			r	Power supply for RTC
113	T16	68	XIN32K	I	X		r	32.768KHz oscillation amplifier input for RTC
114	N13	69	VssRTC	P				Ground for RTC
115	T14	70	XOUT32K	O	X		r	32.768KHz oscillation amplifier output for RTC
116	M13	71	VDET	I	1IC		r	RTC power supply down detect input
117	N14	72	RTCINT	O	OD3	3R	r	RTC interrupt signal output
118	P16	73	BACKUPB	I	1IS		r	RTC operation mode (only RTC operating or entire LSI operating)
119	L12	74	Vdd1	P				Digital internal power supply
120	N15	-	NCS0	O	3T2		b	External memory chip selection bit0
121	M14	75	V_{SS}	P				Digital ground

122	K12	76	Vdd2	P			b	Digital IO power supply
123	N16	-	NRD	O	3T2		b	External memory lead
124	L13	77	TEST	I	3IS	3R	b	Test mode input (connect to digital ground usually)
125	M15	-	NWRENWRL	O	3T2		b	External memory low byte external memory write/selection
126	L14	78	BMODE2	I	3IS	3R	b	Boot mode selector bit2
127	M16	-	EXA1	O	3T2		b	External memory address bit1
128	K13	-	EXA2	O	3T2		b	External memory address bit2
129	L15	79	SCL/GPIO07 /EXTINT17	O/B /I	3ISUD/3T2	3R	b	I^2C clock output/general-purpose port /external interrupt 1- bit7
130	J14	-	EXA3	O	3T2		b	External memory address bit3
131	L16	-	EXA4	O	3T2		b	External memory address bit4
132	K14	80	V_{SS}	P				Digital ground
133	K15	-	EXA5	O	3T2		b	External memory address bit5
134	J12	-	EXA6	O	3T2		b	External memory address bit6
135	K16	81	SDA/GPIO08 /EXTINT18	B/B /I	3ISUD/3T2	3R	b	I^2C data/general-purpose port /external interrupt 1- bit8
136	J16	-	EXA7	O	3T2		b	External memory address bit7
137	J13	82	MCLK/GPIO18	B/B	3ISUD/3T4	3R	b	PCM master clock/general-purpose port
138	J15	-	EXA8	O	3T2		b	External memory address bit8
139	H14	-	EXA9	O	3T2		b	External memory address bit9
140	H12	83	BCK/GPIO19	B/B	3ISUD/3T2	3R	b	PCM bit clock/general-purpose port
141	H16	-	EXA10	O	3T2		b	External memory address bit10
142	G15	84	V_{SS}	P				Digital ground
143	H13	85	Vdd2	P			b	Digital IO power supply
144	H15	-	EXA11	O	3T2		b	External memory address bit11
145	G16	86	LRCK/GPIO1A	B/B	3ISUD/3T2	3R	b	PCMLR clock/general-purpose port
146	G12	87	DIN/GPIO1B	I/B	3ICUD/3T2	3R	b	PCM data input/general-purpose port
147	F16		EXA12	O	3T2		b	External memory address bit12
148	G14	88	DOUT/GPIO1C	O/B	3ICUD/3T2	3R	b	PCM data output/general-purpose port
149	G13	-	V_{SS}	P				Digital ground
150	E16	-	EXA13	O	3T2		b	External memory address bit13
151	D16	89	TIOCA0/GPIO09 /EXTINT19	B/B /I	3ISUD/3T2	3R	b	MTMCh0A input capture and output capture/general-purpose port /external interrupt 1- bit9
152	F12	-	EXA14	O	3T2		b	External memory address bit14
153	F15	90	TIOCA1/GPIO0A /EXTINT1A	B/B /I	3ISUD/3T2	3R	b	MTMCh1A input capture and output capture/general-purpose port /external interrupt 1- bit10
154	E11	-	EXA15	O	3T2		b	External memory address bit15
155	C16	-	EXA16	O	3T2		b	External memory address bit16
156	F13	91	Vdd2	P			b	Digital IO power supply
157	E15	92	V_{SS}	P				Digital ground
158	F14	-	EXA17	O	3T2		b	External memory address bit17
159	E12	93	TXD1/GPIO04 /EXTINT14	O/B /I	3ISUD/3T2	3R	b	UARTCh1 transmission data/general-purpose port /external interrupt 1- bit4
160	B16	-	EXA18	O	3T2		b	External memory address bit18
161	E13	-	EXA19	O	3T2		b	External memory address bit19
162	A16	94	RXD1/GPIO05 /EXTINT15	I/B /I	3ISUD/3T2	3R	b	UARTCh1 receive data/general-purpose port /external interrupt 1- bit5
163	D15	-	EXA20	O	3T2		b	External memory address bit20
164	E14	-	NLBEXA0	O	3T2	3R	b	External memory low byte selection
165	C15	95	Vdd1	P				Digital internal power supply
166	B15	-	EXD0	B	3ICD/3T2	3R	b	External memory data bus bit0

167	D14	-	V_{SS}	P				Digital ground
168	A15	96	TIOCB0/GPIO02 /DMCKO /EXTINT12	B/B /O /I	3ISUD/3T2	3R	b	MTMCh0B input capture and output capture/general-purpose port /digital mic clock output /external interrupt 1- bit2
169	C14	-	EXD1	B	3ICD/3T2	3R	b	External memory data bus bit1
170	D13	-	EXD2	B	3ICD/3T2	3R	b	External memory data bus bit2
171	B14	97	TIOCB1/GPIO03 /DMDIN/EXTINT13	B/B /I/I	3ISUD/3T2	3R	b	MTMCh1B input capture and output capture/general-purpose port /digital mic data input /external interrupt 1- bit3
172	A14	-	EXD3	B	3ICD/3T2	3R	b	External memory data bus bit3
173	C13	-	EXD4	B	3ICD/3T2	3R	b	External memory data bus bit4
174	B13	98	SCK0/GPIO1D	B/B	3ISUD/3T2	3R	b	Cereal I/FCh0 clock/general-purpose port
175	A13	-	EXD5	B	3ICD/3T2	3R	b	External memory data bus bit5
176	C12	99	SDI0/GPIO1E	I/B	3ICUD/3T2	3R	b	Cereal I/FCh0 data input/general-purpose port
177	D12	-	EXD6	B	3ICD/3T2	3R	b	External memory data bus bit6
178	B12	-	EXD7	B	3ICD/3T2	3R	b	External memory data bus bit7
179	D10	100	V_{SS}	P				Digital ground
180	D8	-	Vdd2	P			b	Digital IO power supply
181	C11	101	SDO0/GPIO1F	O/B	3ICUD/3T2	3R	b	Cereal I/FCh0 data output/general-purpose port
182	D11	-	EXD8	B	3ICD/3T2	3R	b	External memory data bus bit8
183	A12	-	EXD9	B	3ICD/3T2	3R	b	External memory data bus bit9
184	B11	102	SCK1/GPIO0D /EXTINT1D	B/B /I	3ISUD/3T2	3R	b	Cereal I/FCh1 clock/general-purpose port /external interrupt 1- bit13
185	A11	-	EXD10	B	3ICD/3T2	3R	b	External memory data bus bit10
186	C10	103	SDI1/GPIO0E /EXTINT1E	I/B /I	3ISUD/3T2	3R	b	Cereal I/FCh1 data input/general-purpose port /external interrupt 1- bit14
187	B10	-	EXD11	B	3ICD/3T2	3R	b	External memory data bus bit11
188	A10	104	SDO1/GPIO0F /EXTINT1F	O/B /I	3ISUD/3T2	3R	b	Cereal I/FCh1 data output/general-purpose port /external interrupt 1- bit15
189	E10	-	V_{SS}	P				Digital ground
190	A9	-	EXD12	B	3ICD/3T2	3R	b	External memory data bus bit12
191	B9	105	TXD2/GPIO0B /EXTINT1B	O/B /I	3ISUD/3T2	3R	b	UARTCh2 transmission data/general-purpose port /external interrupt 1- bit11
192	C9	-	EXD13	B	3ICD/3T2	3R	b	External memory data bus bit13
193	A8	106	RXD2/GPIO0C /EXTINT1C	I/B /I	3ISUD/3T2	3R	b	UARTCh2 receive data/general-purpose port /external interrupt 1- bit12
194	B8	-	EXD14	B	3ICD/3T2	3R	b	External memory data bus bit14
195	E9	107	Vdd2	P			b	Digital IO power supply
196	C8	-	EXD15	B	3ICD/3T2	3R	b	External memory data bus bit15
197	D9	108	V_{SS}	P				Digital ground
198	E8	109	AVssDAMPR	P				Analog ground for RchDAMP
199	A7	110	ROUT	O	3A		d1	RchDAMP output
200	E7	111	AVddDAMPR	P			d1	Analog power supply for RchDAMP
201	D7	112	AVddDAMPL	P			d2	Analog power supply for LchDAMP
202	A6	113	LOUT	O	3A		d2	LchDAMP output
203	B7	114	AVssDAMPL	P				Ground for LChDAMP
204	B6	115	AVssPLL2	P				Analog ground for PLL2
205	C7	116	VCNT2	O	3A		p2	VCO control for PLL2
206	E6	117	AVddPLL2	P			p2	Analog power supply for PLL2
207	C6	118	V_{SS}	P				Digital ground
208	D6	119	Vdd1	P				Digital internal power supply
209	D5	120	AVddADC	P			a	Analog power supply for ADC
210	A5	-	VRH	I	3A		a	ADC high reference voltage

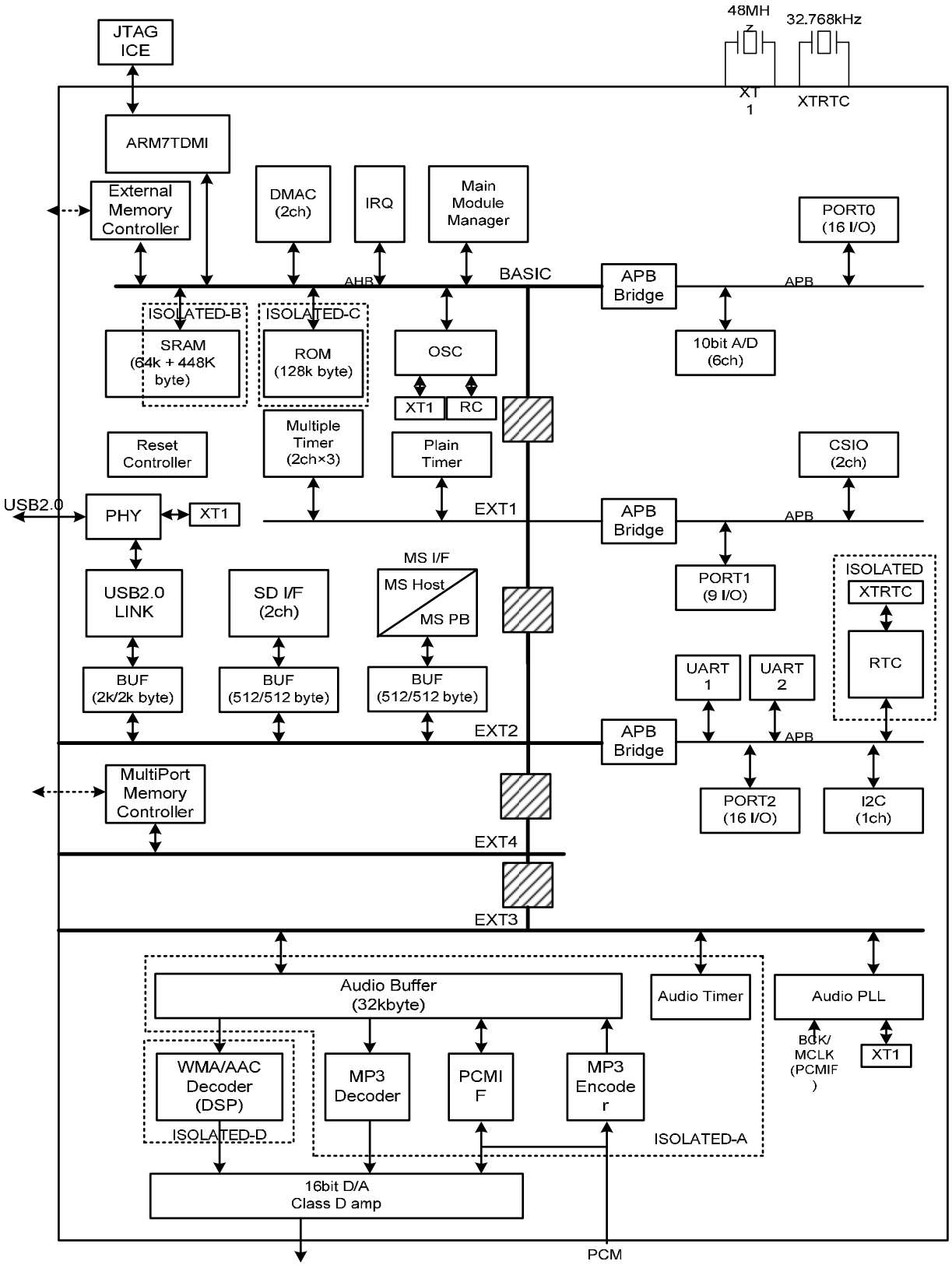
211	B5	121	AN5	I	3A		a	ADC input Ch5
212	A4	122	AN4	I	3A		a	ADC input Ch4
213	C5	123	AN3	I	3A		a	ADC input Ch3
214	B4	124	AN2	I	3A		a	ADC input Ch2
215	A3	125	AN1	I	3A		a	ADC input Ch1
216	B3	126	AN0	I	3A		a	ADC input Ch0
217	C4	-	VR	O	3A		a	ADC standard voltage
218	A2	-	VRL	I	3A		a	ADC [ro-rifarensu] voltage
219	E5	127	AVssADC	P				Analog ground for ADC
220	D4	128	Vdd2	P			b	Digital IO power supply
221	F6	-	-	NC				

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	BMODE0	VRL	AN1	AN4	VRH	LOUT	ROUT	RXD2	EXD12	SDO1	EXD10	EXD9	EXD5	EXD3	TIOCB0	RXD1
B	MPMCDATA	BMODE1	AN0	AN2	AN5	AVssPLL2	AVssDAMP	EXD14	TXD2	EXD11	SCK1	EXD7	SCK0	TIOCB1	EXD0	EXA18
C	MPMCDATA	EXTFIQ	MPMCDATA	VR	AN3	Vss	VCNT2	EXD15	EXD13	SDI1	SDO0	SDI0	EXD4	EXD1	Vdd1	EXA16
D	MPMCADDR	MPMCADDR	MPMCDATA	Vdd2	AVddADC	Vdd1	AVddDAMP	Vdd2	Vss	Vss	EXD8	EXD6	EXD2	Vss	EXA20	TIOCA0
E	MPMCADDR	MPMCADDR	Vss	MPMCDATA	AVssADC	AVddPLL2	AVddDAMP	AVssDAMP	Vdd2	Vss	EXA15	TXD1	EXA19	NLBEXA0	Vss	EXA13
F	MPMCADDR	EXTINT02	EXTINT00	Vss	Vdd2	NC						EXA14	Vdd2	EXA17	TIOCA1	EXA12
G	MPMCADDR	MPMCADDR	MPMCADDR	EXTINT01	Vss							DIN	Vss	DOUT	Vss	LRCK
H	MPMCADDR	MPMCADDR	EXTINT04	EXTINT03	Vdd2							BCK	Vdd2	EXA9	EXA11	EXA10
J	MPMCADDR	SDCD1	SDWP1	MPMCADDR	Vss							EXA6	MCLK	EXA3	EXA8	EXA7
K	SDCMD1	SDAT10	SDAT11	VddSD1	Vss							Vdd2	EXA2	Vss	EXA5	SDA
L	SDAT12	SDAT13	SDCLK1	Vdd1	XIN1							Vdd1	TEST	BMODE2	SCL	EXA4
M	SDCLK0	SDCMD0	SDAT00	VddSD0	XOUT1	Vdd2	MPMCDATA	TDO	Vss	Vdd1	NRES	MPMCDATA	VDET	Vss	NWRENWRL	EXA1
N	SDAT01	SDAT02	SDAT03	AVddUSBP	VssXT1	Vss	MPMCDATA	TCLKA	MPMCDATA	Vdd2	Vss	MPMCDATA	VssRTC	RTCINT	NCS0	NRD
P	SDCD0	SDWP0	AVddUSBP	AVssUSBP	VddXT1	VCNT1	MPMCDATA	RTCK	MPMCWE	MPMCDQM0	MPMCDATA	TMS	NHBNWRH	TCK	NCS1	BACKUPB
R	Vss	AVssUSBP	AVssUSBP	AVddUSBP	AVssUSBP	AVssPLL1	TCLKB	MPMCDATA	MPMCRAS	MPMCCKE	MPMCCS	MPMCDATA	MPMCADDR	MPMCDATA	Vdd2	VddRTC
T	AVddUSBP	USBDDM	USBDDP	AVssUSBP	USBDEXT1	AVddPLL1	MPMCDATA	PHI	MPMCCAS	NTRST	MPMCDQM1	MPMCCLK	TDI	XOUT32K	Vss	XIN32K

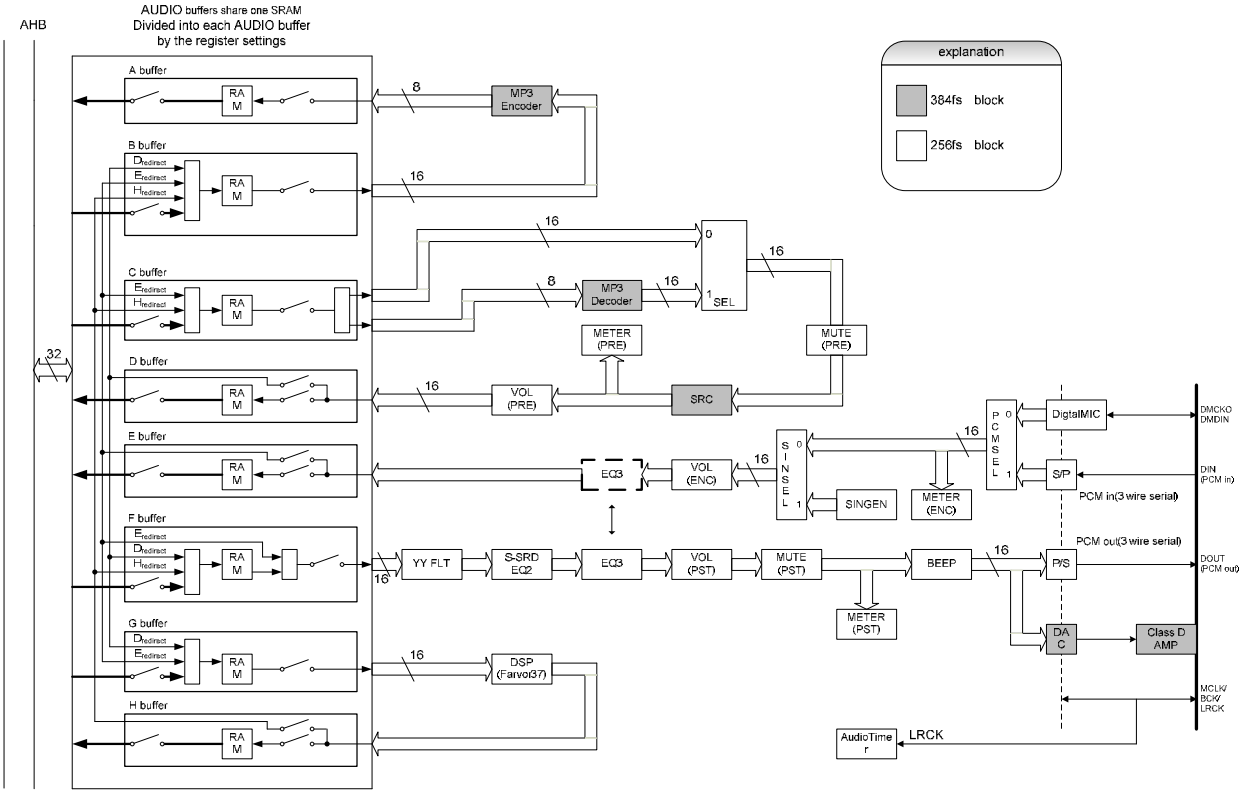
Top View

Block Diagram

Top View



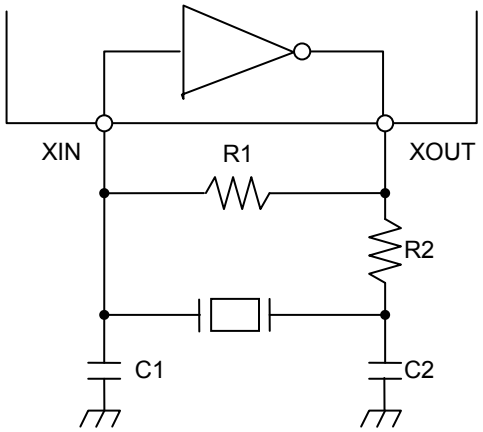
Audio


AHB
AUDIO buffers share one SRAM
Divided into each AUDIO buffer
by the register settings
A buffer
B buffer
C buffer
D buffer
E buffer
F buffer
G buffer
H buffer
RAM
32
8
16
MP3 Encoder
MP3 Decoder
SEL
METER (PRE)
MUTE (PRE)
VOL (PRE)
SRC
EQ3
VOL (ENC)
SINSEL
SINGEN
METER (ENC)
PCMSEL
DigitalMIC
S/P
DMCKO
DMDIN
DIN (PCM in)
PCM in(3 wire serial)
PCM out(3 wire serial)
DOUT (PCM out)
YY FLT
S-SRD EQ2
VOL (PST)
MUTE (PST)
METER (PST)
BEEP
P/S
DAC
Class D AMP
MCLK/ BCK/ LRCK
DSP (Farvoi37)
AudioTimer
LRCK
explanation
384fs block
256fs block

Application Circuit Example

XTAL

Peripheral circuit when oscillation operates



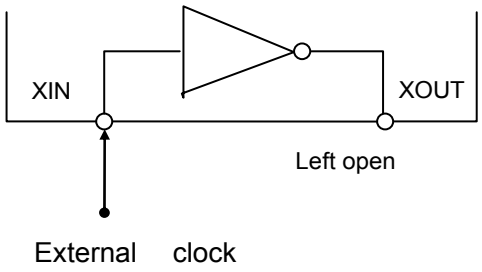
Symbol	Value	
	XIN1/XOUT1 (48MHz)	XIN32K/XOUT32K (32.768KHz)
R1	1MΩ	10MΩ
R2	330Ω	0Ω
C1	6pF	10pF
C2	6pF	10pF

Notes

- Optimize the circuit constant for each product when you use this oscillation cell and ask to the manufacturer of the crystal oscillator to investigate (matching investigation) because the best circuit constant changes depending on the specification of the crystal oscillator used and the ambient surrounding (parasitic capacitance etc. of an external substrate).
- The values of parts are for reference. There is a possibility that the adjustment is needed according to the situation of the set.
- The following may be needed as the anti-noise measures of oscillation circuit.
  (1) Be adjacent as much as possible, and shorten wiring between elements such as this LSI and the crystal oscillator.
  (2) GND of the oscillation circuit close to GND(VSS) of this LSI as much as possible.
  (3) Do not bring the wiring pattern of the large current drive close around the oscillation circuit.
  (4) Take wide pattern to avoid the effect of interference of other signals.

When external clock is input

Do as follows when use the external clock signal that is generated outside of LSI by the oscillation module, etc.



Notes

- Input the signal of a full amplitude to XIN (external clock input).

"the signal of a full amplitude" means

VddXT1 = 0.93V to 1.3V, VddRTC = 0.9V to 1.3V, *Vss* = 0V

Ta =–20°C to +75°C

・Maximum voltage (V_{IH}) : 0.7*Vdd or more, and Vdd or less than Vdd.

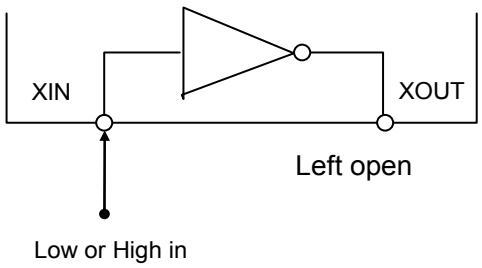
・Minimum voltage (V_{IL}) : 0.3*Vdd or less, and 0V or more than 0V.

(Vdd means VddXT1 in case of XIN1, and VddRTC in case of XIN32K.)

- There is a possibility of influencing the signal quality when there is a long wire pattern on an circuit board of XOUT (The terminal opens).
  Therefore, recommend to cut the wire pattern on an circuit board or no wire pattern on it.

When not use the oscillation cell

Do as follows when not use the oscillation cell.

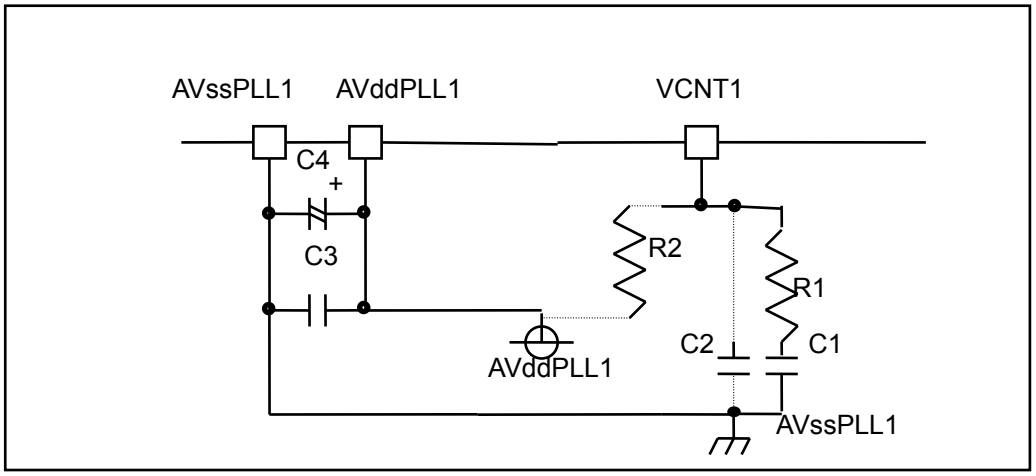


Notes

- Supply the voltage of recommended operating range of
  VddRTC/VssRTC(XIN32K/XOUT32K) even if not use the oscillation cell.
  (power supply to VddXT1/VssXT1(XIN1/XOUT1) is indispensable)

PLL1 (for System)

The figure below shows the PLL1 circuit. Place the decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.



Symbol	Value	Serial number or accuracy
R1	100Ω	±5%
R2	*MΩ	±5%
C1	0.1μF	10% of volume error : ± 10% (–20°C to +75°C) of temperature property : ±
C2	0.001μF	
C3	0.1μF	
C4	33μF	16CV33BS

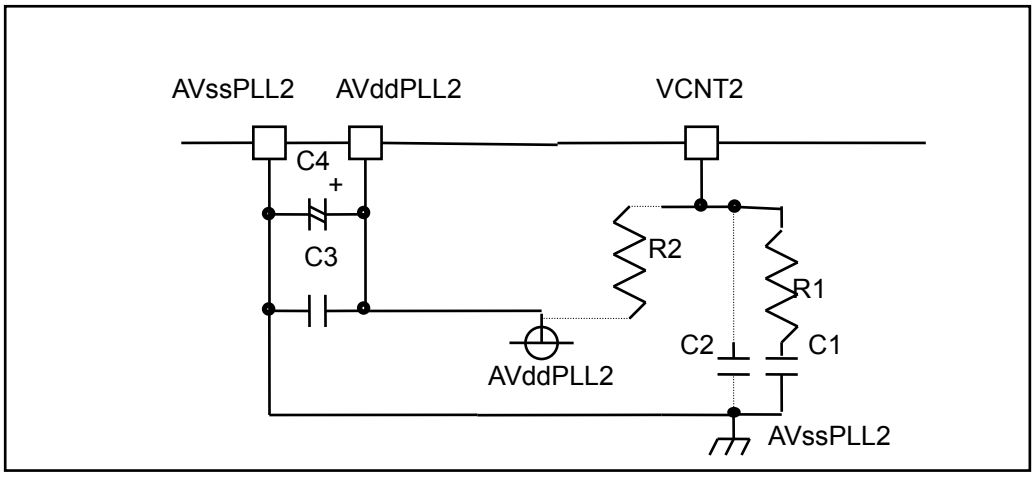
C4 : refers to the part of mounting on the catalog of our company (CV-B S Series).

Notes

- Use R2 basically by unmounting. The characteristic of PLL might be improved by mounting R2. Place the wire pattern.
- The values of parts are for reference. There is a possibility that the adjustment is needed according to the situation of the set.
- Connect with decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.

PLL2 (for Audio)

The figure below shows the PLL2 circuit. Place the decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.



Symbol	Value	Serial number or accuracy
R1	100 to 220Ω	±5%
R2	*MΩ	±5%
C1	4.7μF	10% of volume error : ± 10% of temperature property : ± (–20°C to +75°C)
C2	0.01 About μF	
C3	0.1μF	
C4	33μF	16CV33BS

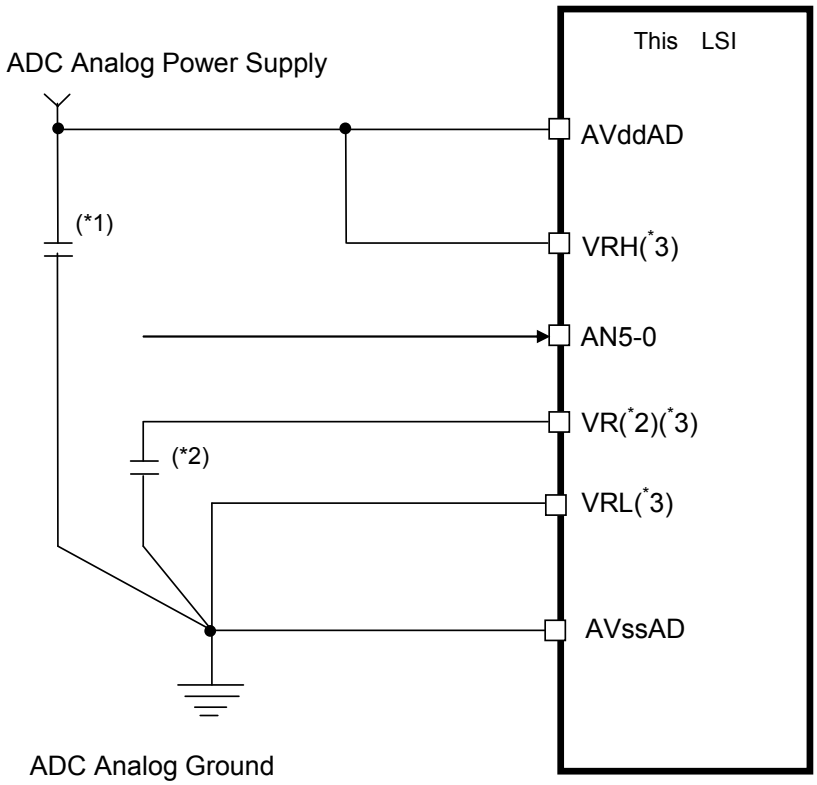
C4 : refers to the part of mounting on the catalog of our company (CV-B S Series).

Notes

- Use R2 basically by unmounting. The characteristic of PLL might be improved by mounting R2. Place the wire pattern.
- The values of parts are for reference. There is a possibility that the adjustment is needed according to the situation of the set.

  Connect with decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.

10bit AD converter



(*1) It is important to get the correct ADC conversion result that the wiring resistance is accurate. Pay attention to keeping low noize.

It is recommended that the ceramic capacitor of the high frequency type to be used as a decoupling capacitor between AVddADC and AVssADC.

Place the capacitor close to the terminal of LSI as much as possible so that the wiring length may be shorten as much as possible.

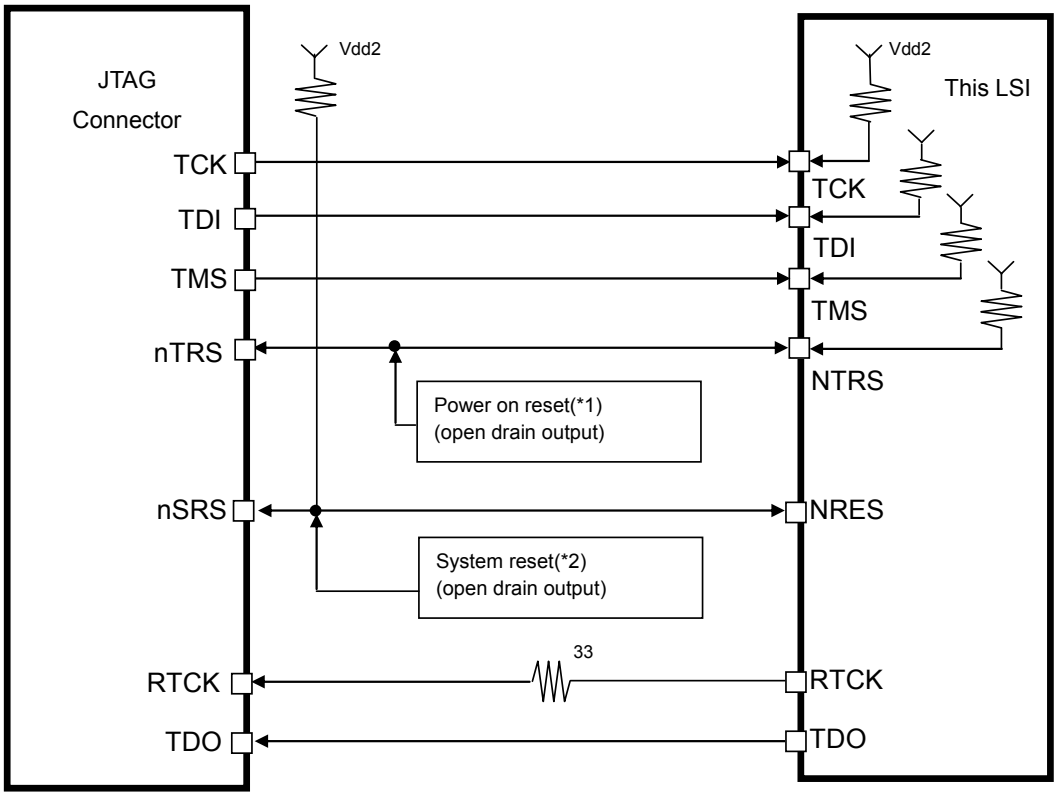
(*2) When the terminal VR is prepared (LC823425-13W1-E:FBGA221J is used), the ADC conversion speed (operation clock frequency) is different depending on the value of the capacitor used. Confirm specs of ADC.

(*3) LC823425-12G1-H:TQFP128L connects VRH and VRL with AVddADC and AVssADC in the package. VR terminal is open in the package.

USB Device

Refer to "USB20PCB design guideline" document .

Example of circuit in surrounding of terminal JTAG (for ICE use and unused)



(*1) Power-on reset is a reset signal that becomes active Low only when the power supply is turned on. The terminal NTRST must be reset only by reset and power-on reset from JTAG.

(*2) System reset is a reset signal that becomes power-on reset and active Low demanded in addition with the system like manual reset etc. The terminal NRES must be reset by reset and system reset from JTAG.

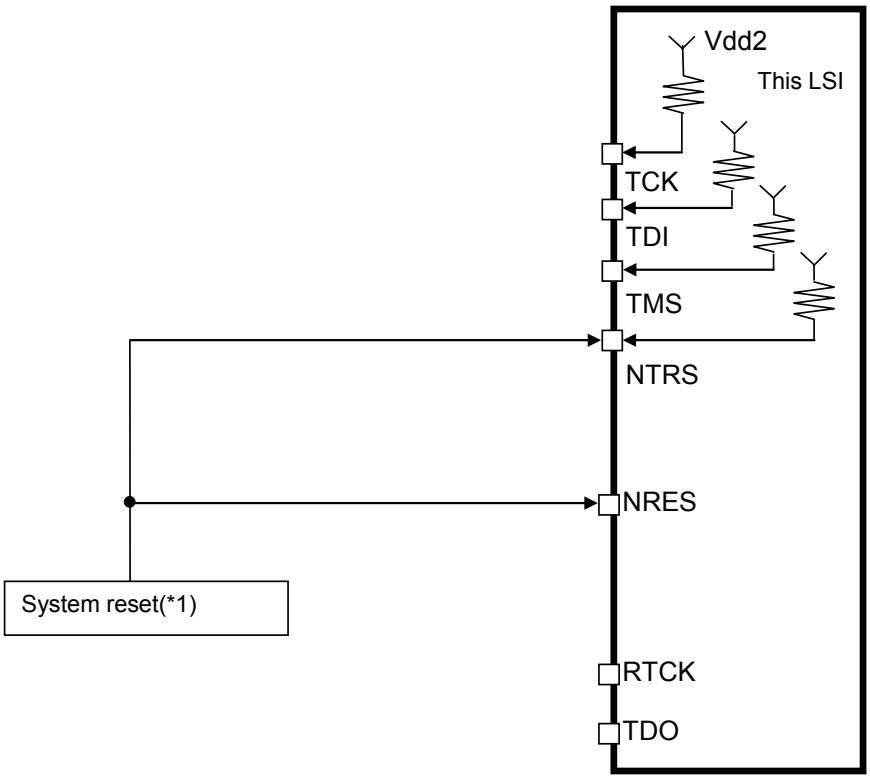
Refer to the data sheet for specs for terminal NRES reset. The terminal NTRST is the same specs as the terminal NRES.

Power-on reset (open drain output) can be realized to connect it with the ground through the capacitor as one example.

As for the ICE unconnection, TCK, TDI, and the terminal TMS open in the state of internal pull-up ON.

The above-mentioned circuit is an example in the surrounding to correspond to both the ICE use and ICE unused cases on the assumption of the JTAG ICE use made of YDC (Yokokawa digital computer).
Ask the manufacturer when you use other products.

Example of circuit in surrounding of terminal JTAG (ICE unused)

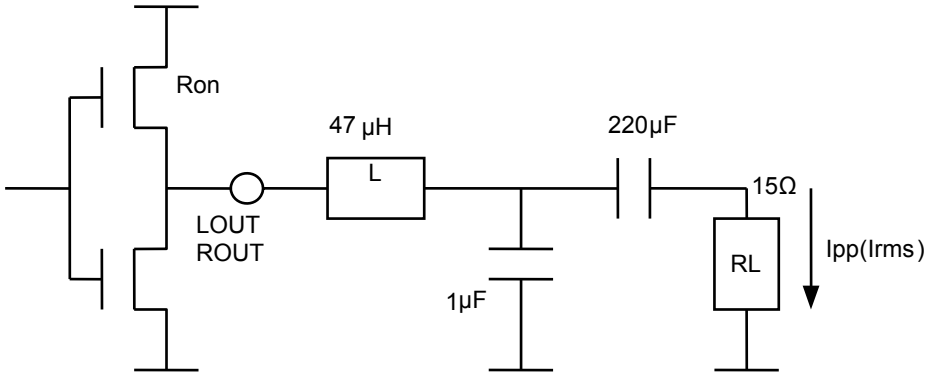


(*1) System reset is a reset signal that becomes power-on reset (reset signal that becomes active Low only when the power supply is turned on) and active Low demanded in addition with the system of manual reset etc.

TCK, TDI, and the terminal TMS open for ICE unused in the state of internal pull-up ON.
Power-on reset is at least necessary for the terminal NTRST in the same specs as the terminal NRES even when ICE unused.

The above-mentioned circuit is an example of the assumption of the case with ICE unused, and the simplification of the circuit in the surrounding.

D class amplifier



Output wattmeter calculation

[Condition]

- The DC resistance element of the coil, capacitor is small.
- Maximum output amplitude =90%[6] to power supply of PWM
- 1.2V=(AVddDAMPL, AVddDAMPR), power-supply voltage of D class amplifier
- 2Ω= Turning on resistance of internal transistor for D class amplifier (Ron).
- 15Ω= Headphone load resistance (RL)

assume the current that flows to the headphone to be Ipp
Ipp = (1200/2) × 0.9 / (15+2) = 31.7(mA)
Irms = Ipp / SQRT(2) = 22.4(mA)
Prms = $Irms^2$ × 15 = 7.53(mW)

External power supply

D class amplifier power supply (AVddDAMPL,AVddDAMPR) must use a transient response and good power supply. When the power supply where the transient response is bad is used and the capacity of the capacitor is small, a peculiar pumping phenomenon to D class amplifier is generated. The power-supply voltage change when the pumping phenomenon is generated must not exceed the recommended operating range.

[6] Theoretical value of Delta-sigma circuit

Power supply sequence

Background

The basis of turn on/off of the power supply is the following order (It is acceptable simultaneously).

- At turning on

  Vdd *(internal) → Vdd *(IO) → Vsig (external signal)

- At turning off

  Vsig (external signal) → Vdd *(IO) → Vdd *(internal)

Turning on of Vdd *(outside) while Vdd *(internal) are turning off might generate the glitch on IO signals and flow of through current.To avoid it, the above-mentioned procedure is recommended as a basis of the sequence.

Recommendation

Example 1 of sequence

After grouping power supply terminals into four ①, ②, ③-1, ③-2 groups, the following order is recommended as a sequence according to a basic policy in this LSI (It is acceptable simultaneously).

- At turning on

  ① → ② → ③-1 → Vsig

- At turning off

  Vsig → ③-1 → ② → ①

(Note)

- ① (internal circuit operation voltage)The internal logic is reset by → ② (reset terminal input) and an irregular state is canceled. Therefore, start up these two power supplies first of all in order of ① → ② (It is acceptable simultaneously).
- ③-Two can be operated alone. Separately, it is assumed the RTC terminal control sequence, describes, and refer.

Example 2 of sequence

The following sequence that makes the power supply at same timing as much as possible and simplifies is possible (It is acceptable simultaneously).

- At turning on

  ① → ②, ③-1 → Vsig

- At turning off

  Vsig → ②, ③-1 → ①

(Note)

- Regarding ③-2, It is supposed that the signal collision with an external device cannot occur. In this case, ③-2 starts up together with ②, ③-1.

Definition of power supply group

① Internal power supply and analog power supplies

① are entire simultaneous power supplies ON, and simultaneous power supplies OFF.

- Vdd1
- VddXT1
- AVddPLL1
- AVddUSBPHY1

② External IO power supply 1

- Vdd2

③-1 External IO power supply2 and analog power supply

- VddSD0
- VddSD1
- AVddUSBPHY2
- AVddADC
- AVddPLL2
- AVddDAMPL
- AVddDAMPR

③-2 Internal and external IO power supply (sharing)

- VddRTC

  (Separately, RTC terminal control sequence is described)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC823425-12G1-H	TQFP128L (Pb-Free / Halogen Free)	450 / Tray JEDEC
LC823425-13W1-E	FBGA221J (Pb-Free)	840 / Tray JEDEC