CD54HCT573, CD74HCT573
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

- **4.5-V to 5.5-V V_{CC} Operation**
- **Wide Operating Temperature Range of −55°C to 125°C**
- **Balanced Propagation Delays and Transition Times**
- **Standard Outputs Drive Up To 10 LS-TTL Loads**
- **Significant Power Reduction Compared to LS-TTL Logic ICs**
- **Inputs Are TTL-Voltage Compatible**

CD54HCT573 . . . F PACKAGE
CD74HCT573 . . . DB, E, OR M PACKAGE
(TOP VIEW)

```
         ___
        | OE [ 1      20 ] V_CC
         1D [ 2      19 ] 1Q
         2D [ 3      18 ] 2Q
         3D [ 4      17 ] 3Q
         4D [ 5      16 ] 4Q
         5D [ 6      15 ] 5Q
         6D [ 7      14 ] 6Q
         7D [ 8      13 ] 7Q
         8D [ 9      12 ] 8Q
        GND [ 10     11 ] LE
```
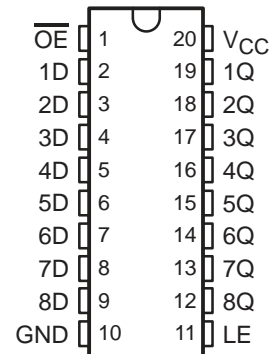
description/ordering information

The 'HCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP – E	Tube	CD74HCT573E	CD74HCT573E
	SSOP – DB	Tape and reel	CD74HCT573DBR	HK573
	SOIC – M	Tube	CD74HCT573M	HCT573M
		Tape and reel	CD74HCT573M96	
	CDIP – F	Tube	CD54HCT573F3A	CD54HCT573F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)

To Seven Other Channels
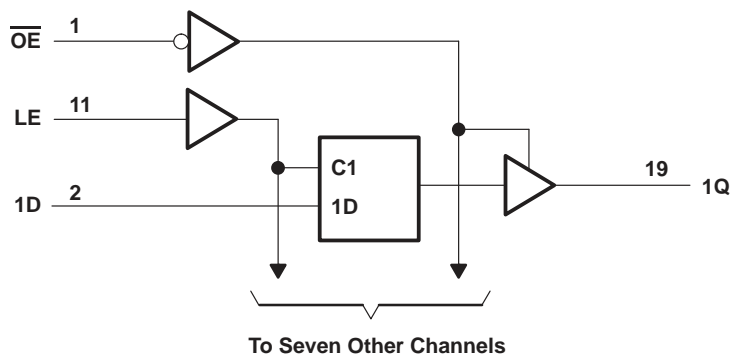
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 1) . . . . ±20 mA
Continuous output drain current per output, I_O (V_O = 0 to V_{CC}) . . . . ±35 mA
Continuous output source or sink current per output, I_O (V_O = 0 to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 70°C/W
                                              E package . . . . 69°C/W
                                              M package . . . . 58°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
            2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		$T_A = 25°C$		$T_A = -55°C$ TO 125°C		$T_A = -40°C$ TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V
V_I	Input voltage		V_{CC}		V_{CC}		V_{CC}	V
V_O	Output voltage		V_{CC}		V_{CC}		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		500		500		500	ns

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$		$T_A = -55°C$ TO 125°C		$T_A = -40°C$ TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20$ μA	4.5 V	4.4		4.4		4.4		V
		$I_{OH} = -6$ mA		3.98		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20$ μA	4.5 V		0.1		0.1		0.1	V
		$I_{OL} = 6$ mA			0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or 0		5.5 V		±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		5.5 V		8		160		80	μA
ΔI_{CC}†	One input at $V_{CC} - 2.1$ V, Other inputs at 0 or V_{CC}		4.5 V to 5.5 V		360		490		450	μA
C_i					10		10		10	pF
C_o					20		20		20	pF

† Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD
$\overline{OE}$	1.25
Any D	0.3
LE	0.65

Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 360 μA max at 25°C).

timing requirements over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	16		24		20		ns
t_{su}	Setup time, data before LE↓	13		20		16		ns
t_h	Hold time, data after LE↓	10		15		13		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 50 pF		35		53		44	ns
	LE				35		53		44	
t_{en}	$\overline{OE}$	Q	C_L = 50 pF		35		53		44	ns
t_{dis}	$\overline{OE}$	Q	C_L = 50 pF		35		53		44	ns
t_t		Q	C_L = 50 pF		12		18		15	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	53	pF

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
RECOVERY TIME

VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following
      characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
   D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
   E. The outputs are measured one at a time, with one input transition per measurement.
   F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   G. t_{PZL} and t_{PZH} are the same as t_{en}.
   H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8685601RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8685601RA CD54HCT573F3A	Samples
CD54HCT573F	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD54HCT573F	Samples
CD54HCT573F3A	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8685601RA CD54HCT573F3A	Samples
CD74HCT573DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK573	Samples
CD74HCT573E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT573E	Samples
CD74HCT573EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT573E	Samples
CD74HCT573M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT573M	Samples
CD74HCT573M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT573M	Samples
CD74HCT573M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT573M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HCT573, CD74HCT573 :

● Catalog: CD74HCT573

● Military: CD54HCT573

NOTE: Qualified Version Definitions:

   ● Catalog - TI's standard catalog product

   ● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS
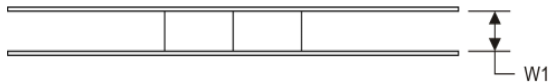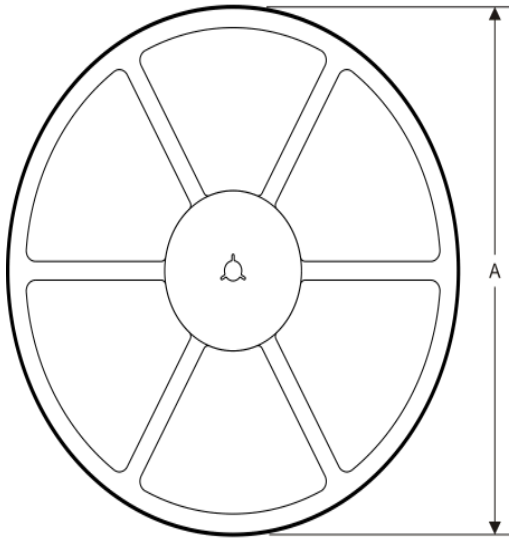
TAPE DIMENSIONS
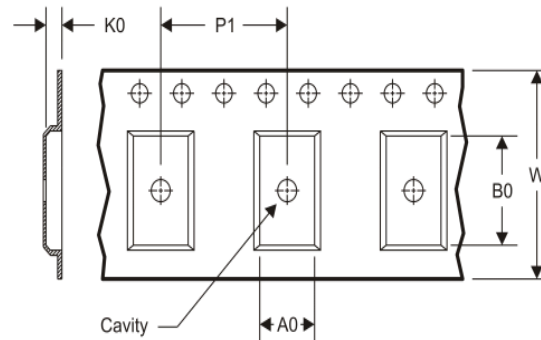
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Cavity

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
CD74HCT573M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT573DBR	SSOP	DB	20	2000	367.0	367.0	38.0
CD74HCT573M96	SOIC	DW	20	2000	367.0	367.0	45.0

J (R–GDIP–T**)   CERAMIC DUAL IN–LINE PACKAGE
14 LEADS SHOWN

DIM ＼ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°–15°

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM	PINS **	14	16	18	20
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION ⟨C⟩		AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) ⟨D⟩

0.045 (1,14)
0.030 (0,76) ⟨D⟩

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⟨D⟩

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
    ⟨C⟩ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
    ⟨D⟩ The 20 pin end lead shoulder width is a vendor option, either half or full width.
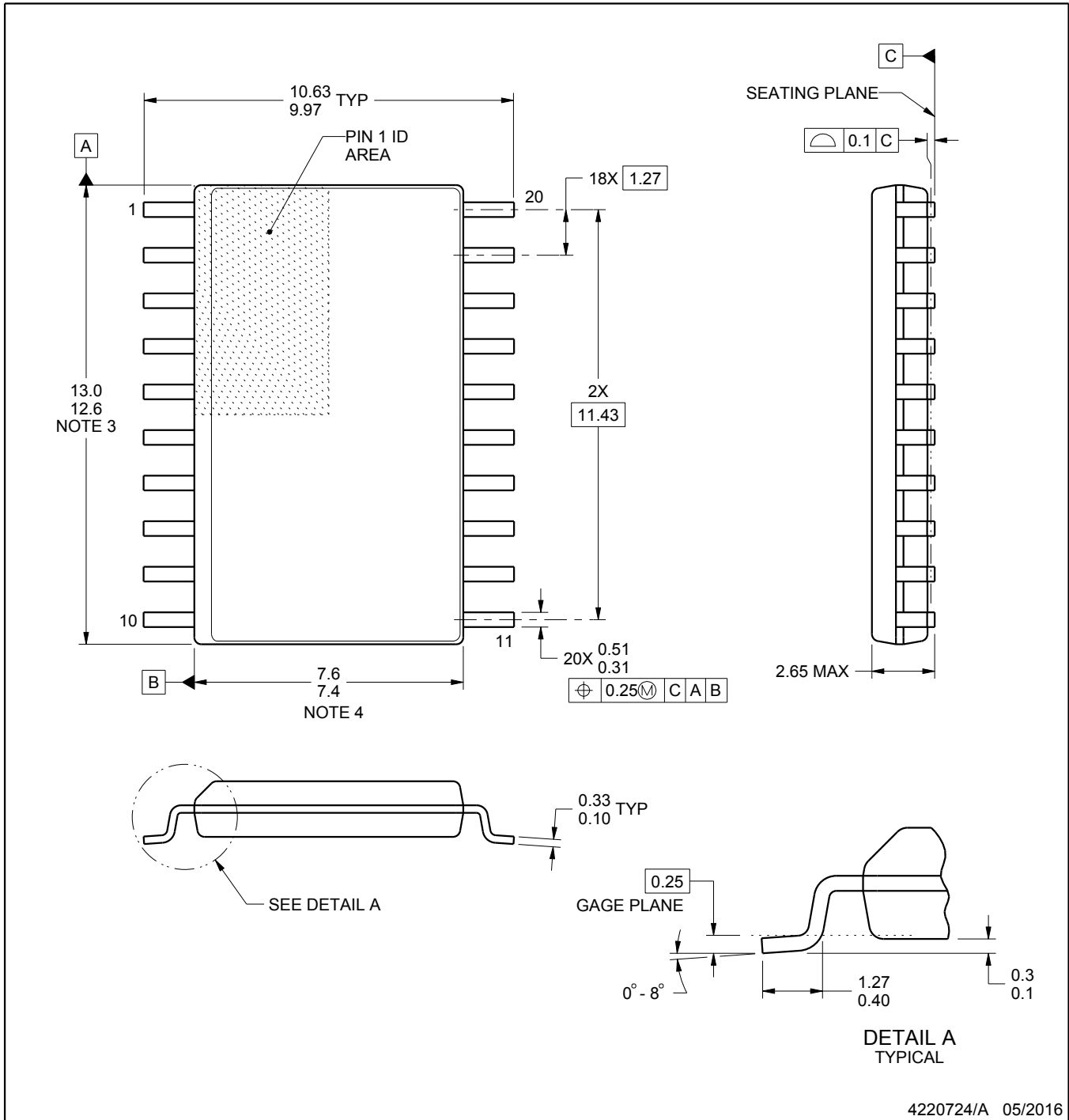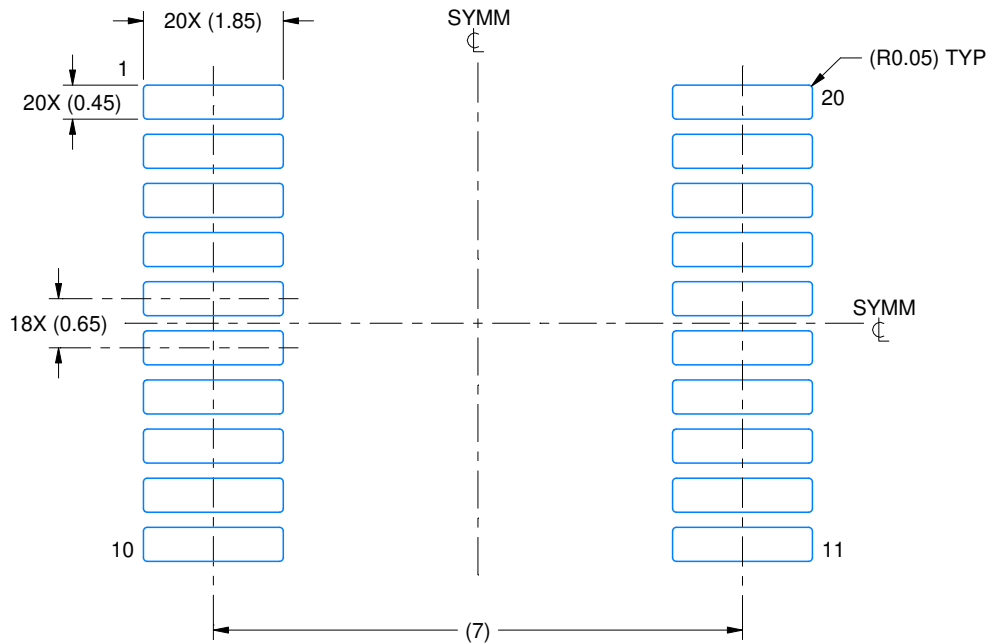
4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
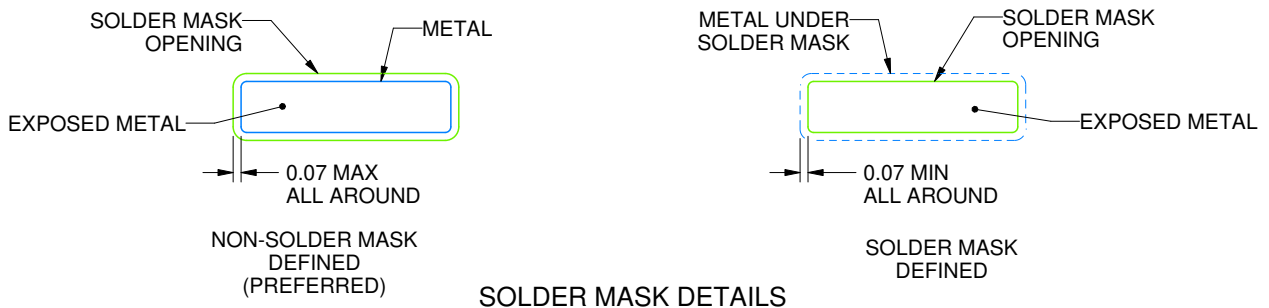5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)
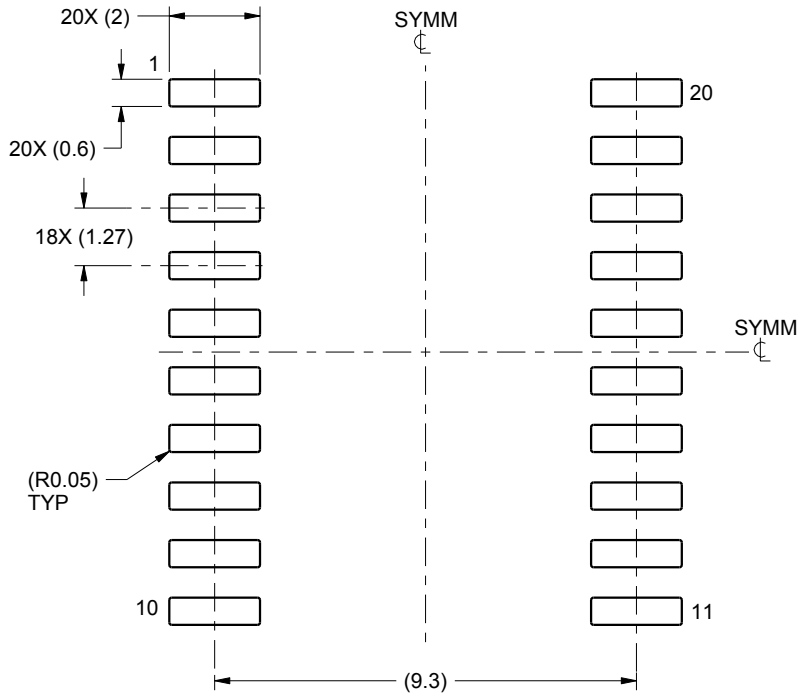
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
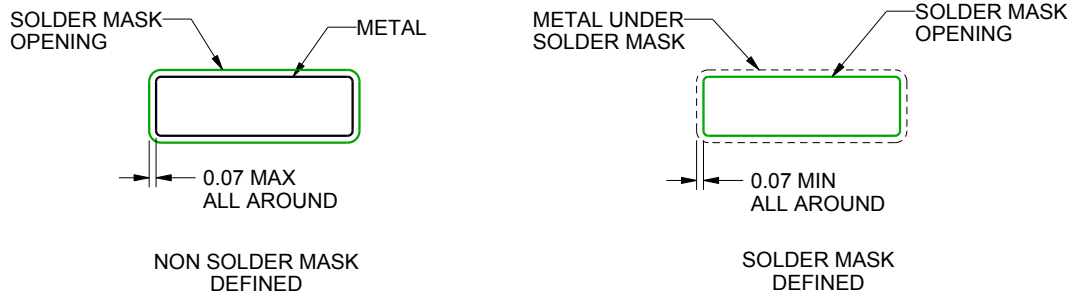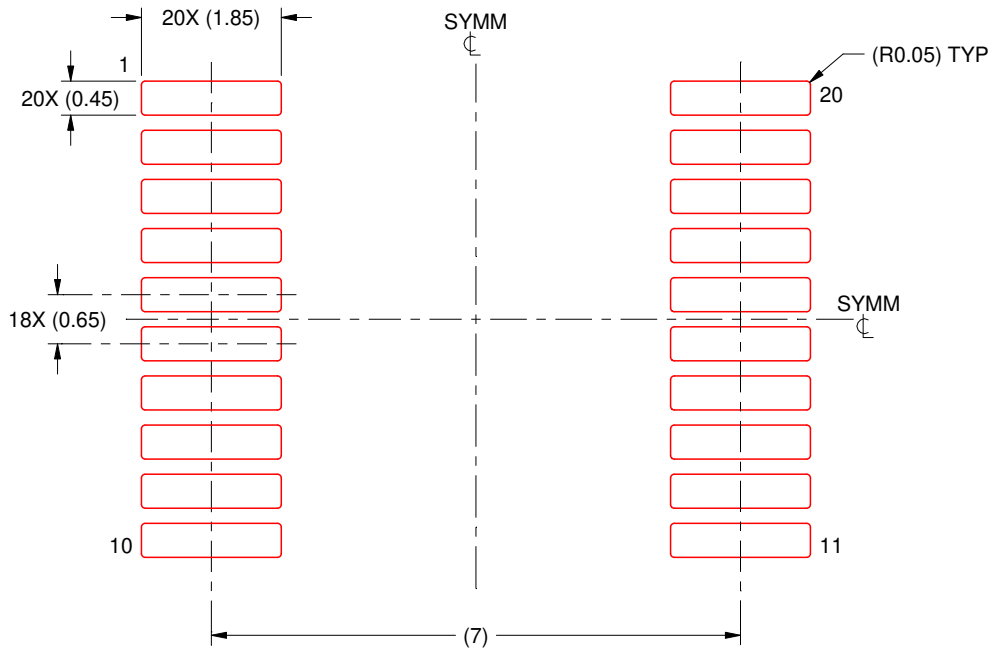
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)
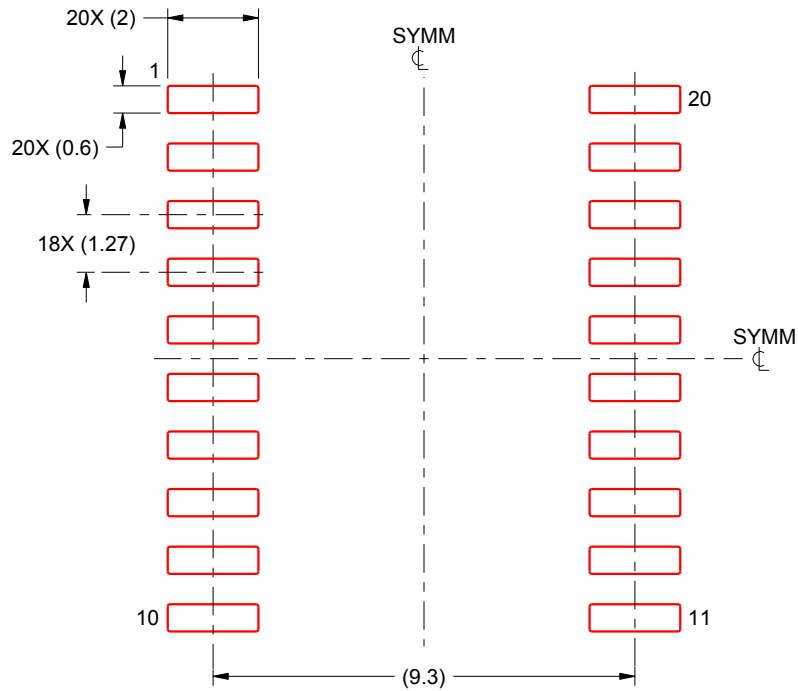
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

18X 0.65

1

20

7.5 / 6.9 NOTE 3

2X 5.85

10

11

B

5.6 / 5.0 NOTE 4

20X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

C

◯ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95 / 0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4214851/B   08/2019
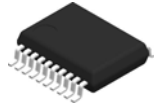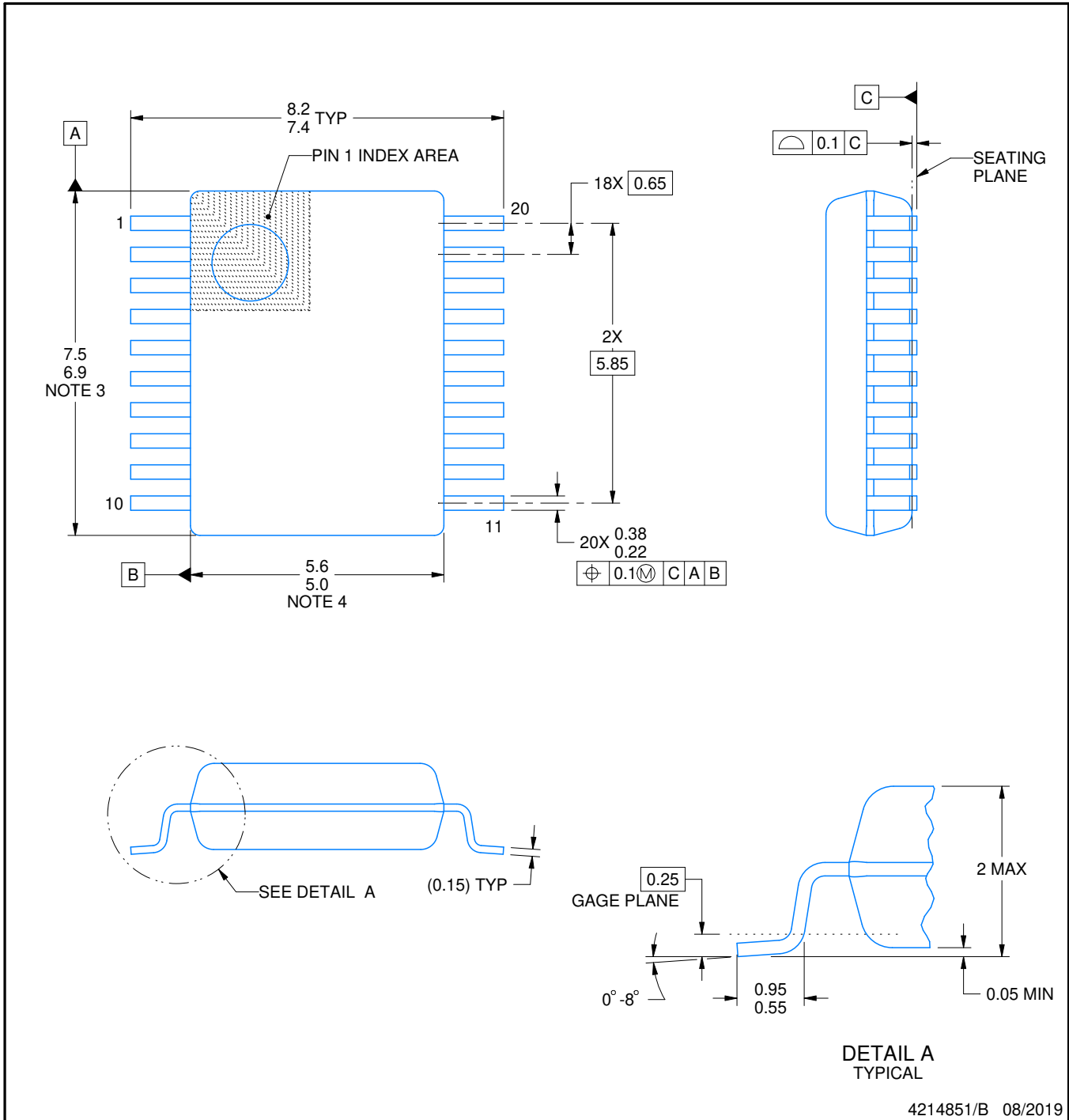
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

20X (1.85)

1

20X (0.45)

18X (0.65)

SYMM

(R0.05) TYP

20

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.