

# EPC2204 – Enhancement Mode Power Transistor

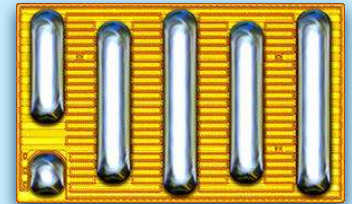
 $V_{DS}, 100\text{ V}$ 
 $R_{DS(on)}, 6\text{ m}\Omega$ 
 $I_D, 29\text{ A}$ 


Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$  while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

### Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

### Questions:



Die Size: 2.5 x 1.5 mm

**EPC2204 eGaN® FETs are supplied only in passivated die form with solder bars.**

### Applications

- DC-DC Converters
- Isolated DC-DC Converters
- Lidar
- Sync rectification for AC-DC and DC-DC
- Point of Load Converters
- USB-C
- Class-D Audio
- LED Lighting
- eMobility

### Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low  $Q_G$
- Small Footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2204>

### Maximum Ratings

PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	29	A
	Pulsed (25°C, $T_{PULSE} = 300\ \mu\text{s}$ )	125	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	

### Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

### Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.25\text{ mA}$	100			V
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$		0.04	0.2	mA
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.01	1.3	
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$		0.3	6.7	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.03	0.2	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 4\text{ mA}$	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 16\text{ A}$		4.4	6	mΩ
$V_{SD}$	Source-Drain Forward Voltage <sup>#</sup>	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		1.6		V

<sup>#</sup> Defined by design. Not subject to production test.

Dynamic Characteristics# (T<sub>j</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		644	851	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			2.3		
C <sub>OSS</sub>	Output Capacitance			304	456	
C <sub>OSS(ER)</sub>	Effective Output Capacitance, Energy Related (Note 2)	V <sub>DS</sub> = 0 to 50 V, V <sub>GS</sub> = 0 V		401		
C <sub>OSS(TR)</sub>	Effective Output Capacitance, Time Related (Note 3)			501		
R <sub>G</sub>	Gate Resistance			0.4		Ω
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 16 A		5.7	7.4	nC
Q <sub>GS</sub>	Gate-to-Source Charge	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 16 A		1.8		
Q <sub>GD</sub>	Gate-to-Drain Charge			0.8		
Q <sub>G(TH)</sub>	Gate Charge at Threshold			1		
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		25	38	
Q <sub>RR</sub>	Source-Drain Recovery Charge			0		

# Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: C<sub>OSS(ER)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Note 3: C<sub>OSS(TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Figure 1: Typical Output Characteristics at 25°C

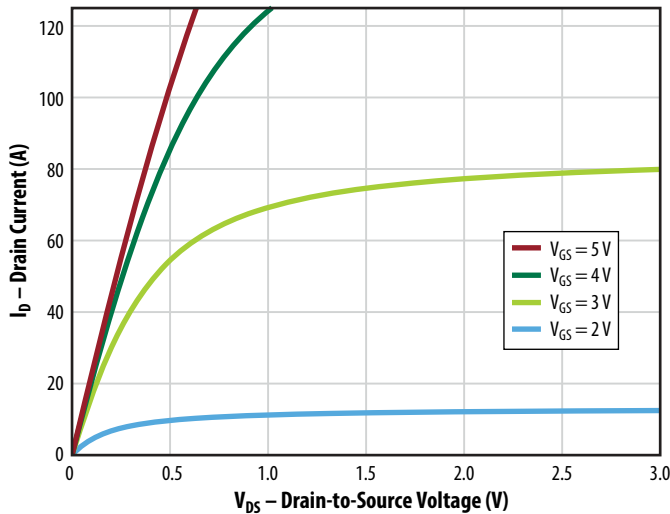


Figure 2: Typical Transfer Characteristics

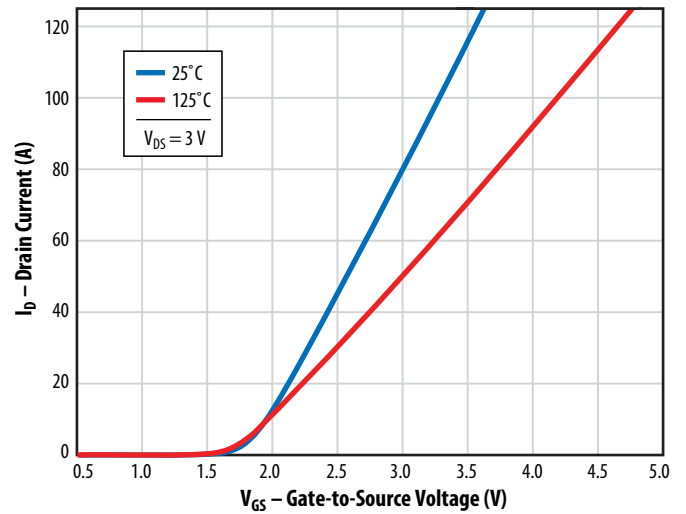


Figure 3: R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Drain Currents

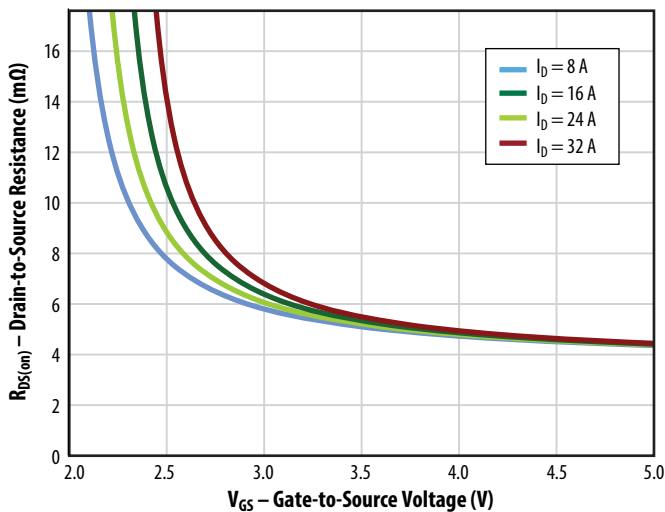


Figure 4: Typical R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Temperatures

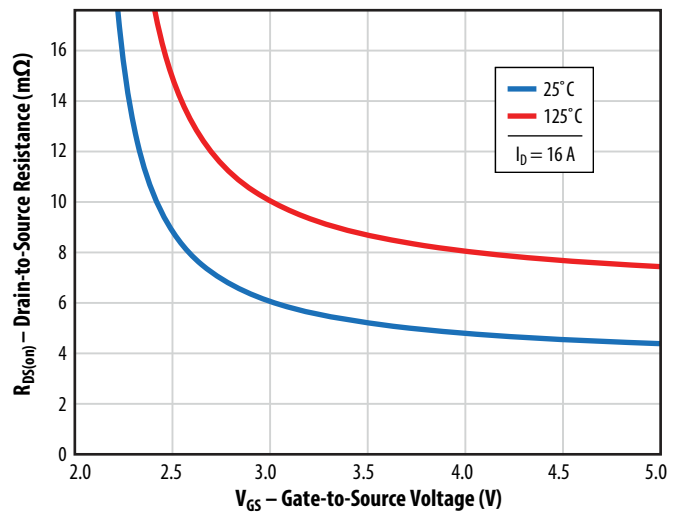


Figure 5a: Typical Capacitance (Linear Scale)

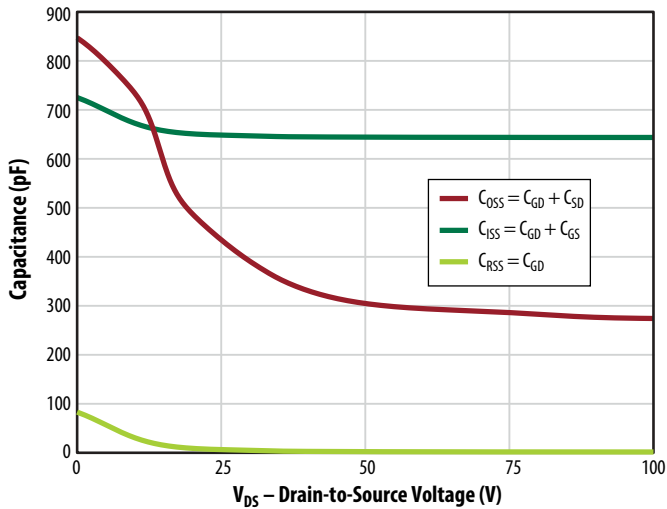


Figure 5b: Typical Capacitance (Log Scale)

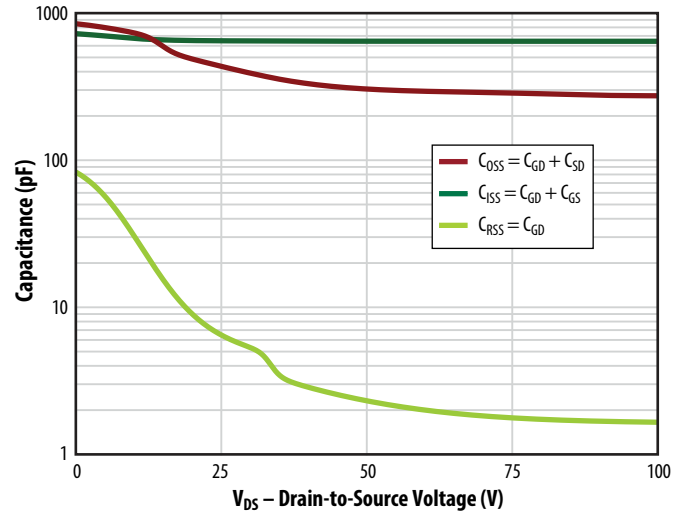


Figure 6: Typical Output Charge and  $C_{OSS}$  Stored Energy

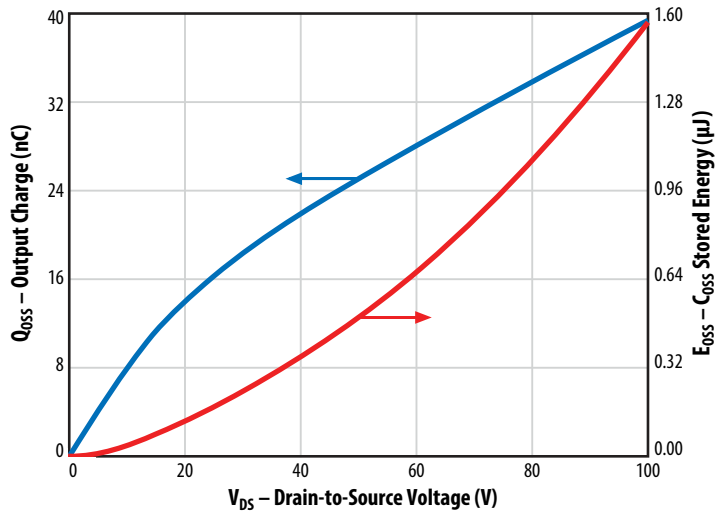


Figure 7: Typical Gate Charge

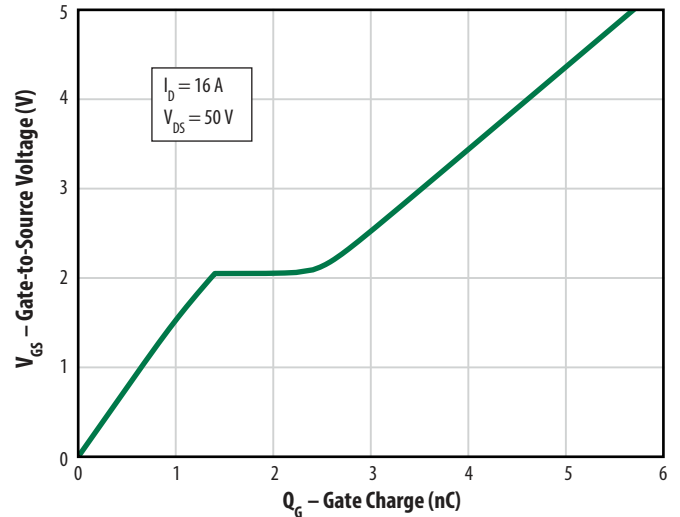


Figure 8: Reverse Drain-Source Characteristics

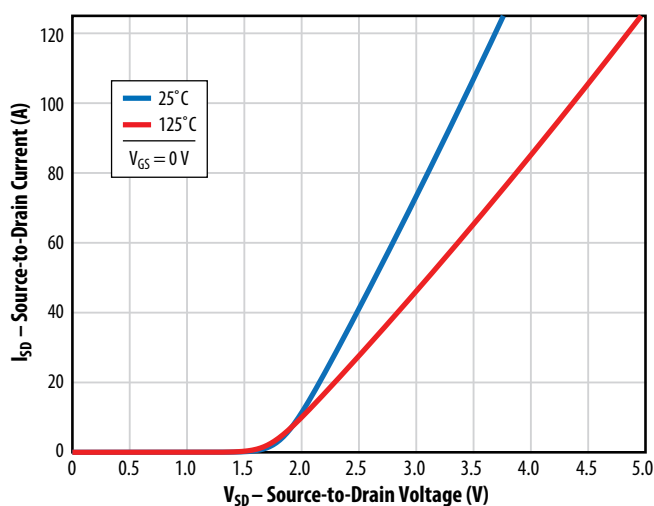
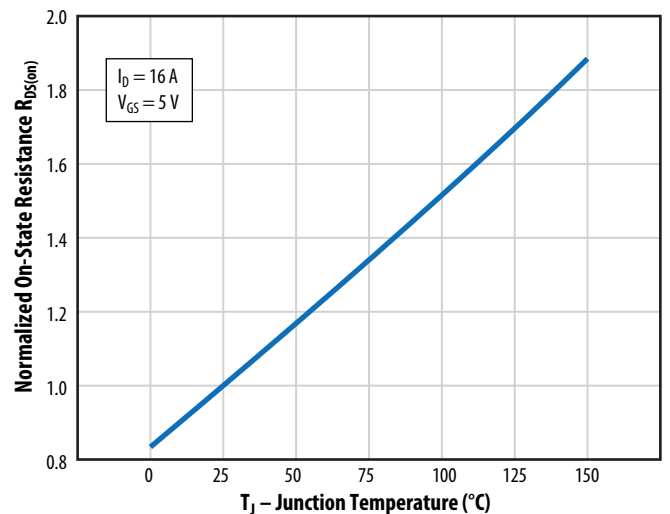


Figure 9: Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Normalized Threshold Voltage vs. Temperature

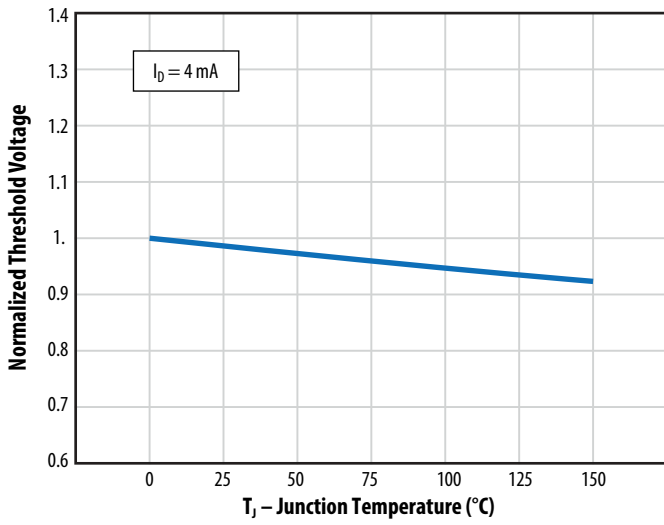


Figure 11: Safe Operating Area

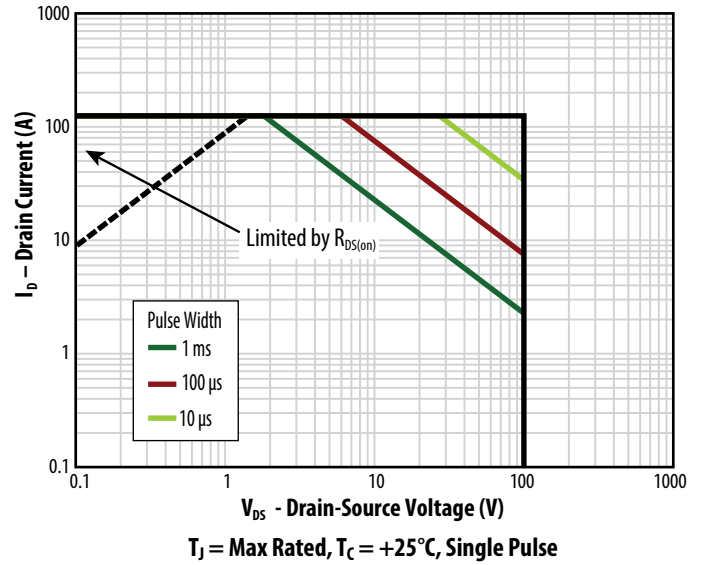
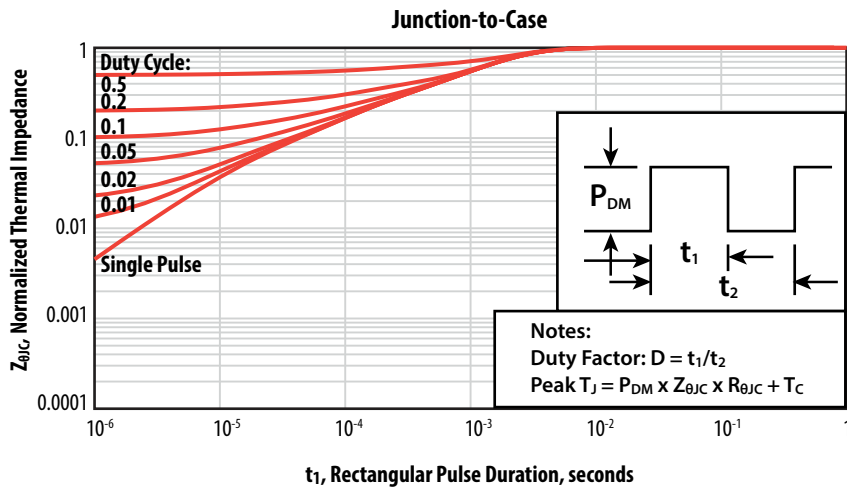
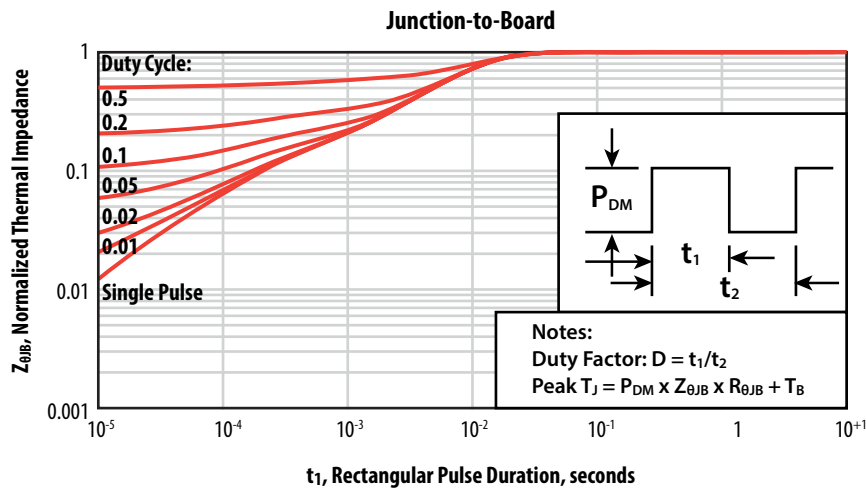
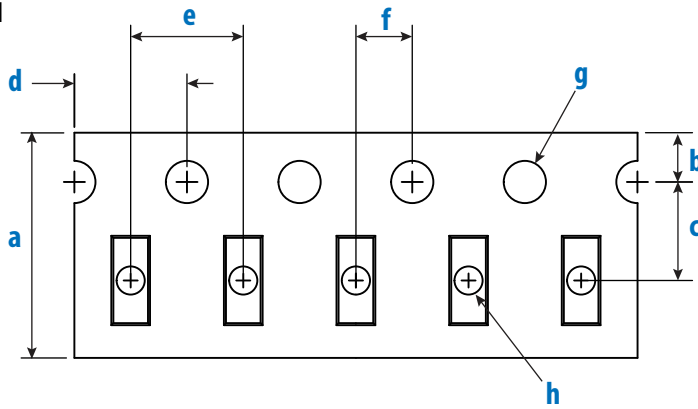
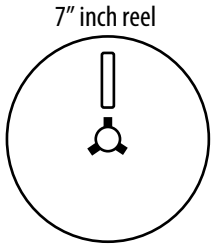


Figure 12: Transient Thermal Response Curves



**TAPE AND REEL CONFIGURATION**

4 mm pitch, 8 mm wide tape on 7" reel



Loaded Tape Feed Direction →



Die orientation dot  
Gate solder bar is under this corner

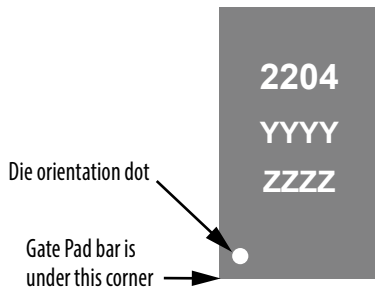
Die is placed into pocket solder bar side down (face side down)

EPC2204 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

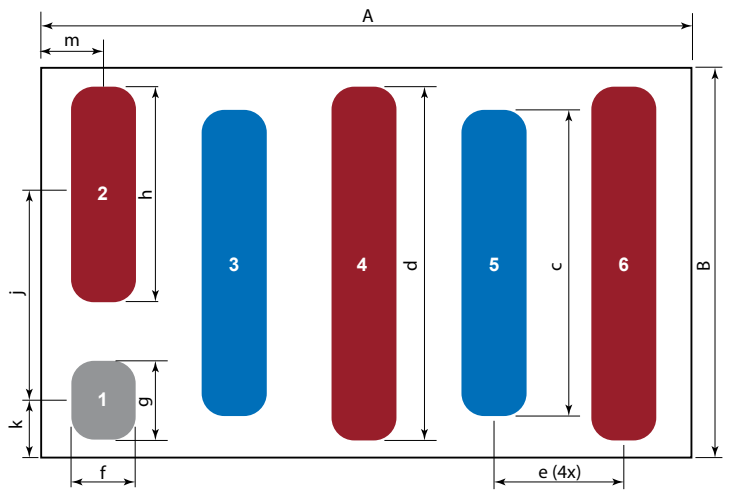
**DIE MARKINGS**



Part Number	Laser Markings		
	Part # Marking Line 1	Lot Date Code Marking Line 2	Lot Date Code Marking Line 3
EPC2204	2204	YYYY	ZZZZ

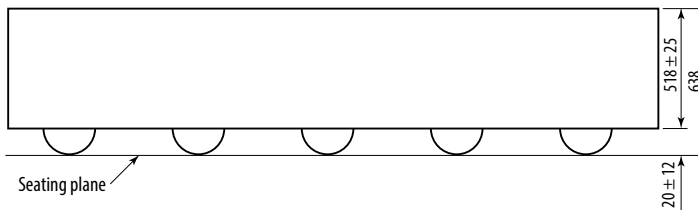
**DIE OUTLINE**

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c	1155	1175	1195
d	1330	1350	1370
e		500	
f	230	250	270
g	280	300	320
h	805	825	845
j		787.5	
k		225	
m		250	

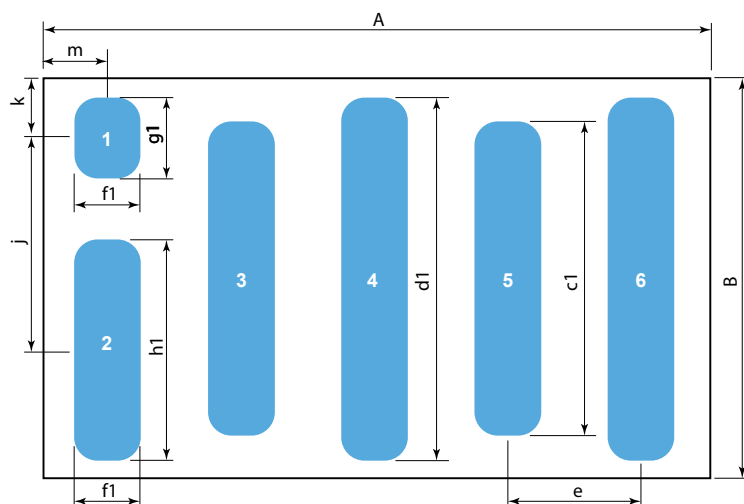
Side View



Pad 1 is Gate;  
Pads 2, 4, 6 are Source;  
Pads 3, 5 are Drain

Note: Dimensions d and c are centered

**RECOMMENDED LAND PATTERN**  
(units in  $\mu\text{m}$ )

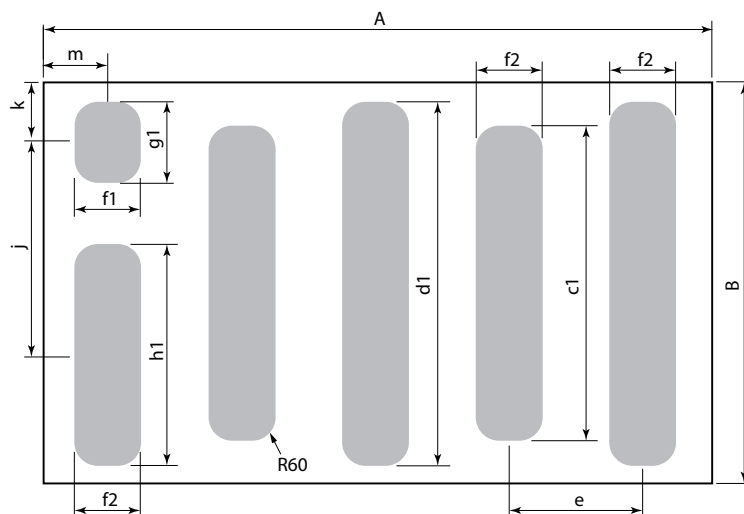


Land pattern is solder mask defined

DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5
k	225
m	250

Pad 1 is Gate;  
Pads 2, 4, 6 are Source;  
Pads 3, 5 are Drain

**RECOMMENDED STENCIL DRAWING**  
(units in  $\mu\text{m}$ )



DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
f2	210
g1	280
h1	805
j	787.5
k	225
m	250

Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at <https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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