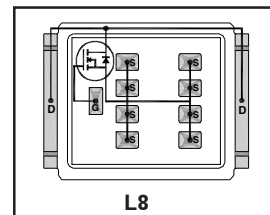


- RoHS Compliant, Halogen Free ①
- Lead-Free (Qualified up to 260°C Reflow)
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①
- Industrial Qualified

DirectFET™ Power MOSFET ②
Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	R_{DS(on)}
75V min	±20V max	1.8mΩ @ 10V
Q_{g tot}	Q_{gd}	V_{gs(th)}
200nC	62nC	3.0V



Applicable DirectFET Outline and Substrate Outline ①

SB	SC		M2	M4	L4	L6	L8
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Description

The IRF7759L2TR/TR1PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has a footprint smaller than a D²PAK and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems.

The IRF7759L2TR/TR1PbF is optimized for high frequency switching and synchronous rectification applications. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance power converters.

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF7759L2TRPbF	DirectFET2 Large Can	Tape and Reel	4000	"TR" suffix
IRF7759L2TR1PbF	DirectFET2 Large Can	Tape and Reel	1000	"TR1" suffix EOL notice # 264

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	75	V
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)④	160	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)④	113	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)③	26	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited) ④	375	
I _{DM}	Pulsed Drain Current ⑤	640	
E _{AS}	Single Pulse Avalanche Energy ⑥	257	mJ
I _{AR}	Avalanche Current ⑤	96	A

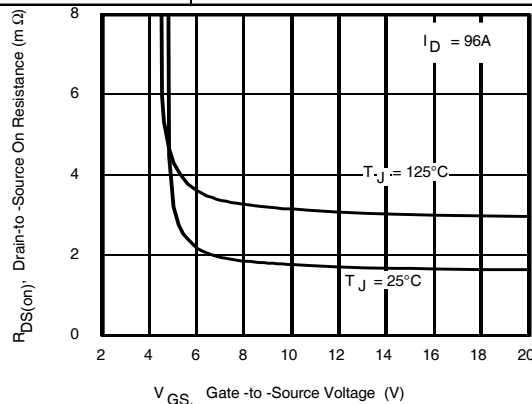


Fig 1. Typical On-Resistance vs. Gate Voltage

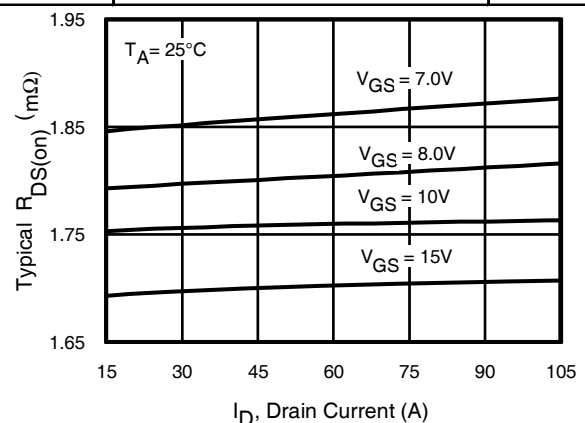


Fig 2. Typical On-Resistance vs. Drain Current

Notes:

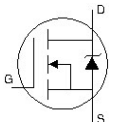
- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④ T_C measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting T_J = 25°C, L = 0.056mH, R_G = 25Ω, I_{AS} = 96A.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 2\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.8	2.3	m Ω	$V_{GS} = 10V, I_D = 96A$ ⑦
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	74	—	—	S	$V_{DS} = 25V, I_D = 96A$
Q_g	Total Gate Charge	—	200	300	nC	$V_{DS} = 38V$ $V_{GS} = 10V$ $I_D = 96A$ See Fig. 9
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	37	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	11	—		
Q_{gd}	Gate-to-Drain Charge	—	62	93		
Q_{godr}	Gate Charge Overdrive	—	91	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	73	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	60	—		
R_G	Gate Resistance	—	1.1	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 38V, V_{GS} = 10V$ ⑦ $I_D = 96A$ $R_G = 1.8\Omega$
t_r	Rise Time	—	37	—		
$t_{d(off)}$	Turn-Off Delay Time	—	80	—		
t_f	Fall Time	—	33	—		
C_{iss}	Input Capacitance	—	12222	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 60V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	1465	—		
C_{riss}	Reverse Transfer Capacitance	—	609	—		
C_{oss}	Output Capacitance	—	7457	—		
C_{oss}	Output Capacitance	—	955	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	160	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	640		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 96A, V_{GS} = 0V$ ⑦
t_{rr}	Reverse Recovery Time	—	64	96	ns	$T_J = 25^\circ\text{C}, I_F = 96A, V_{DD} = 38V$
Q_{rr}	Reverse Recovery Charge	—	150	225	nC	$di/dt = 100A/\mu s$ ⑦

Notes:

⑤ Repetitive rating; pulse width limited by max. junction temperature.

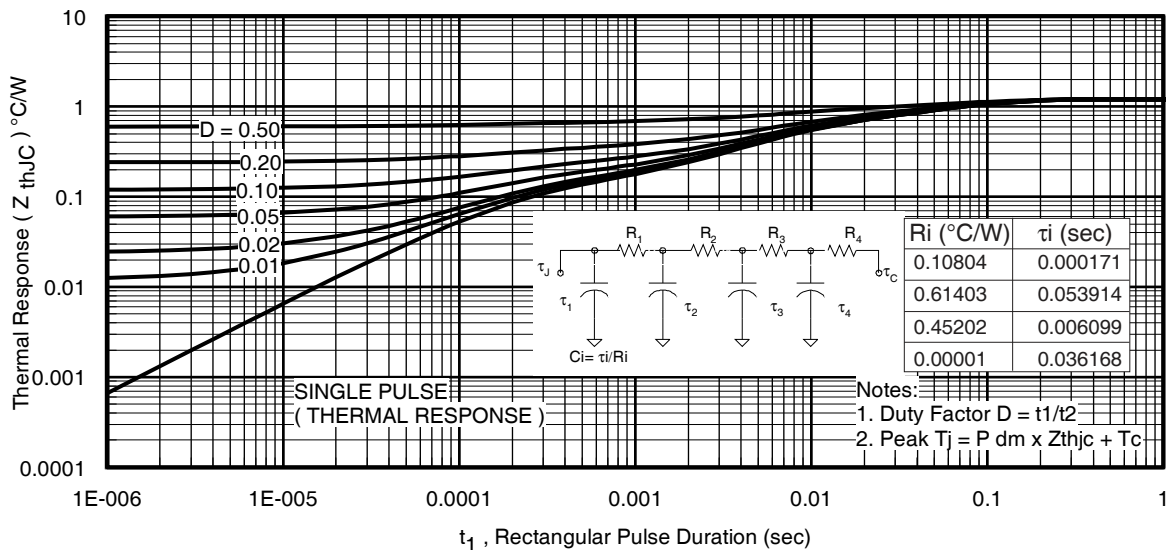
 ⑦ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

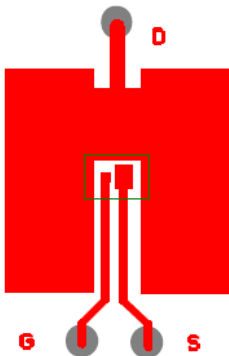
	Parameter	Max.	Units
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	125	W
$P_D @ T_C = 100^\circ\text{C}$	Power Dissipation ④	63	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ①	3.3	
T_P	Peak Soldering Temperature	270	°C
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		

Thermal Resistance

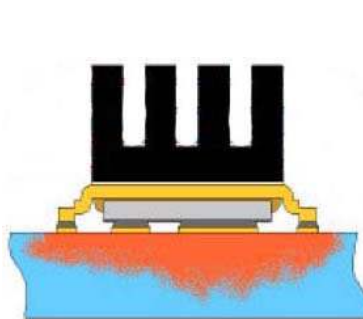
	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ③	20	—	
$R_{\theta J-Can}$	Junction-to-Can ③⑩	—	1.2	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	—	0.5	


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case ④
Notes:

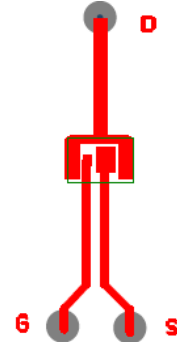
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④ T_C measured with thermocouple incontact with top (Drain) of part.
- ⑤ Used double sided cooling, mounting pad with large heatsink.
- ⑥ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑦ R_{θ} is measured at T_J of approximately 90°C .



③ Surface mounted on 1 in. square Cu board (still air).



⑥ Mounted on minimum footprint full size board with metalized back and with small clip heatsink. (still air)



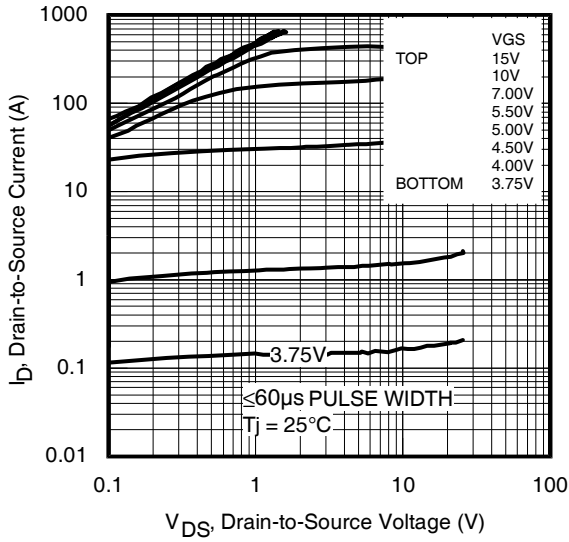


Fig 4. Typical Output Characteristics

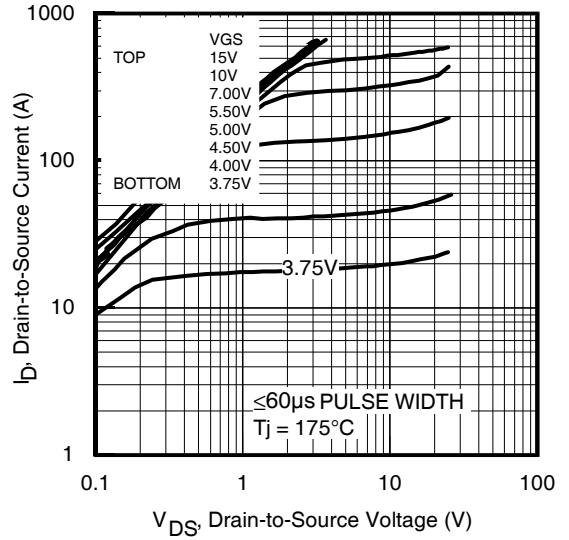


Fig 5. Typical Output Characteristics

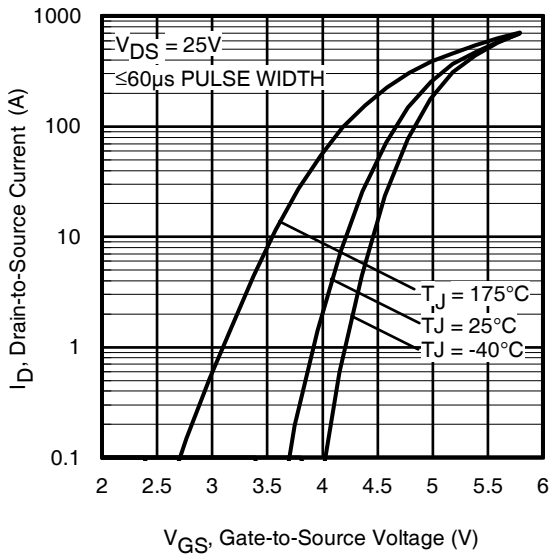


Fig 6. Typical Transfer Characteristics

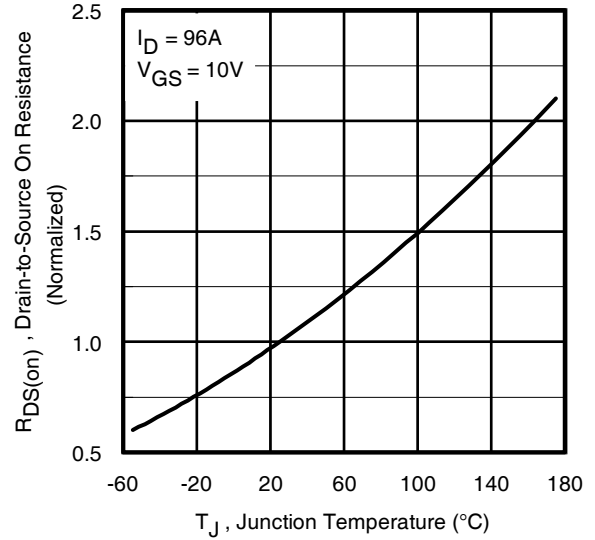


Fig 7. Normalized On-Resistance vs. Temperature

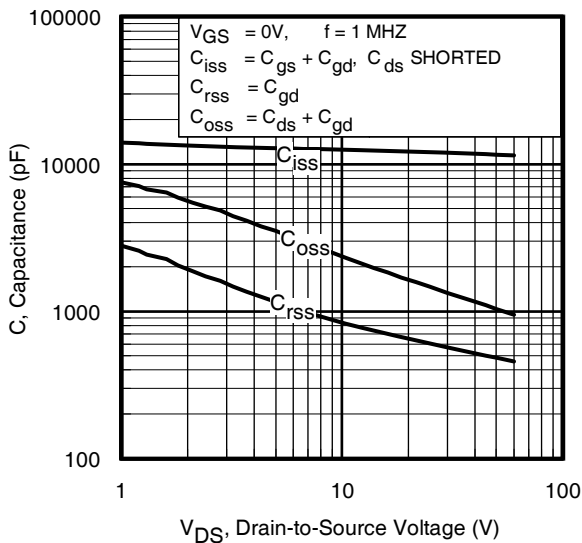


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

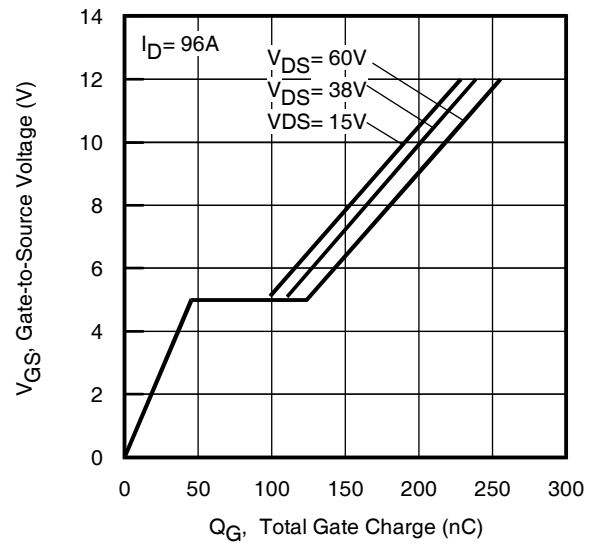


Fig 9. Typical Total Gate Charge vs. Gate-to-Source Voltage

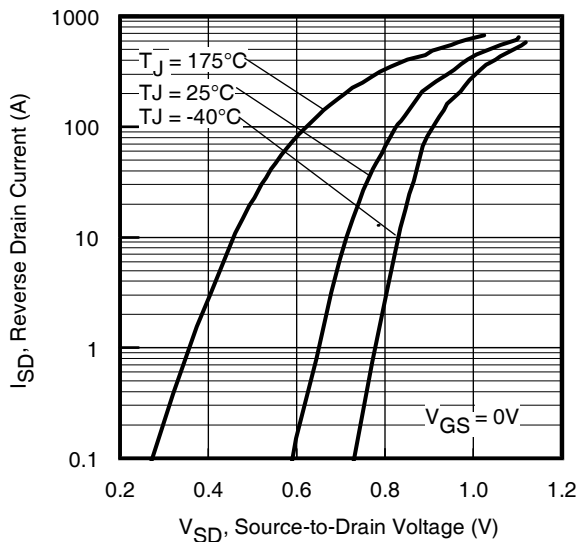


Fig 10. Typical Source-Drain Diode Forward Voltage

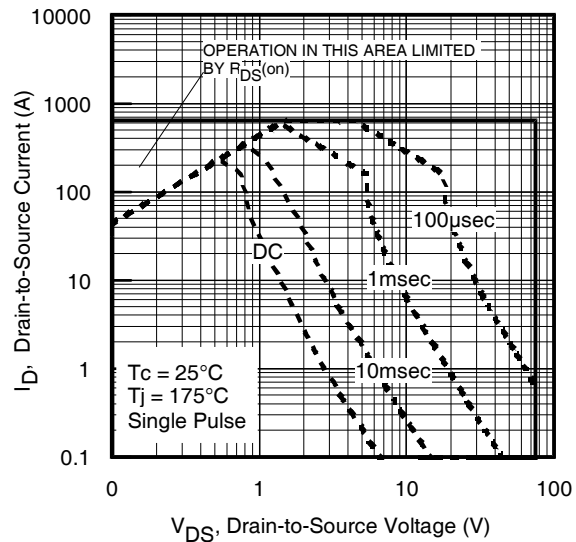


Fig11. Maximum Safe Operating Area

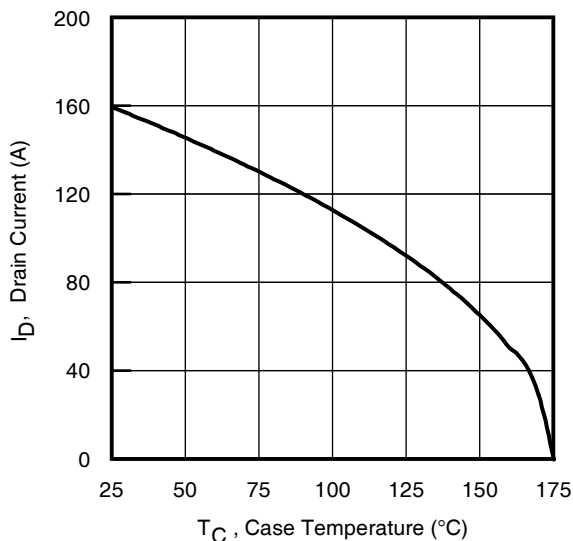


Fig 12. Maximum Drain Current vs. Case Temperature

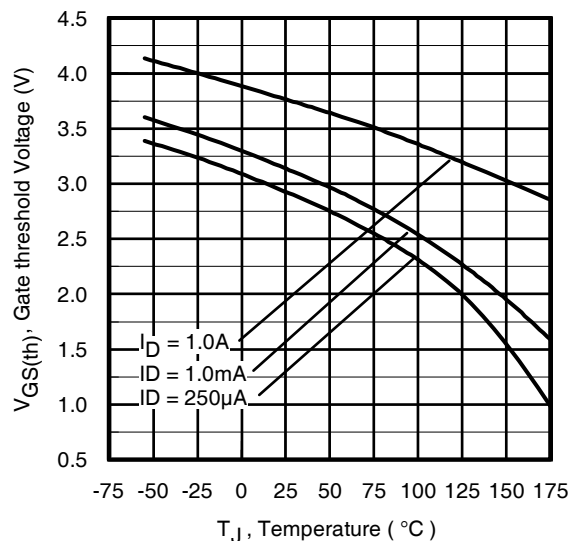


Fig 13. Typical Threshold Voltage vs. Junction Temperature

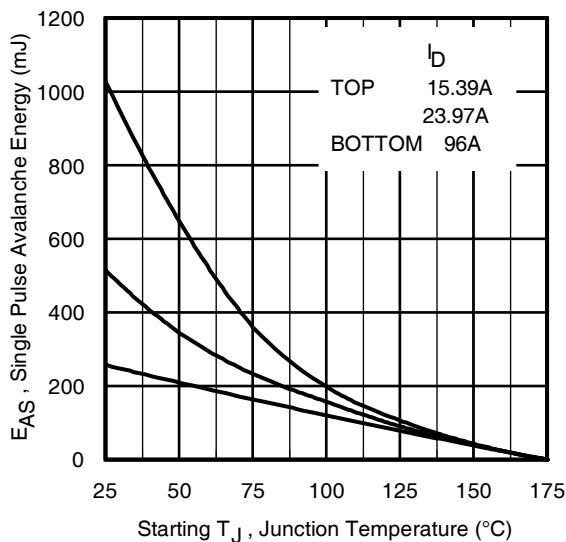


Fig 14. Maximum Avalanche Energy Vs. Drain Current

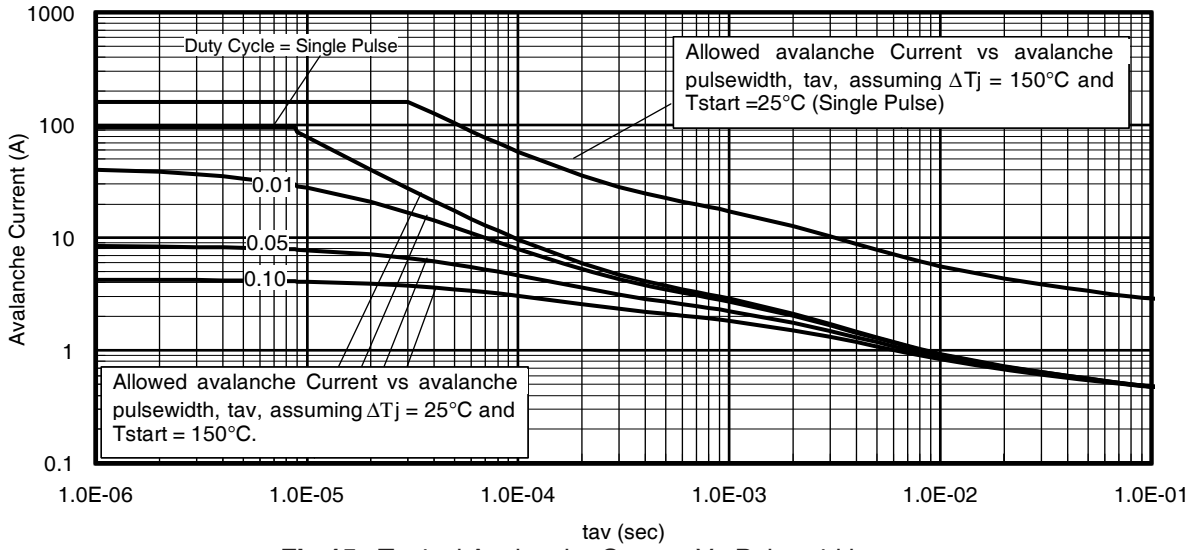


Fig 15. Typical Avalanche Current Vs.Pulsewidth

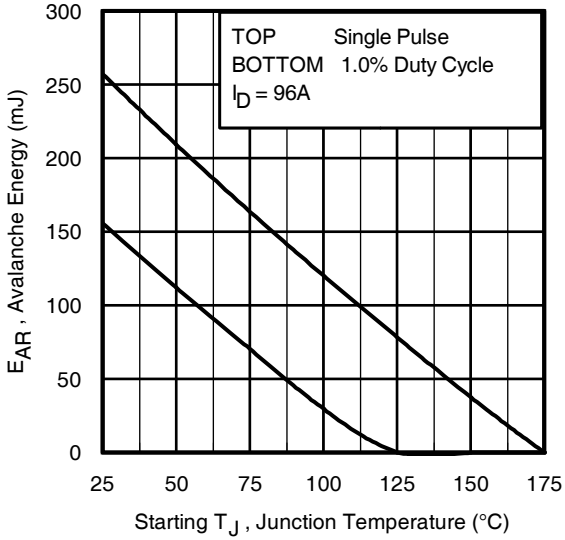


Fig 16. Maximum Avalanche Energy Vs. Temperature

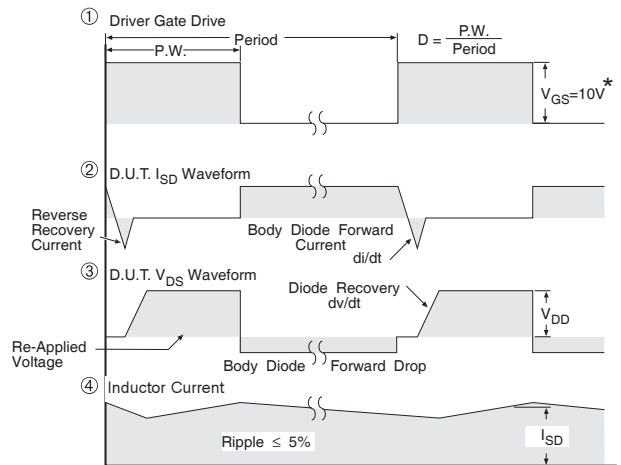
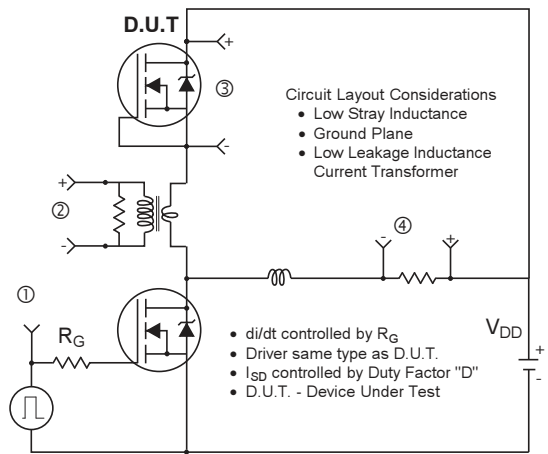
Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 19a, 19b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_a$$



* $V_{GS} = 5V$ for Logic Level Devices

Fig 17. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

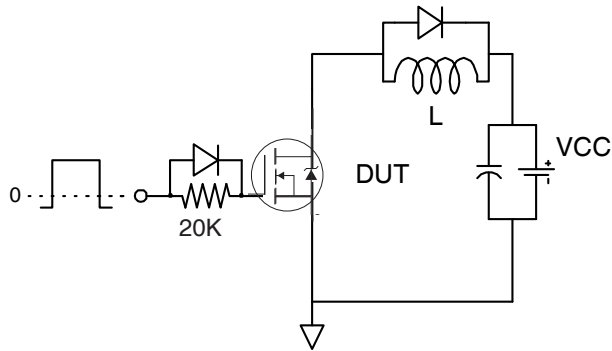


Fig 18a. Gate Charge Test Circuit

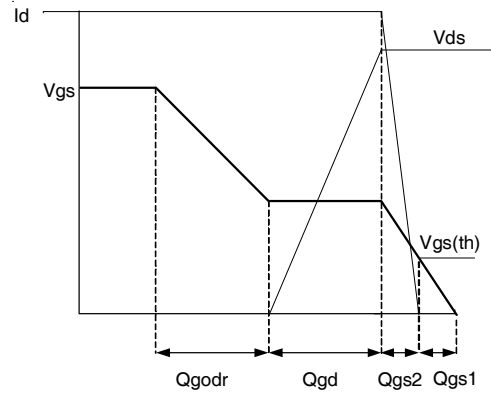


Fig 18b. Gate Charge Waveform

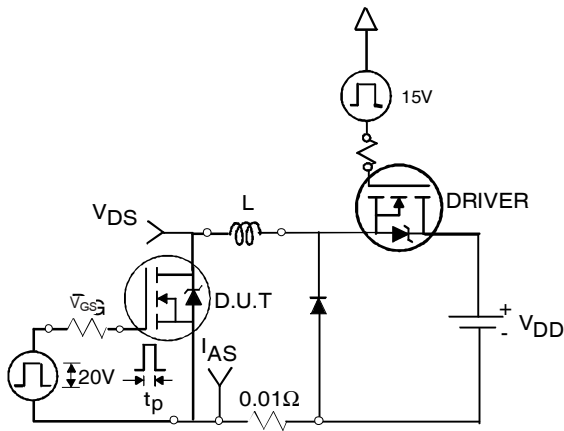


Fig 19a. Unclamped Inductive Test Circuit

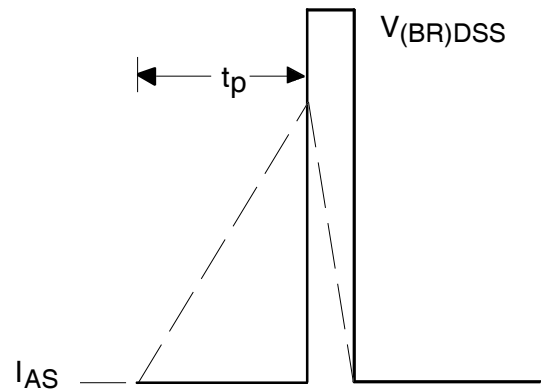


Fig 19b. Unclamped Inductive Waveforms

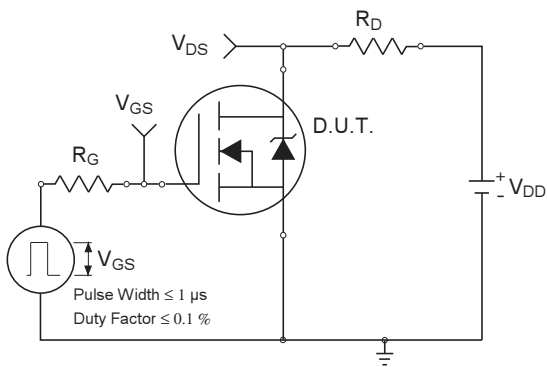


Fig 20a. Switching Time Test Circuit

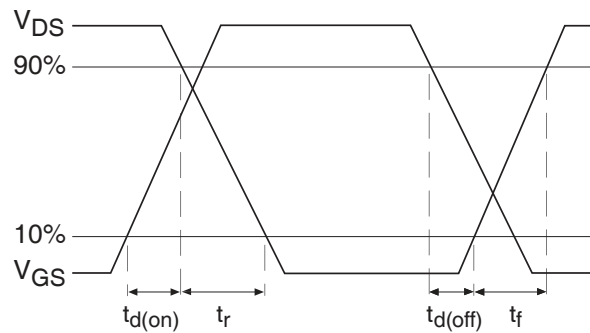
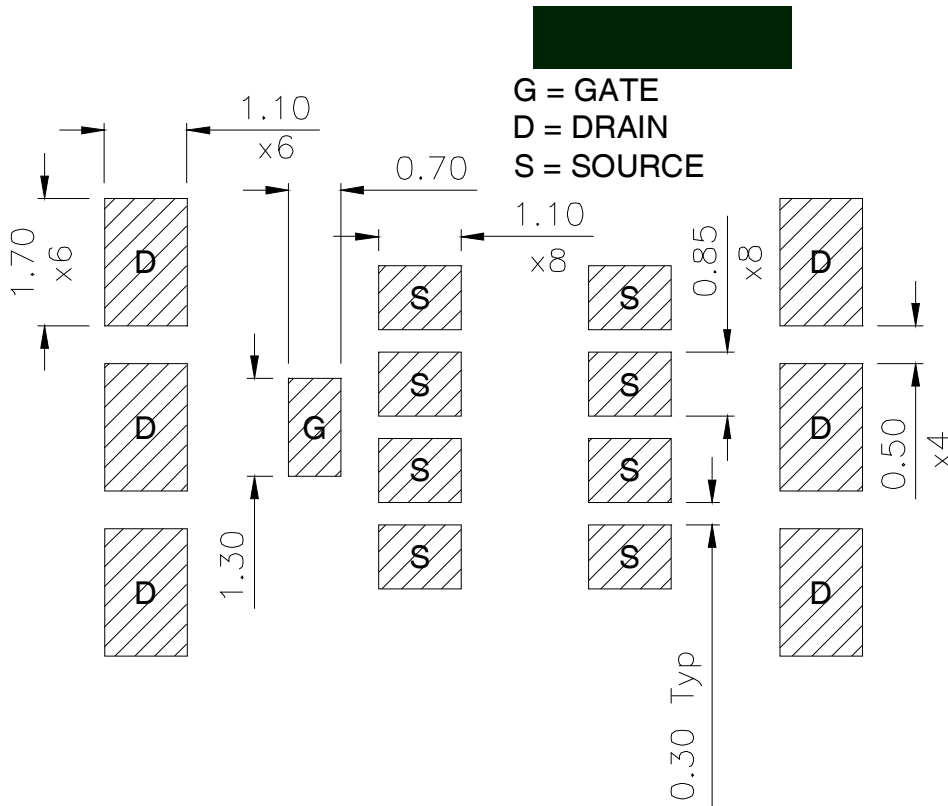
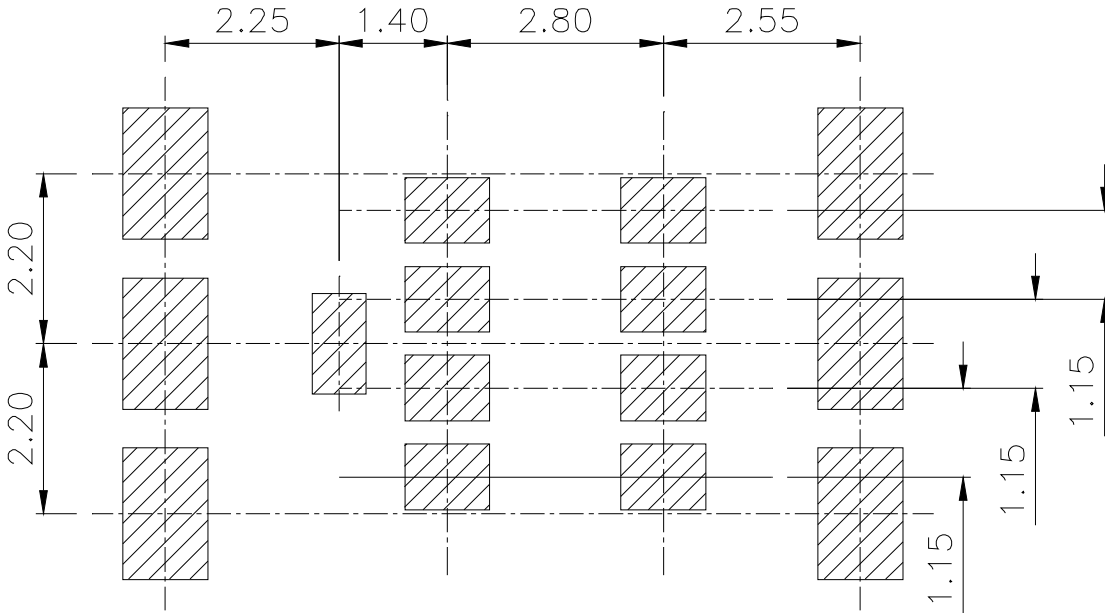


Fig 20b. Switching Time Waveforms

DirectFET™ Board Footprint, L8 (Large Size Can).

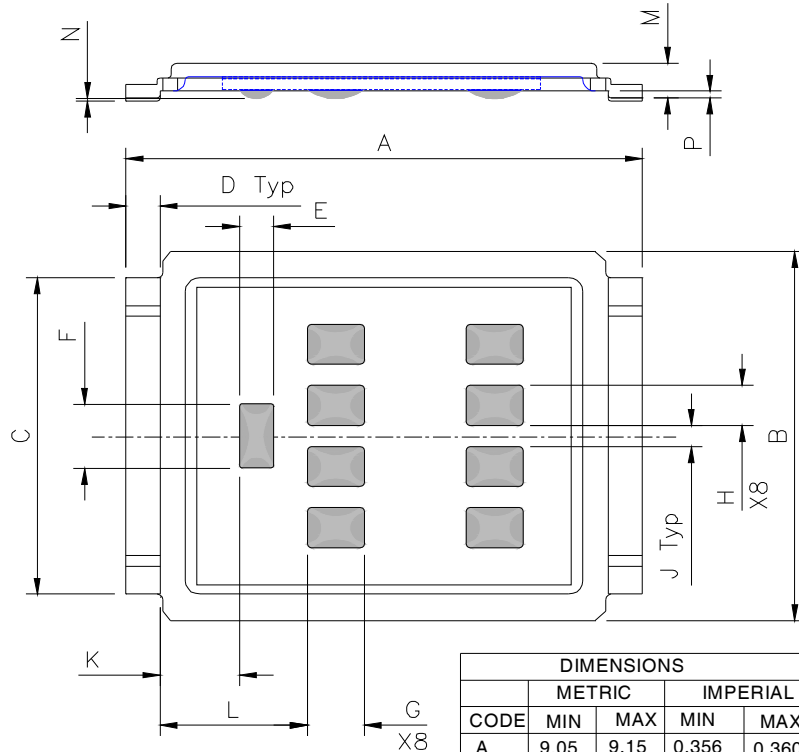
Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

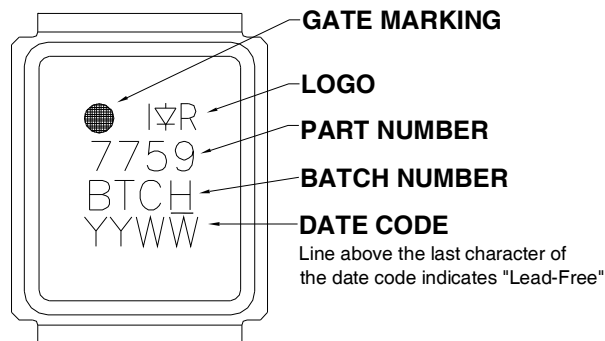
DirectFET™ Outline Dimension, L8 Outline (LargeSize Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations



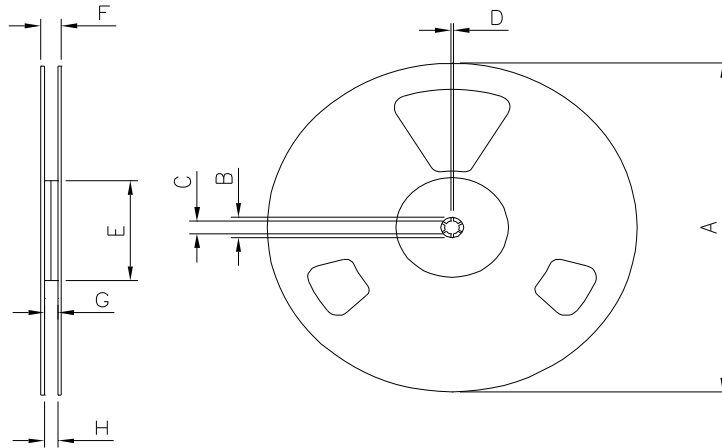
CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	9.05	9.15	0.356	0.360
B	6.85	7.10	0.270	0.280
C	5.90	6.00	0.232	0.236
D	0.55	0.65	0.022	0.026
E	0.58	0.62	0.023	0.024
F	1.18	1.22	0.046	0.048
G	0.98	1.02	0.015	0.017
H	0.73	0.77	0.029	0.030
J	0.38	0.42	0.015	0.017
K	1.34	1.47	0.053	0.058
L	2.52	2.69	0.099	0.106
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.09	0.18	0.003	0.007

DirectFET™ Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

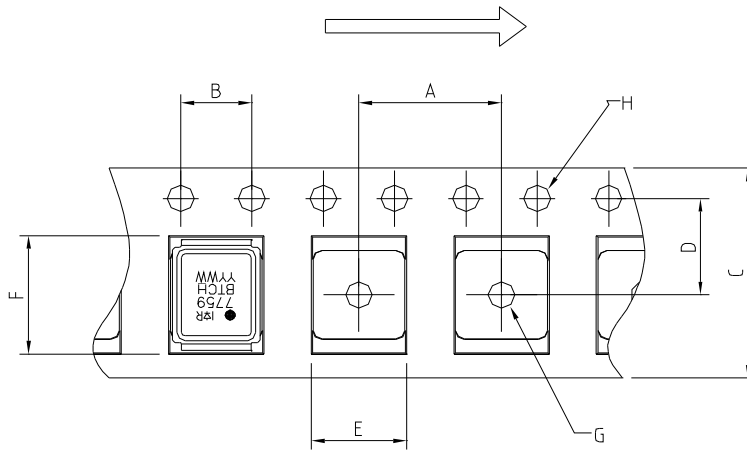
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4000 parts (ordered as IRF7759L2TR).

REEL DIMENSIONS				
STANDARD OPTION (QTY 4000)				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	330.00	N.C	12.992	N.C
B	20.20	N.C	0.795	N.C
C	12.80	13.20	0.504	0.520
D	1.50	N.C	0.059	N.C
E	99.00	100.00	3.900	3.940
F	N.C	22.40	N.C	0.880
G	16.40	18.40	0.650	0.720
H	15.90	19.40	0.630	0.760

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	11.90	12.10	0.469	0.476
B	3.90	4.10	0.154	0.161
C	15.90	16.30	0.626	0.642
D	7.40	7.60	0.291	0.299
E	7.20	7.40	0.284	0.291
F	9.90	10.10	0.390	0.398
G	1.50	NC	0.059	NC
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification Information[†]

Qualification level	Industrial ^{††}	
	(per JEDEC JESD47F ^{†††} guidelines)	
	Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level	DFET2	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.
 Please contact your International Rectifier sales representative for further information:
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
2/24/2014	<ul style="list-style-type: none"> • Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #264) • Updated data sheet with new IR corporate template

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