

**General Description**

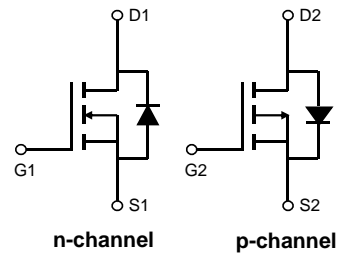
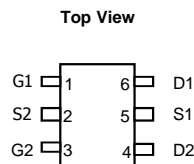
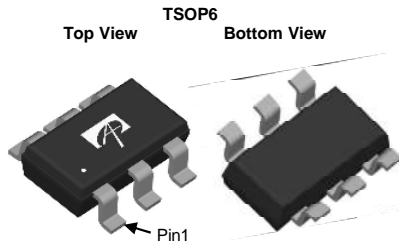
The AO6601 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications.

**Product Summary**
**N-Channel**

$V_{DS} = 30V$   
 $I_D = 3.4A$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 60m\Omega$  ( $V_{GS} = 10V$ )  
 $< 70m\Omega$  ( $V_{GS} = 4.5V$ )  
 $< 90m\Omega$  ( $V_{GS} = 2.5V$ )

**P-Channel**

$-30V$   
 $-2.3A$  ( $V_{GS} = -10V$ )  
 $R_{DS(ON)} < 115m\Omega$  ( $V_{GS} = -10V$ )  
 $< 150m\Omega$  ( $V_{GS} = -4.5V$ )  
 $< 200m\Omega$  ( $V_{GS} = -2.5V$ )


**Absolute Maximum Ratings  $T_A = 25^\circ C$  unless otherwise noted**

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 12$	V
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	-2.3	A
		$T_A = 70^\circ C$	-1.8	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	20	-15	
Power Dissipation <sup>B</sup>	$P_D$	$T_A = 25^\circ C$	1.15	W
		$T_A = 70^\circ C$	0.73	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	78	110	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	106	150
Maximum Junction-to-Lead	$R_{\theta JL}$	64	80	$^\circ C/W$

**N-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.5	1	1.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	20			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =3.4A T <sub>J</sub> =125°C		46 73	60 88	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A		50	70	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =2A		62	90	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =3.4A		14		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.75	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				1.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz	185	235	285	pF
C <sub>oss</sub>	Output Capacitance		25	35	45	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		10	18	25	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.9	1.8	2.7	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =3.4A		10	12	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge		4.7	6	nC	
Q <sub>gs</sub>	Gate Source Charge		0.95		nC	
Q <sub>gd</sub>	Gate Drain Charge		1.6		nC	
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =4.4Ω, R <sub>GEN</sub> =3Ω		3.5		ns
t <sub>r</sub>	Turn-On Rise Time		1.5		ns	
t <sub>D(off)</sub>	Turn-Off DelayTime		17.5		ns	
t <sub>f</sub>	Turn-Off Fall Time		2.5		ns	
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =3.4A, dI/dt=100A/μs		8.5	12	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =3.4A, dI/dt=100A/μs		2.55	4	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

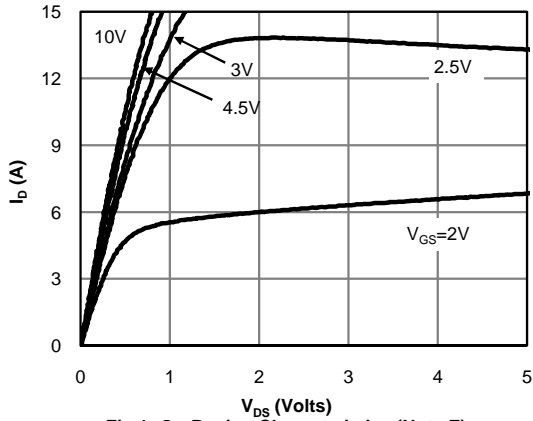
D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

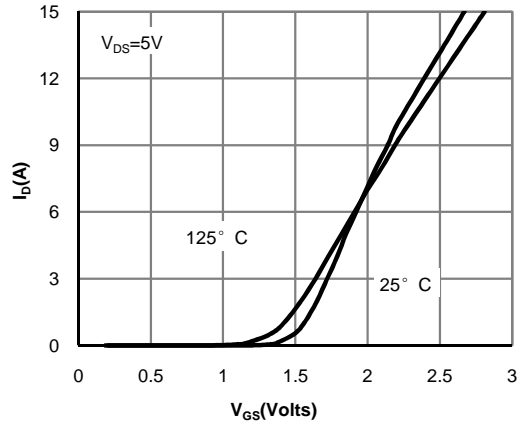
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

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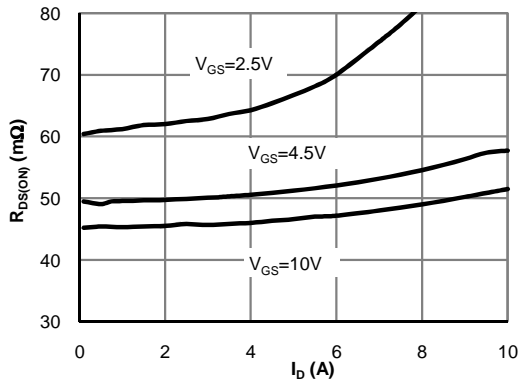
**N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



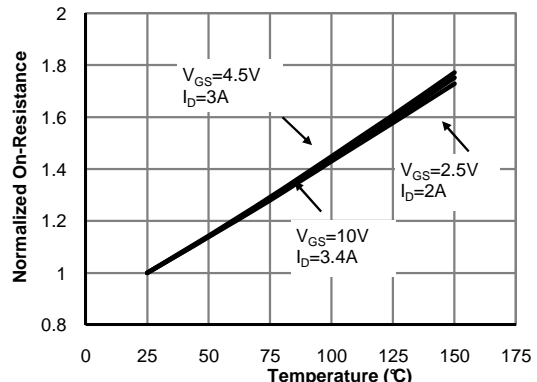
**Fig 1: On-Region Characteristics (Note E)**



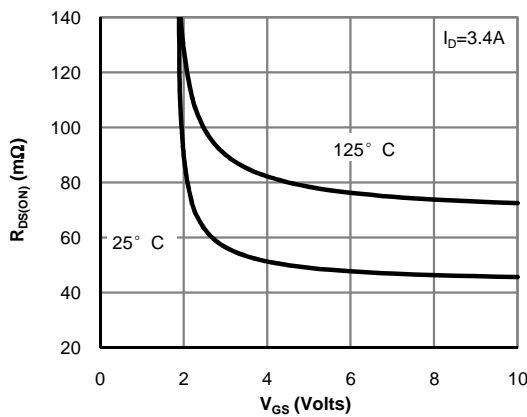
**Figure 2: Transfer Characteristics (Note E)**



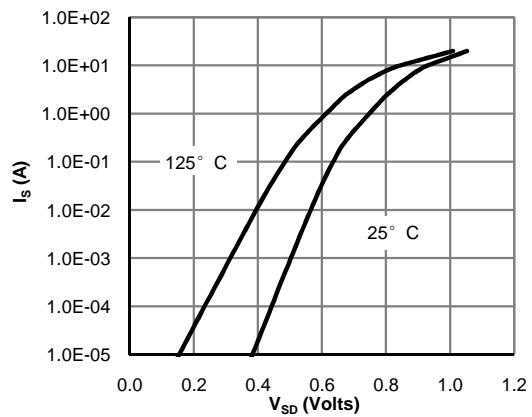
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

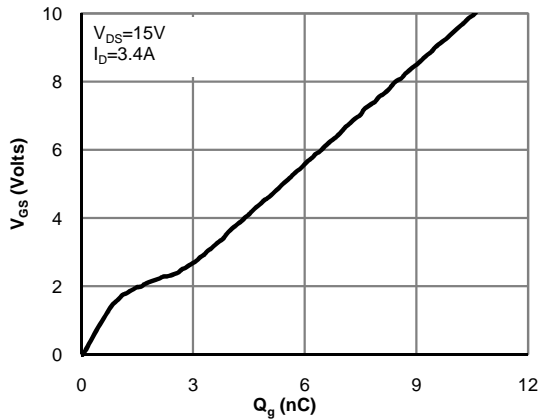


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

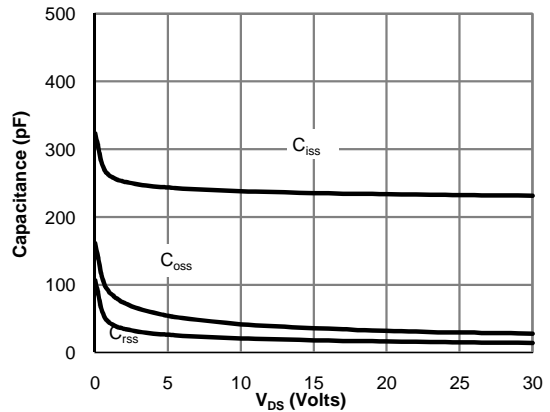


**Figure 6: Body-Diode Characteristics (Note E)**

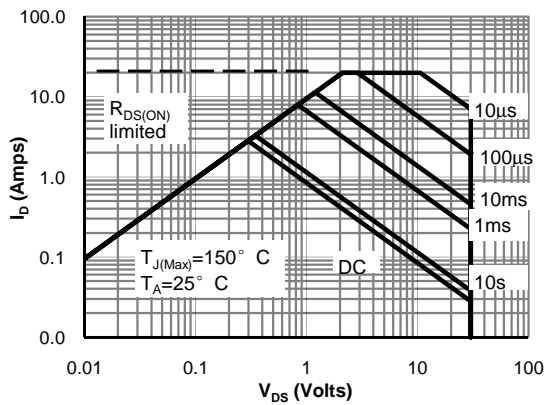
**N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



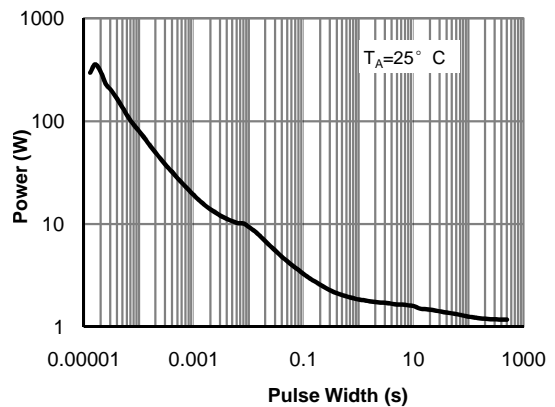
**Figure 7: Gate-Charge Characteristics**



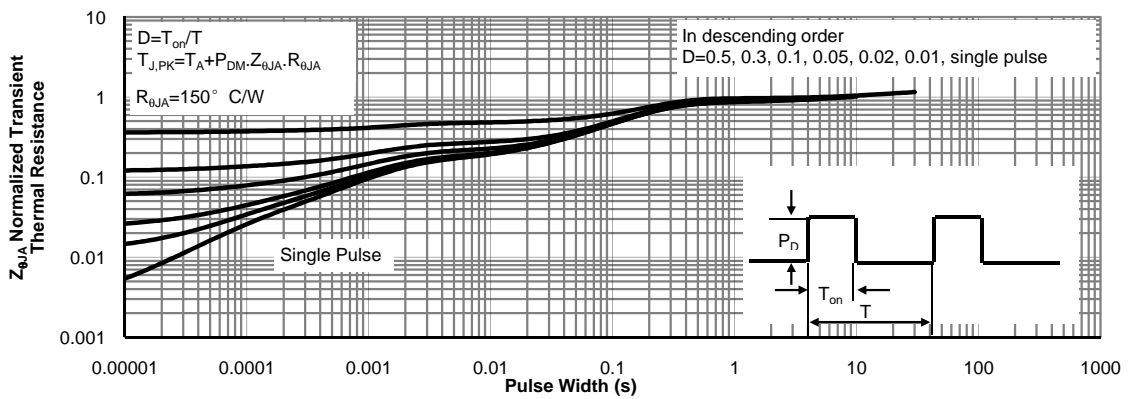
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

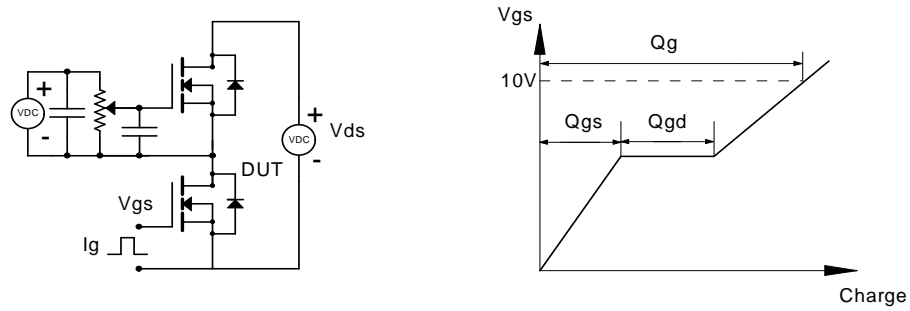


**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

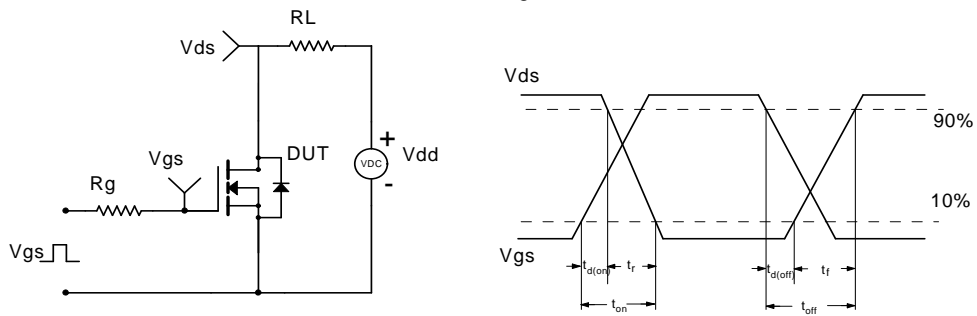


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

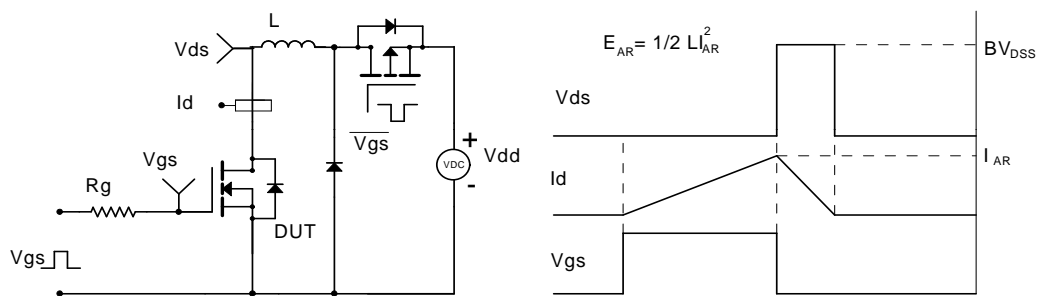
Gate Charge Test Circuit & Waveform



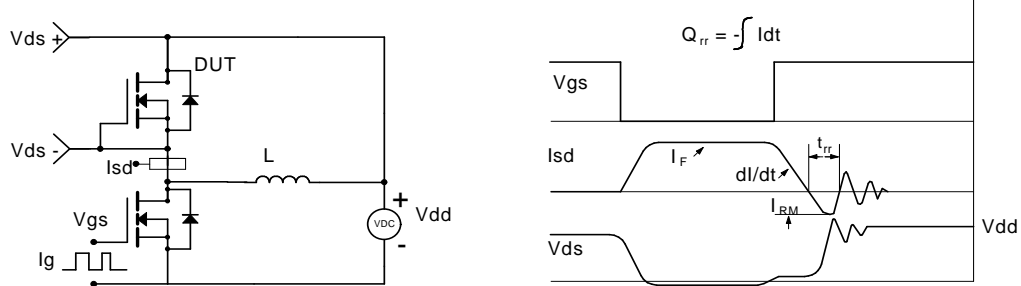
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



**P-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.6	-1	-1.4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-15			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-2.3A T <sub>J</sub> =125°C		88 143	115 200	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-2A		103	150	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-1A		139	200	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-2.3A		8		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.78	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-1.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz	205	260	315	pF
C <sub>oss</sub>	Output Capacitance		25	37	50	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		10	20	30	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	4	8	12	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-2.3A	4.5	5.9	7	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		2	2.8	4	nC
Q <sub>gs</sub>	Gate Source Charge			0.7		nC
Q <sub>gd</sub>	Gate Drain Charge			1		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =6Ω, R <sub>GEN</sub> =3Ω		6		ns
t <sub>r</sub>	Turn-On Rise Time			3.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			20		ns
t <sub>f</sub>	Turn-Off Fall Time			5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-2.3A, dI/dt=100A/μs		11.5	15	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-2.3A, dI/dt=100A/μs		4.5	6	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

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**P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

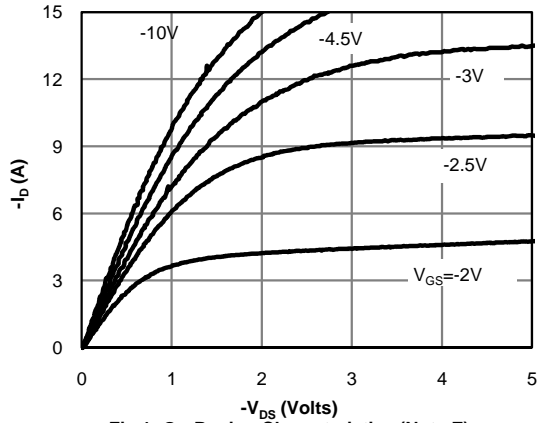


Fig 1: On-Region Characteristics (Note E)

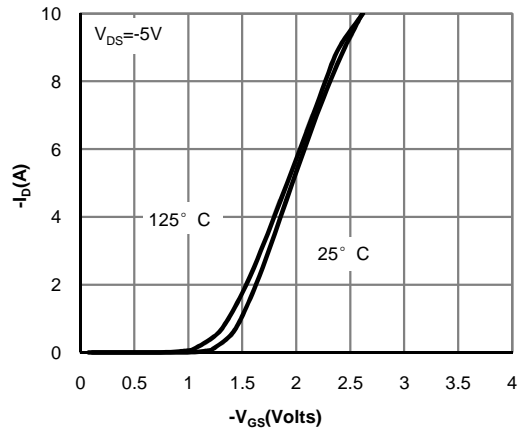


Figure 2: Transfer Characteristics (Note E)

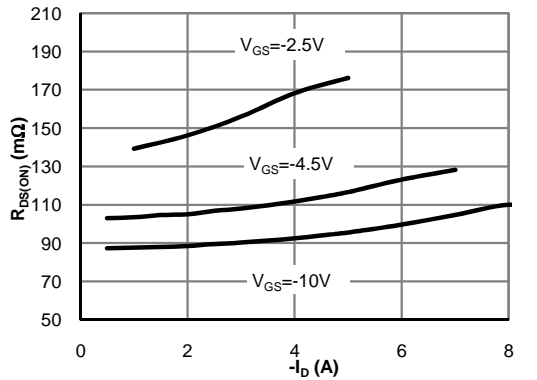


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

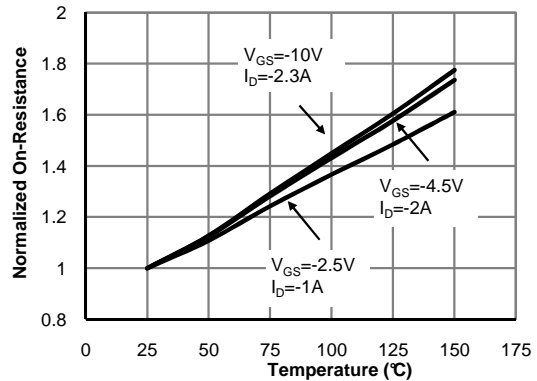


Figure 4: On-Resistance vs. Junction Temperature (Note E)

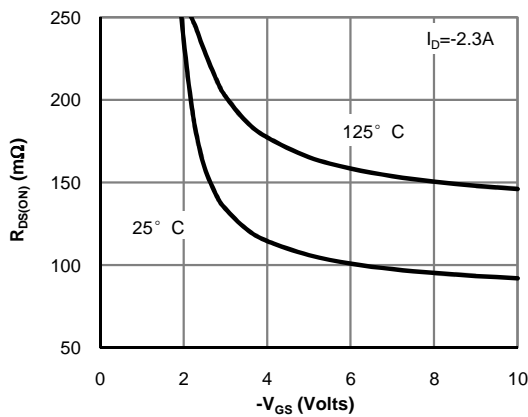


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

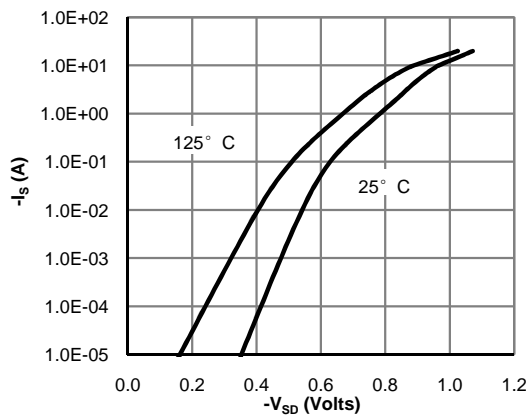


Figure 6: Body-Diode Characteristics (Note E)

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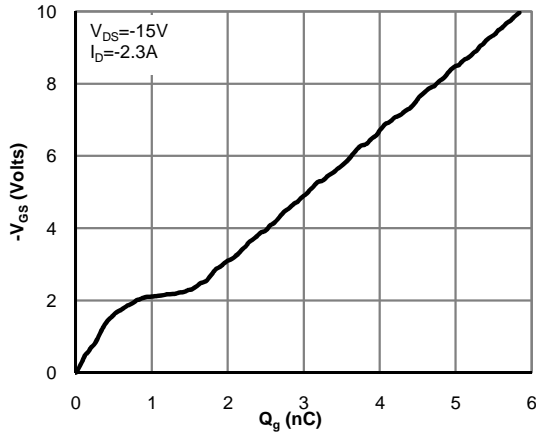


Figure 7: Gate-Charge Characteristics

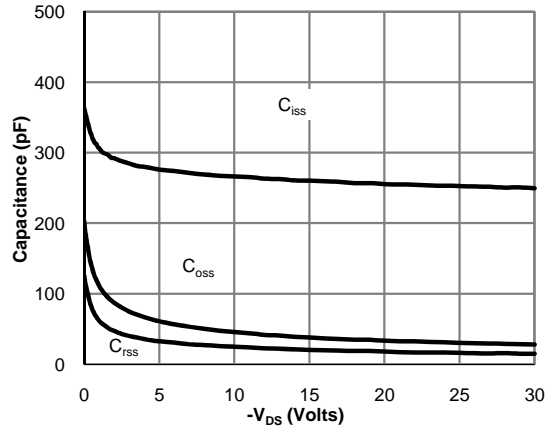


Figure 8: Capacitance Characteristics

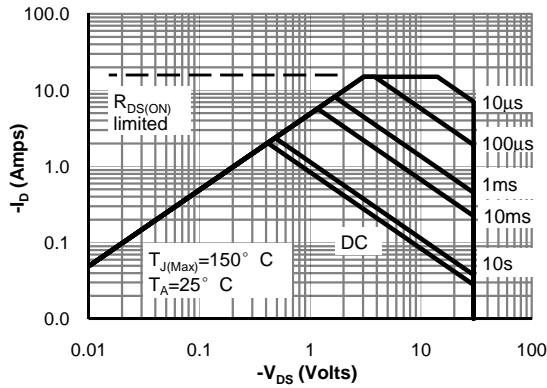


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

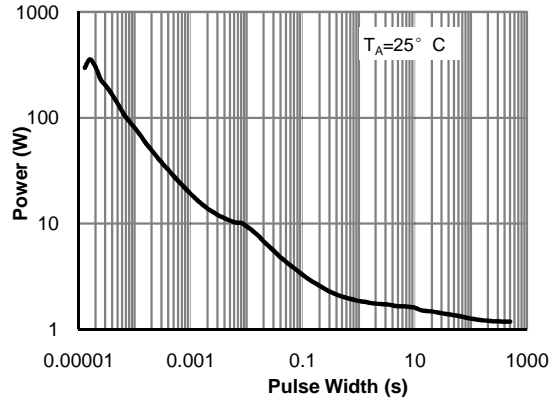


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

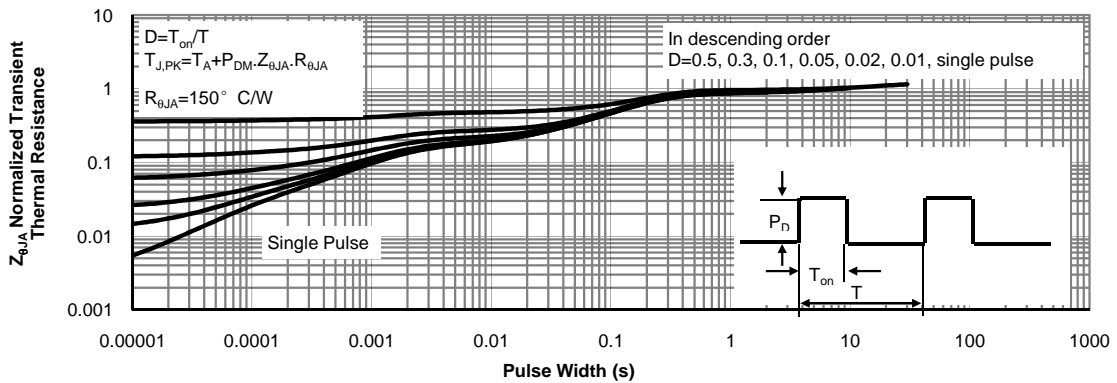
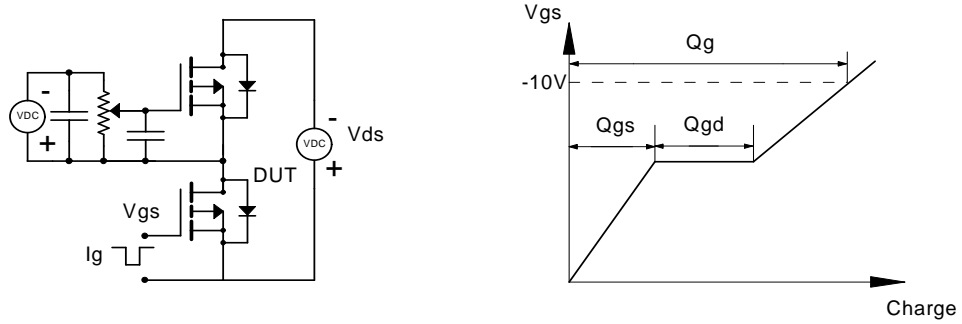


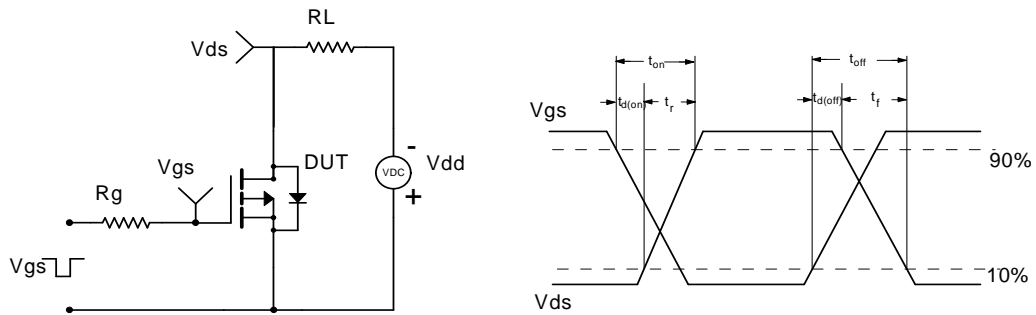
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



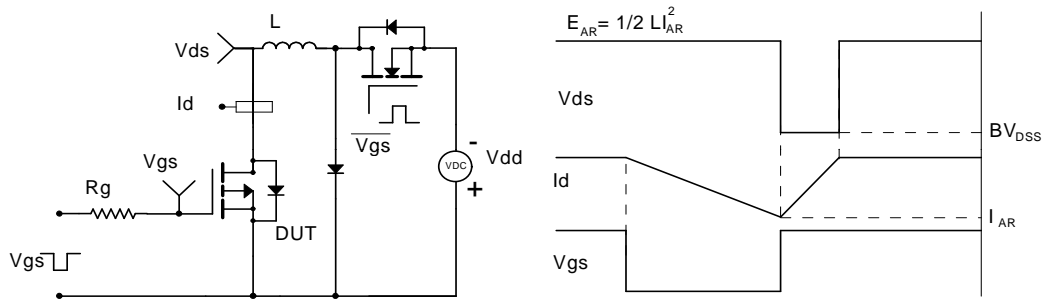
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

