NCP5604A, NCP5604B

High Efficiency White LED Driver

The NCP5604A and NCP5604B products are multiple output LED drivers dedicated to the display back light. The NCP5604A drives up to 4 LEDs, the NCP5604B version being dedicated to the three LED applications.

The two parts share a common built−in DC/DC converter, based on a charge pump structure, including the new 1.33X mode of operation, improving the efficiency over the full input battery supply voltage span over 90%.

Features

- 2.7 to 5.5 V Input Voltage Range
- Consistent 85% Efficiency
- 1.0 μA Quiescent Supply Current
- All Pins are Fully ESD Protected
- Built−in Short Circuit Protection
- Provides Four Independent LED Drives
- 200 kHz Digital Dimming Function
- Unloaded LED Protection
- Short Circuit Current Proof
- Tight 0.5% LED Current Matching
- These are Pb−Free Devices*

Typical Applications

- Portable Back Light
- Digital Cellular Phone Camera Photo Flash
- LCD and Key Board Simultaneously Drive

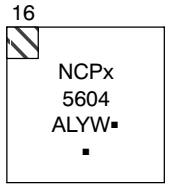
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

WQFN16 (3x3)
MT SUFFIX
CASE 488AK

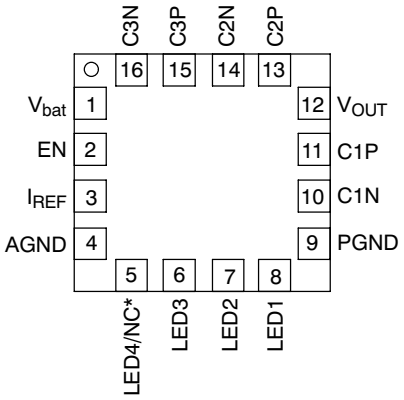
MARKING DIAGRAM



NCPx5604	= Specific Device Code x = A or B
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



* Pin 5 in not connected in the NCP5604B

(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5604AMTR2G	WQFN16 (Pb−Free)	3000/Tape & Reel
NCP5604BMTR2G	WQFN16 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

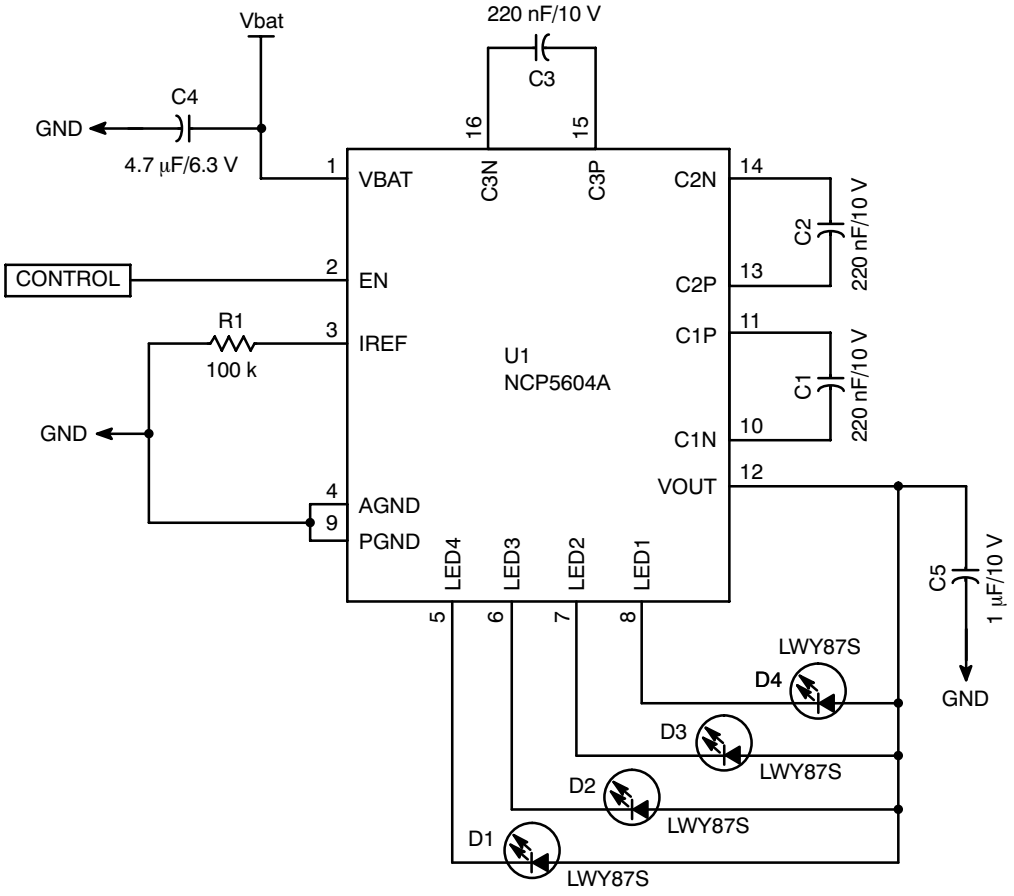


Figure 1. Typical Multiple White LED Driver

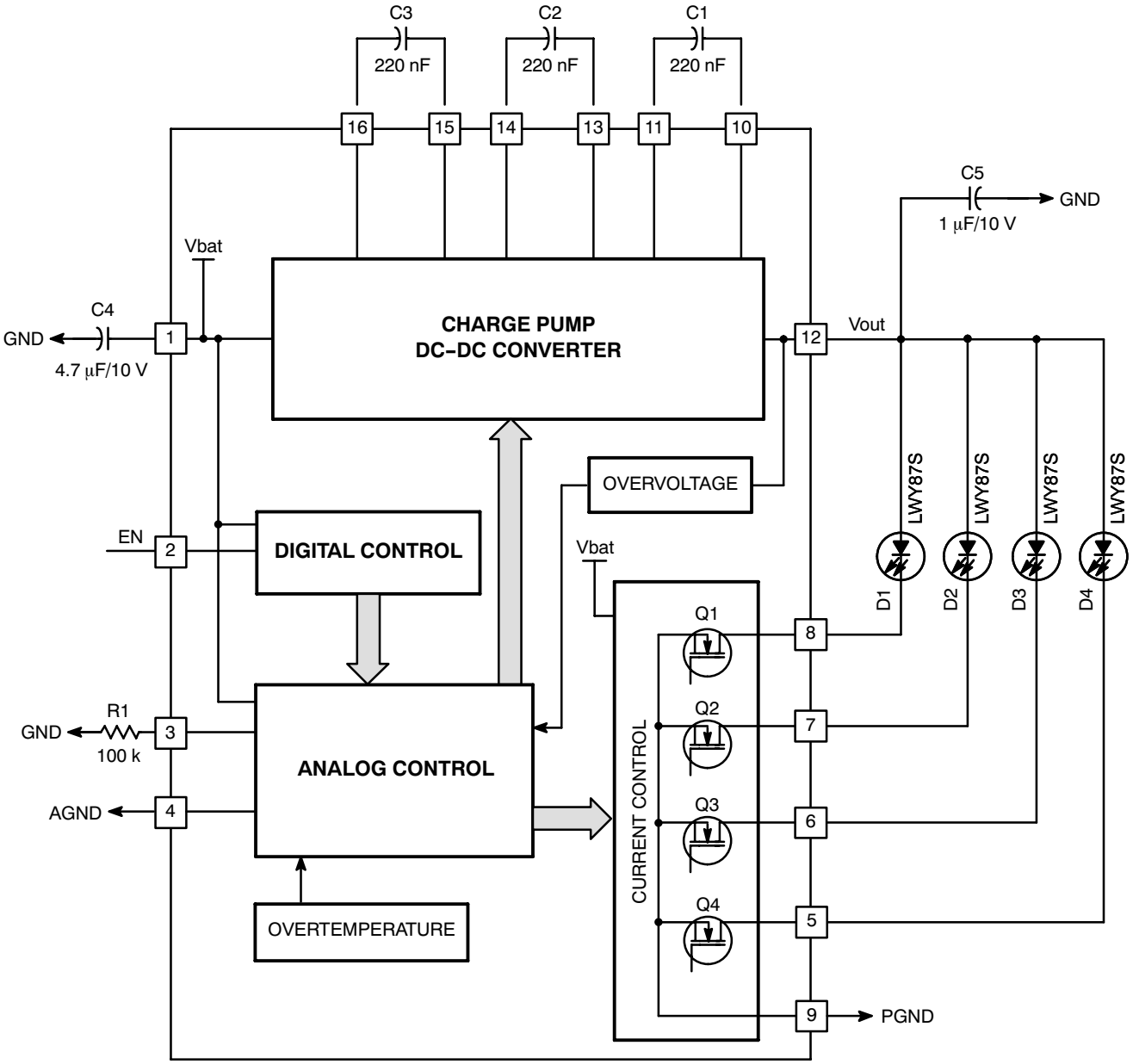


Figure 2. NCP5604A Simplified Block Diagram

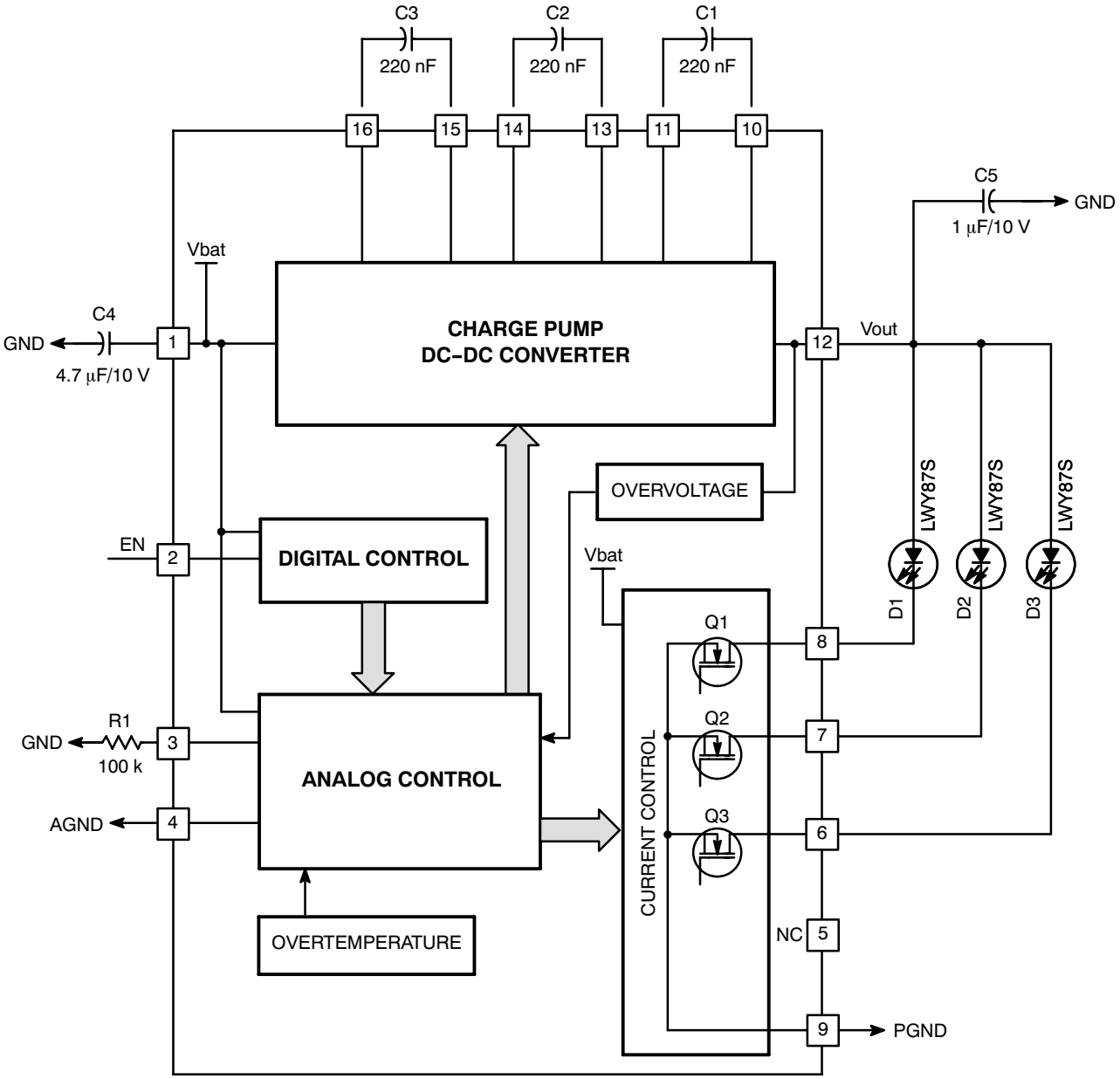


Figure 3. NCP5604B Simplified Block Diagram (Pin 5 disconnected)

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1	VBAT	INPUT, POWER	Input Battery voltage to supply the analog and digital blocks. The pin must be decoupled to ground by a 1.0 μF ceramic capacitor.
2	EN	INPUT, DIGITAL	This pin carries the Enable function to control the DC−DC converter. It can be used to digitally dim the LED by using a PWM technique. EN = Low → shutdown mode, the DC−DC is disconnected from the load. EN = High → operating mode, the DC−DC is activated. The digital PWM dimming can operate over the 100 Hz − 200 kHz frequency, depending upon the application requirements.
3	I_{REF}	INPUT, ANALOG	This pin provides the reference current, based on the internal bandgap voltage reference, to control the output current flowing in the LED. A 1% tolerance, or better, resistor shall be used to get the highest accuracy of the LED biases. An external current source can be used to bias this pin to dim the light coming out of the LED. In no case shall the voltage at pin 3 be forced either higher or lower than the 600 mV provided by the internal reference.
4	AGND	POWER	This pin is the GROUND signal for the analog and digital blocks and must be connected to the system ground.
5	LED4	INPUT, POWER	NCP5604A: This pin sinks to ground and monitors the current flowing into the fourth LED, intended to be used in backlight application. The current is limited to 25 mA maximum (Note 2). NCP5604B: This pin is not connected.
6	LED3	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the third LED, intended to be used in backlight application. The current is limited to 25 mA maximum (Note 2).
7	LED2	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the second LED, intended to be used in backlight application. The current is limited to 25mA maximum (Note 2).
8	LED1	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the first LED, intended to be used in backlight application. The current is limited to 25 mA maximum (Note 2).
9	PGND	POWER	This pin is the GROUND reference for the DC−DC converter and the output current control. The pin must be connected to the system ground, a ground plane being strongly recommended.
10	C1N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1P, pin 11 (Note 1).
11	C1P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1N, pin 10 (Note 1).
12	VOUT	OUTPUT, POWER	This pin provides the output voltage supplied by the DC−DC converter. The Vout pin must be bypassed by 1.0 μF ceramic capacitor located as close as possible to the pin to properly bypass the output voltage to ground. The circuit shall not operate without such bypass capacitor properly connected to the Vout pin. The output voltage is internally clamped to 5.5 V in the event of no load situation. On the other hand, the output current is limited to 100 mA in the event of a short circuit to ground.
13	C2P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2N, pin 14 (Note 1).
14	C2N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2P, pin 13 (Note 1).
15	C3P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C3N, pin 16 (Note 1).
16	C3N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C3P, pin 15 (Note 1).

1. Using low ESR 1.0 μF ceramic capacitor is mandatory to optimize the Charge Pump efficiency. The DC Bias effect must be taken into account when selecting the ceramic capacitor. Smallest foot print packages (size 0602 and lower) are prone to strong DC bias effect, reducing the real capacitance significantly.
2. Total DC−DC output current is limited to 100 mA.
3. The exposed flag shall be connected to ground.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply	V_{BAT}	7.0	V
Output Power Supply	Vout	7.0	V
Digital Input Voltage Digital Input Current	EN	$-0.3 < V < V_{BAT}$ 1.0	V mA
Human Body Model: R = 1500 Ω, C = 100 pF (Note 4) Machine Model	ESD	2 200	kV V
QFN16 Package Power Dissipation @ T_A = +85°C (Note 5) Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$	 320 125	 mW °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Moisture Sensitivity Level (Note 7)	MSL	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM): JESD22−A114.
   Machine Model (MM): JESD22−A115.
5. The maximum package power dissipation limit must not be exceeded.
6. Latchup current maximum rating: ± 100 mA per JEDEC standard: JESD78.
7. Moisture Sensitivity Level (MSL): per IPC/JEDEC standard: J−STD−020A.

POWER SUPPLY SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.)

Pin	Symbol	Rating	Min	Typ	Max	Unit
1	V_{bat}	Power Supply	2.7	–	5.5	V
12	I_{out}	Continuous DC Current in the Load (Note 8) @ Vf = 3.2 V, 3.3 V < Vbat < 5.5 V (Total Iout = 4*LED)	100	–	–	mA
12	Isch	Continuous Output Short Circuit Current	–	40	150	mA
12	V_{out}	Output Voltage Compliance (OVP)	4.8	–	6.0	V
12	Tstart	DC−DC Start Time (Cout = 1.0 μF) – from Vout = 0 V to full load operation, @ Vbat = nominal	–	100	–	μs
1	I_{stdb}	Standby Current, @ Iout = 0 mA, EN = GND Vbat = 3.6 V Vbat = 4.2 V	 – –	 0.3 0.4	 3.0 5.0	μA
1	I_{op}	Operating Current, @Iout = 0 mA, EN = H 2.85 V < Vbat < 5.5 V Vbat = 3.6 V	 – –	 1.0 –	 – 1.5	mA
5, 6, 7, 8	I_{MAT}	Output LED to LED Current Matching, @ Vbat = 3.6 V, I_{LED} = 20 mA, LED1 to LED4 are identical (Note 9)	−2.0	±0.2	+2.0	%
5, 6, 7, 8	I_{TOL}	Output Current Tolerance (Note 9) @ 3.2 V < Vbat < 4.2 V, I_{LED} = 20 mA	−5.0	±1.0	+5.0	%
–	Fpwr	Charge Pump Operating Frequency −25°C < T_A < 85°C	0.85	1.0	1.15	MHz
–	T_{SD}	Thermal Shutdown Protection	–	160	–	°C
–	T_{SDH}	Thermal Shutdown Protection Hysteresis	–	30	–	°C
–	E_{PWR}	Efficiency (Note 9) LED1 to LED4 = 5.0 mA, Vf = 2.95 V (Total = 20 mA), Vbat = 3.2 V LED1 to LED4 = 25 mA, Vf = 3.3 V (Total = 100 mA), Vbat = 3.8 V	 – –	 87 85	 – –	%

8. The total output current is evenly distributed across the external LED.
9. LED4 is not connected in the NCP5604B version.
10. The NCP5604B controls 75 mA in total in the three current mirrors, the extra 25 mA available current from the DC−DC converter being available for external purpose.

ANALOG SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.)

Pin	Symbol	Rating	Min	Typ	Max	Unit
3	I_{REF}	Reference Current @ Vref = 600 mV (Note 11)	1.0	–	100	μA
3	V_{REF}	Reference Voltage (Note 12)	−2%	600	+2%	mV
–	I_{LEDR}	Reference Current (IREF) to Output LED Current Ratio	–	260	–	–

11. The overall output current tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.
12. The external circuit must not force the I_{REF} pin voltage either higher or lower than the 600 mV specified.

DIGITAL PARAMETERS SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.) Note: Digital inputs undershoot < − 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{BAT}.

Pin	Symbol	Rating	Min	Typ	Max	Unit
2	F_{PWM}	Input Enable PWM	0.1	–	200	kHz
2	V_{IH}	Positive Going Input High Voltage Threshold, EN Signal	1.3	–	V_{BAT}	V
2	V_{IL}	Negative Going Input High Voltage Threshold, EN Signal	0	–	0.4	V

APPLICATIONS INFORMATION

DC−DC OPERATION

The converter is based on a charge pump technique to generate a DC voltage capable to supply the White LED load The system regulates the current flowing into each LED by means of internal current mirrors associated with the white diodes. Consequently, the output voltage will be equal to the Vf of the LED, plus the 300 mV (typical) developed across the internal NMOS mirror. Typically, assuming a standard white LED forward biased at 10 mA, the output voltage will be 3.8 V.

The third external capacitor makes possible the 1.33X extra mode of operation, with a significant efficiency improvement of the converter over the normal battery voltage span. The threshold levels have been defined to optimize this range of operating voltage, assuming a high efficiency is not relevant when the system is connected to a battery charger (i.e. Vbat > 4.5 V).

The built−in OVP circuit continuously monitor each output and stops the converter when the voltage is above 5.0 V. The converter resumes to normal operation when the voltage drops below 5.0 V (no latch−up mechanism). Consequently, the chip can operate with no load during any test procedures, but in the case of special applications, it is recommended to connect the non used LED driver either to a LED, or to the Vbat supply to minimize the internal losses (see LOAD CONNECTION paragraph).

LOAD CURRENT CALCULATION

The load current is derived from the 600 mV reference voltage provided by the internal Band Gap associated to the external resistor connected across I_{REF} pin and Ground (see Figure 4). In any case, no voltage shall be forced at I_{REF} pin, either downward or upward.

The reference current is multiplied by the constant k = 260 to yield the output load current. Since the reference voltage is based on a temperature compensated Band Gap structure, a tight tolerance resistor will provide a very accurate load current. The resistor is calculated from the Ohm's law (R_{bias} = Vref/I_{REF}) and a more practical equation can be arranged to define the resistor value for a given output current:

$$R_{bias} = (Vref * k)/Iout$$
$$R_{bias} = (0.6 * 260)/Iout \quad \text{(eq. 1)}$$

$$R_{bias} = 156/Iout \quad \text{(eq. 2)}$$

Consequently, the resistor value will range between R_{bias} = 156/25 mA = 6240 Ω and R_{bias} = 156/0.5 mA = 312 kΩ. Obviously, the tolerance of such a resistor must be 1% or better, with a 100 ppm thermal coefficient, to get the expected overall tolerance.

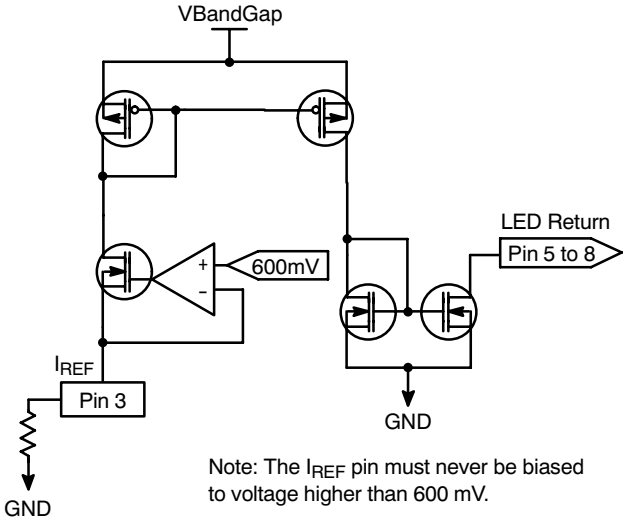


Figure 4. Basic Reference Current Source

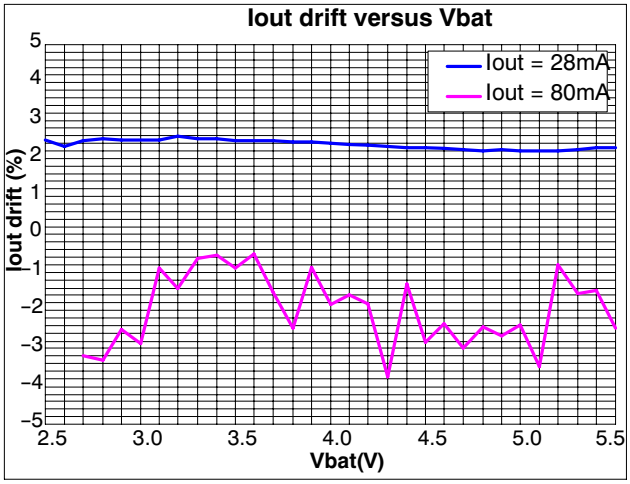


Figure 5. Typical I_{OUT} Tolerance as a Function of the V_{BAT} Supply

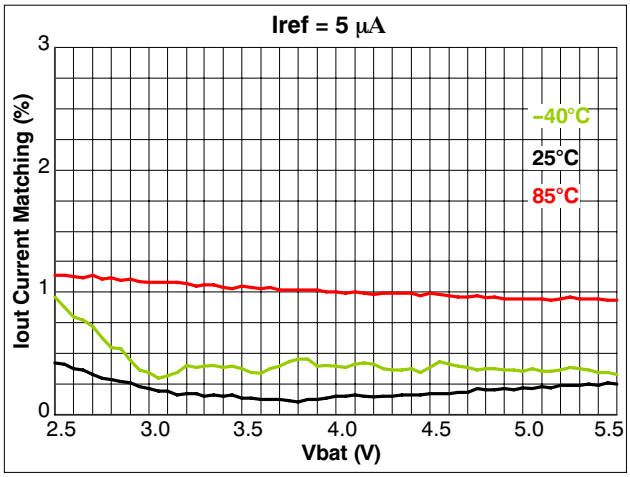


Figure 6. Typical LED to LED Current Matching at Low I_{REF}

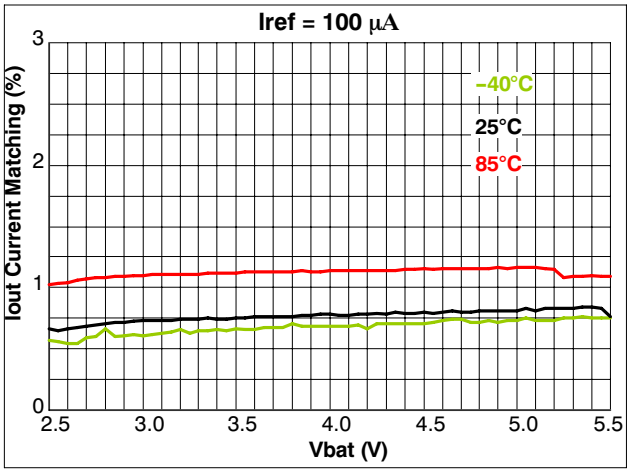


Figure 7. Typical LED to LED Current Matching at I_{REF} Maximum

LOAD CONNECTION

The NCP5604A chip is capable of driving the four LED simultaneously, as depicted in Figure 1, but the load can be arranged to accommodate one or two LED if necessary in the application (see Figure 8). The four current mirror can be connected in parallel to drive a single powerful LED, thus yielding 100 mA current capability in a single LED.

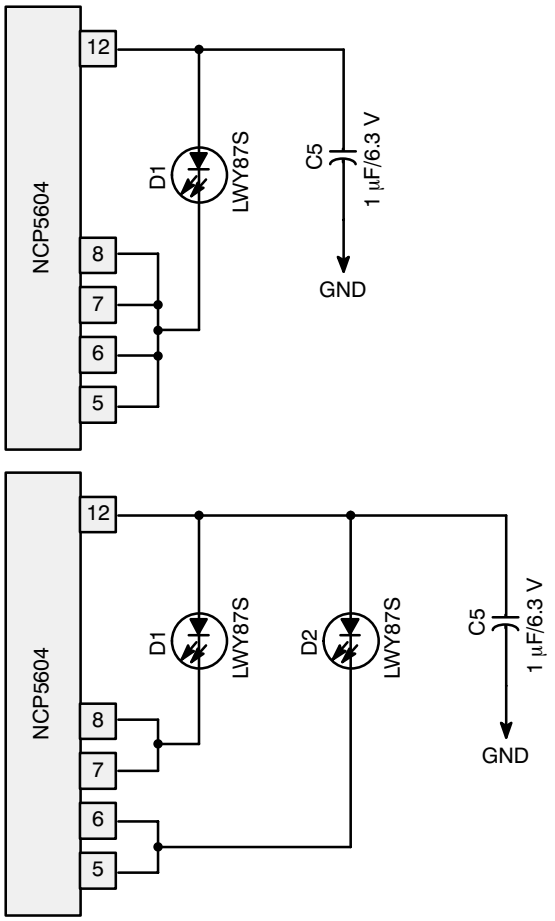


Figure 8. Typical Single and Double LED Connections

The applications using three LED shall use the NCP5604B version to make profit of the highest efficiency (see Figure 9). In this case, LED4 is not connected and pin 5 is internally unconnected.

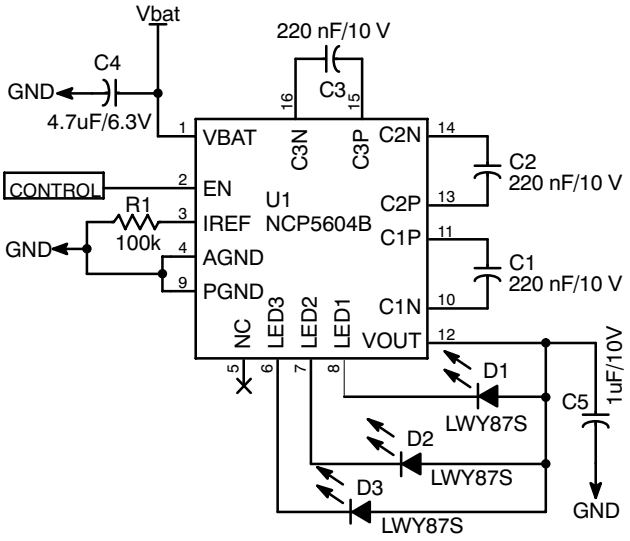


Figure 9. Using the NCP5604B to Drive a Three LED Layout

Finally, an external network can be connected across Vout and ground, but the current through such network will not be regulated by the NCP5604A chip (see Figure 10). On top of that, the total current out of the Vout pin shall be limited to 100 mA.

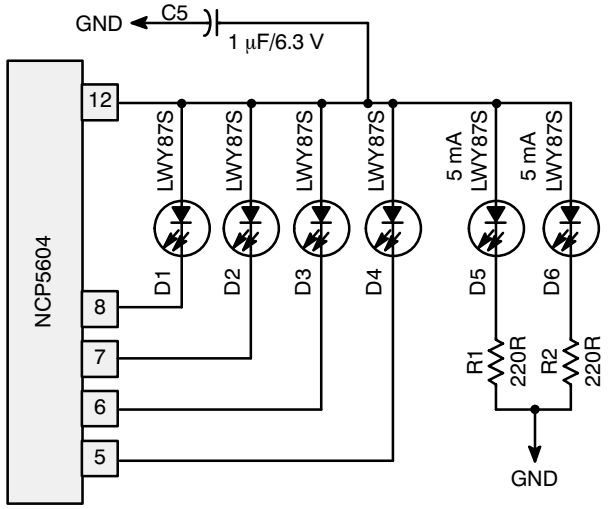


Figure 10. Extra Load Connected to Vout

DIMMING

The dimming can be achieved by two means:

- Use a digital PWM signal to control the EN pin
- Use an analog signal to control the reference current IREF pin.

The digital PWM is straightforward, yielding a zero to 100% duty cycle, but the output current is pulsed since the system is continuously switched ON/OFF. There is no need for extra passive component, the clock being provided by an I/O port from the MCU (see Figure 11).

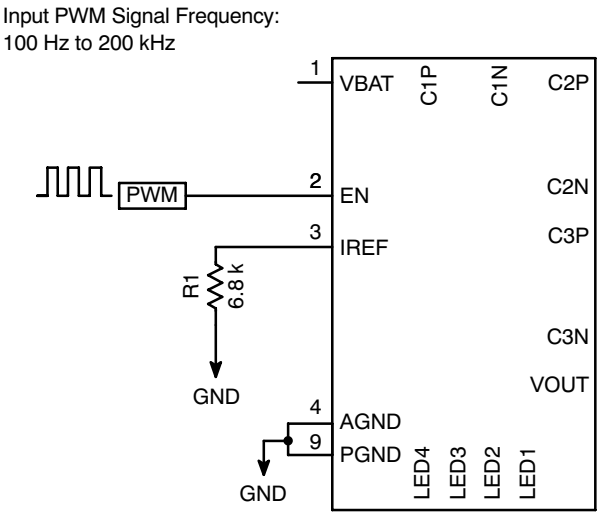


Figure 11. Basic Digital PWM Dimming Control

The PWM frequency can be up to 200 kHz once the circuit has been properly started. On the other hand, with a 1% to 99% span, the circuit supports a large Duty Cycle to accommodate any range of dimming. The waveforms given in Figure 12 illustrate the NCP5604A behavior during the 50 kHz PWM operation. The same mechanism applies for the NCP5604B version.

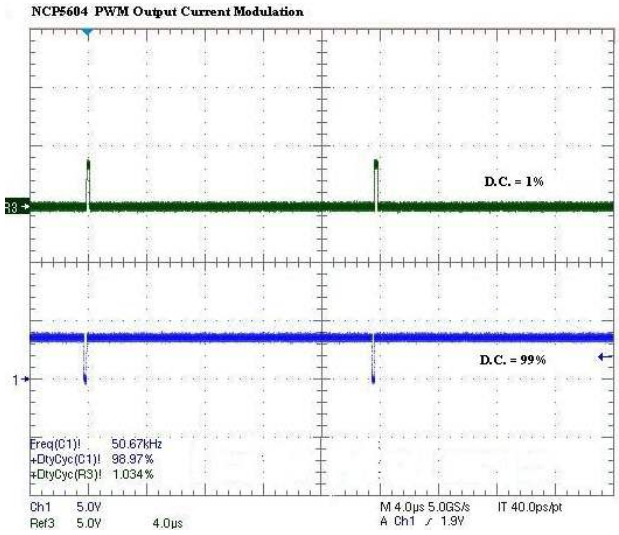


Figure 12. PWM Modulation Span: 1% to 99%

Besides the popular PWM mode, a simple analog technique can be built with two extra components (one resistor + one NMOS), the net advantage being a continuous output current once the operating point has been stabilized (see Figure 13). The absolute output current tolerance depends upon the precision of the two external resistors, the $R_{DS(on)}$ of the NMOS being negligible in front of the resistor value. The example given, Figure 13 yields a 1.0 mA output current when Q1 is OFF,

and 23 mA when Q1 is ON. The concept can use either a DC drive or a pulsed mode to dynamically dim the light out of the LED.

A different analog approach, but more complex solution, can be derived from either a DC or a pulsed voltage associated with a current mirror built with low cost discrete devices (see Figure 14). The associated filter (R2/R3/C1) provides a continuous voltage to the current mirror, thus a digitally controlled continuous output current. Generally speaking, the PWM frequency could be either in the low end 20 Hz to 200 Hz band, or above the audio band (25 kHz and beyond) to make sure the dimming can be adjusted from zero to 100% without any audible noise. As a matter of fact, the NCP5604A has been designed to guarantee 200 kHz PWM at the ENABLE pin.

The current mirror can be largely improved by using an external operational amplifier to get a very stable and temperature independent current, but such a solution could turn out to be too expensive and, generally speaking, the basic structure given, Figure 13, gives good results since the current depends mostly upon the quality of resistor R2.

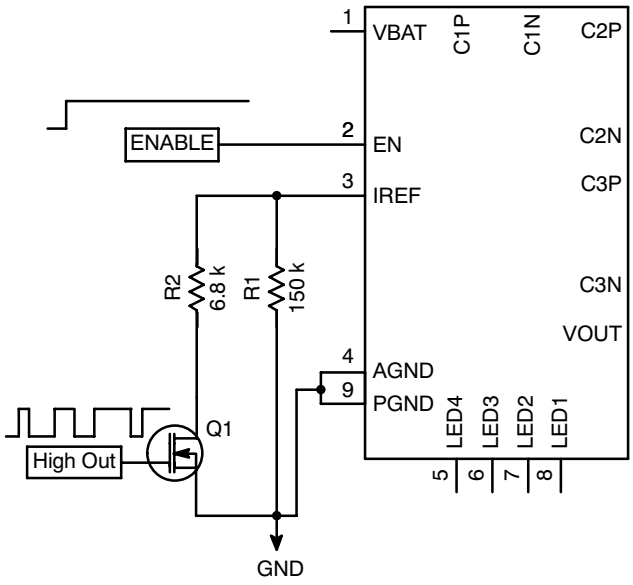


Figure 13. Basic Analog Dimming Control

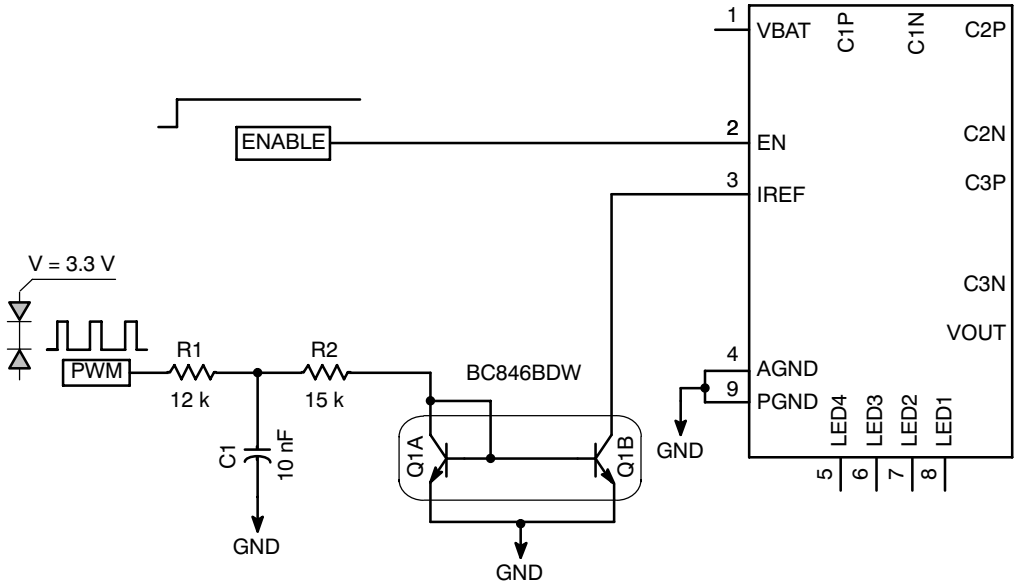


Figure 14. Basic Analog PWM Dimming Control

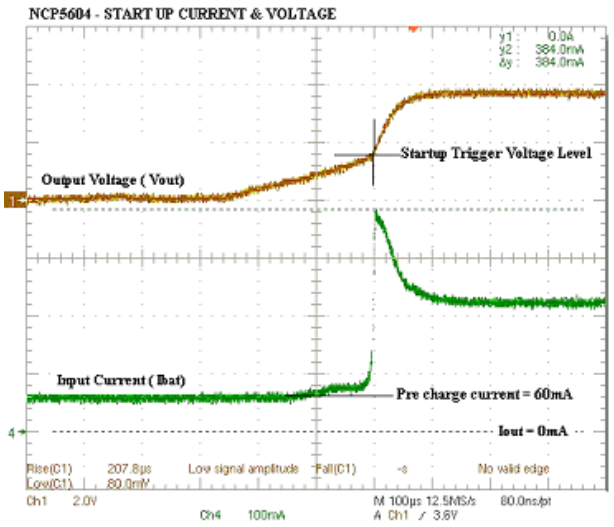


Figure 15. Startup Operation

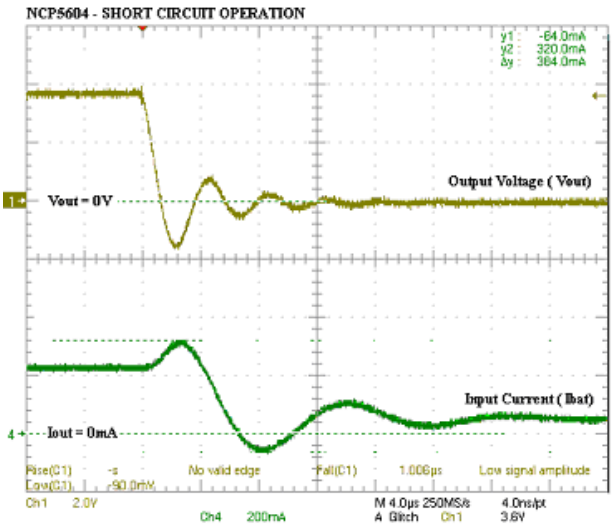


Figure 17. Input Current Short Circuit Operation

SHORT CIRCUIT OPERATION

The circuit is designed to support a short circuit across Vout and Ground without damage. When a short occurs, the pulsed output current increases to the maximum peak value until the output voltage drops below 1 V. At this point, the pulsed current is limited to 40 mA average (typical), until the short is removed. The waveforms given in Figure 16 illustrate the functional operation. Similarly, the input current is limited 300 mA peak (typical) as depicted in Figure 17.

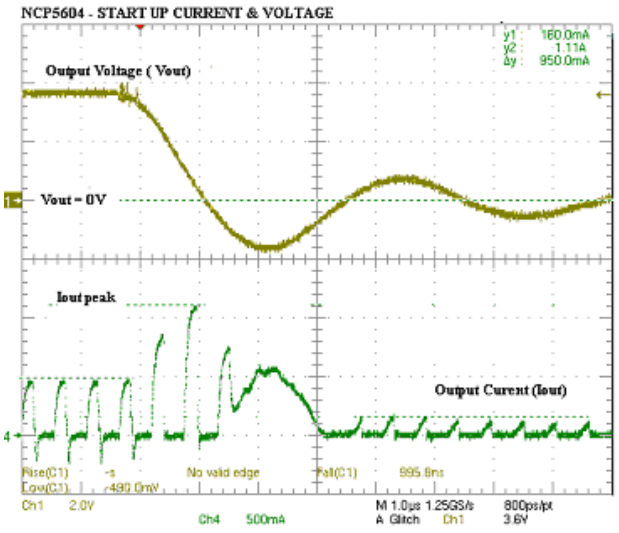


Figure 16. Output Short Circuit Operation

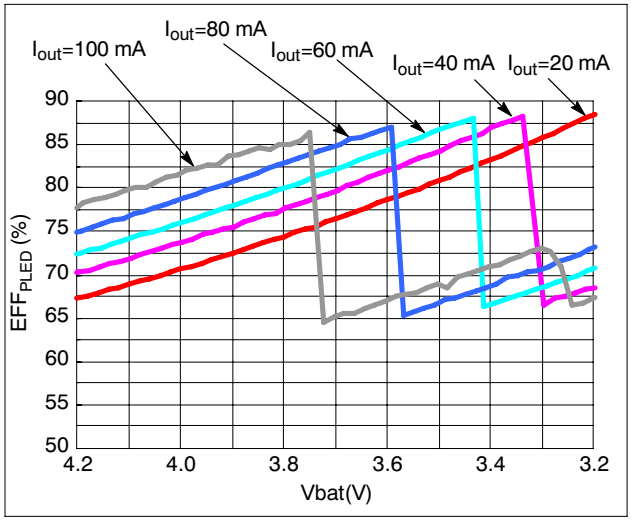


Figure 18. Typical Efficiency

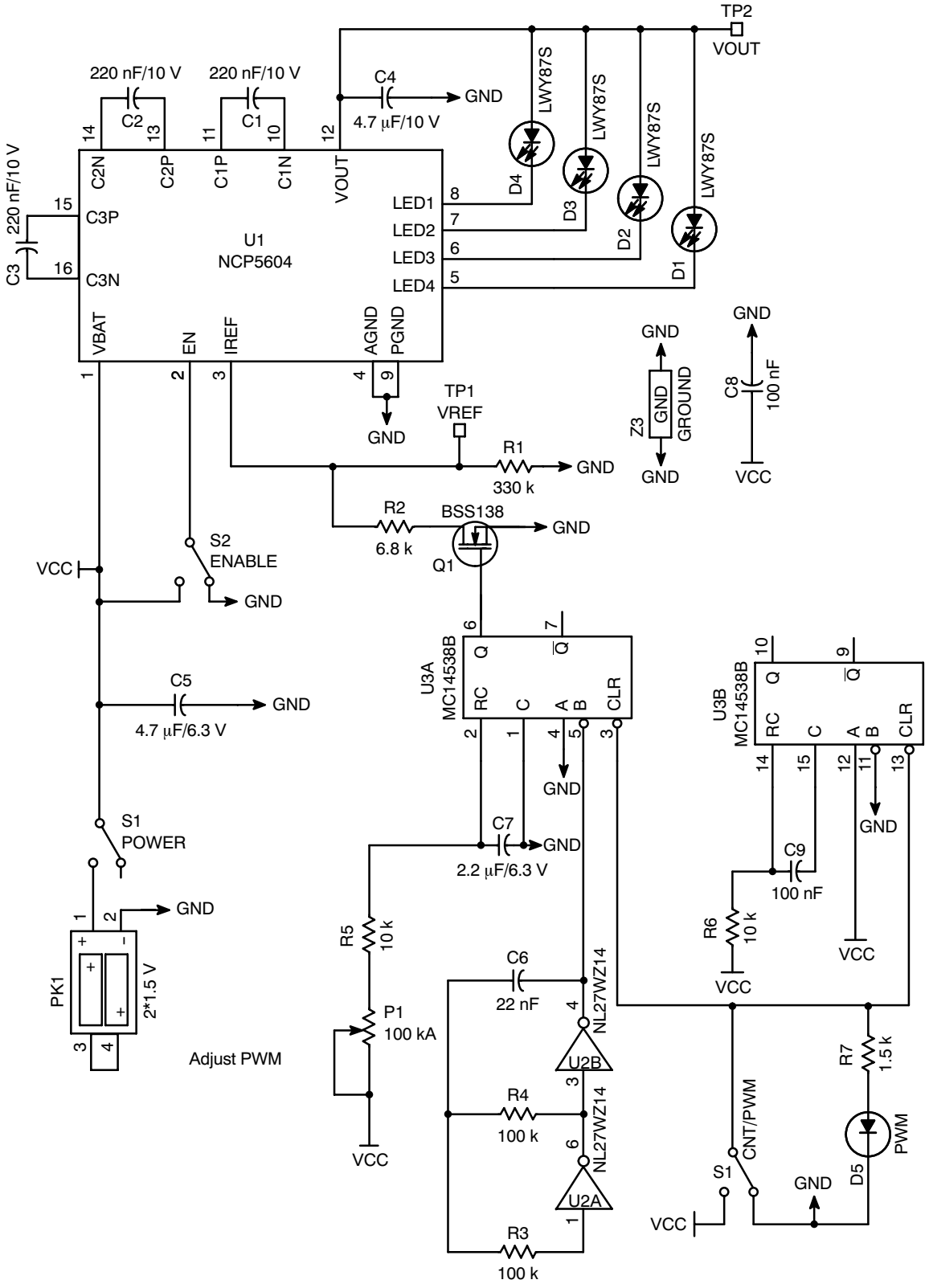


Figure 19. Demo Board Schematic Diagram

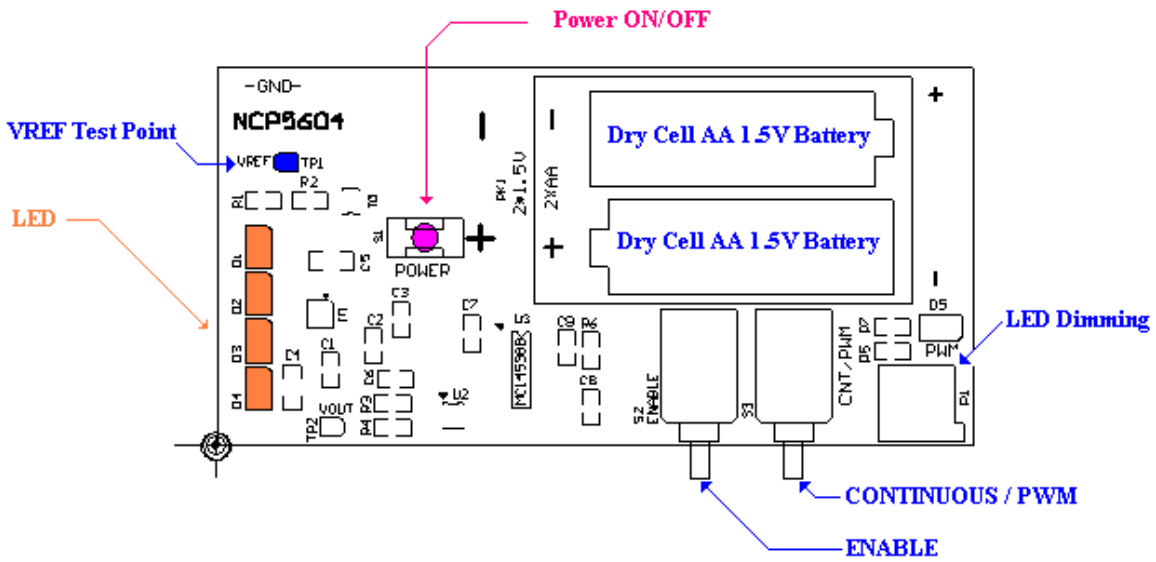


Figure 20. Silk View Top Layer

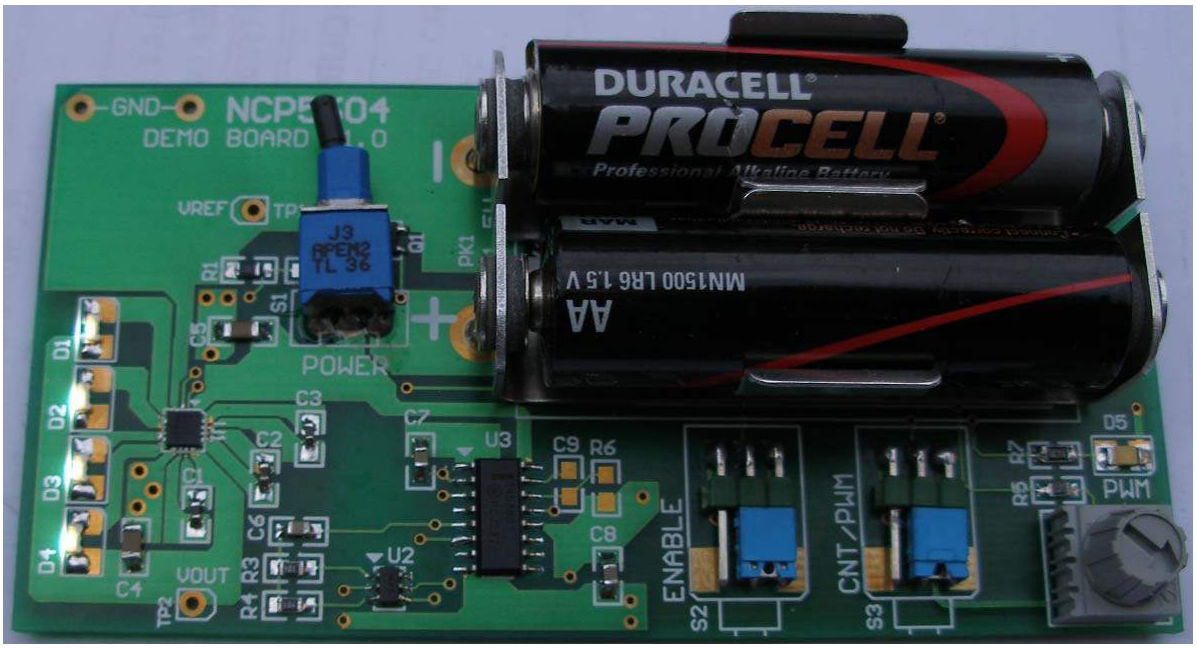
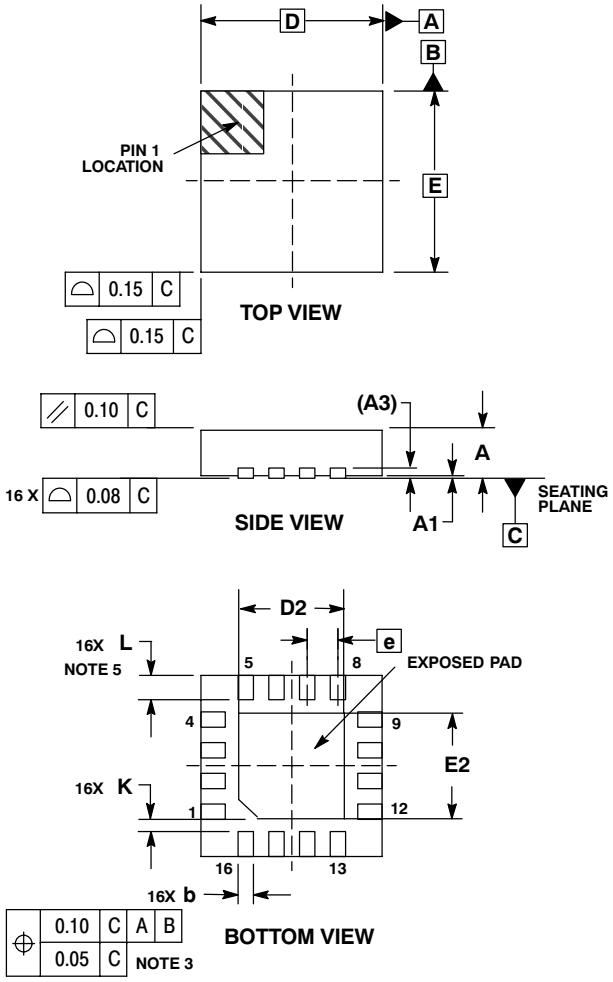


Figure 21. Demo Board Printed Circuit Layout

PACKAGE DIMENSIONS

WQFN16
MT SUFFIX
CASE 488AK−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your loca
Sales Representative