Using the TPS650250EVM Power Management IC for Li-Ion Powered Systems

The TPS650250EVM is an integrated Power Management evaluation tool for use of the TPS650250 in applications that are powered with one Li-Ion or Li-Polymer cell and require multiple power rails. The TPS650250 contains three adjustable highly efficient switching step-down converters, three LDOs, and additional status and I/O pins.

Contents

List of Figures

List of Tables

1 Introduction

1.1 Description

The TPS650250 provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O and memory rails in a processor based system. All three step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents. The converters can be forced into fixed frequency PWM mode by pulling the MODE pin high.

The TPS650250 also integrates two general purpose 200mA LDO voltage regulators, which are enabled with an external input pin. Each LDO operates with an input voltage range between 1.5V and 6.5V allowing them to be supplied from one of the step-down converters or directly from the battery. The output voltage of the LDOs can be set with an external resistor divider for maximum flexibility. Additionally there is a 30mA LDO typically used to provide power in a processor based system to a voltage rail that is always on. TPS650250 comes in a small 5mm $\times$ 5mm 32 pin QFN package (RHB).

1.2 Applications

- Smart / Cellular Phone
- Digital Still Cameras
- Samsung ARM based Processors, etc
- Freescale™ i.MX31 procesors, etc.
- Split Supply DSP and uP Solutions

1.3 Features

- Input Voltage Range : 3.3V up to 5.5V
- All Output DCDC Converters and LDOs Externally Adjustable
- Default Output Voltages for DCDC1 and DCDC2
- Output Current Rating : 1.6-A (DCDC1) / 0.8-A (DCDC2) / 0.8-A (DCDC3) 0.2-A (LDO1, LDO2)
- 2.25-MHz Switching Frequency
- Thermal Shutdown Protection

2 TPS650250EVM Electrical Performance Specifications

Table 1. TPS650250EVM Electrical and Performance Specifications

Parameter		Notes & Conditions		Min	Nom	Max	Units
INPUT CHARACTERISTICS							
V_{IN}	Input Voltage			3.3		5.5	V
V_{IN_UVLO}	Input UVLO	V_{IN} falling			2.35		V
OUTPUT CHARACTERISTICS							
V_{OUT_DCDC1}	Output Voltage DCDC1	V_{IN} = Nom, I_{OUT} = Nom	DEFDCDC1 = high		3.3		V
			DEFDCDC1 = low		2.7		
V_{OUT_DCDC2}	Output Voltage DCDC2	Vin = 3.3V to 6 V, Iout = 0 mA to 800 mA	DEFDCDC2 = high		2.5		V
			DEFDCDC2 = low		1.8		
	Accuracy DCDC1, DCDC2	VINDCDC2 = 3.3V to 6V, Iout = 0 mA to 800 mA	PFM/PWM	–2%		2%	
			PWM	-1%		1%	
V_{OUT_DCDC3}	Output Voltage DCDC3	VIN = 3.3V to 6V, Iout = 0 mA to 800 mA			1.2		V
	Accuracy DCDC3	Vin = 3.3V to 6 V, Iout = 0 mA to 800 mA, With 1% tolerance resistors	PFM/PWM	-4%		4%	
			PWM	–3%		3%	
F_{SW}	Switching Frequency				2250		kHz
V_{OUT_LDO1}	Output Voltage LDO1				2.5		V
V_{OUT_LDO2}	Output Voltage LDO2				1.4		V
	Accuracy LDO1, LDO2	Iout = 10 mA, with 1% tolerance resistors		–3%		5%	
V_{VDD_ALIVE}	Output Voltage VDD_Alive				1.0		V
	Accuracy VDD_Alive	Iout = 0 mA		–3%		3%	
I_{OUT_DCDC1}	Output Current DCDC1	V_{OUT} = Nom		1600			mA
I_{OUT_DCDC2}	Output Current DCDC2	V_{OUT} = Nom		800			mA
I_{OUT_DCDC3}	Output Current DCDC3	V_{OUT} = Nom		800			mA
	Output Current LDO1, LDO2	V_{IN} = 1.8 V, V_{OUT} = 1.3 V		200			mA
	Output Current LDO1, LDO2	V_{IN} = 1.5 V, V_{OUT} = 1.3 V			120		mA
	Output Current VDD_ALIVE					30	mA

3 Modifications

3.1 Voltage Scaling for DCDC3

The output voltage of DCDC3 is externally adjustable with the resistor divider network R10 and R11.

The factory EVM configuration is R10 = 182k and R11 = 182k, resulting in an output voltage of 1.2V.

See the TPS650250 data sheet (SLVS843) for assistance on changing the output voltage.

DCDC3 has no preset default output voltages as DCDC1 and DCDC2.

There is a voltage scaling circuit on the EVM, so the output voltage of DCDC3 can be switched between two voltages. This feature is very useful in order to reduce the power consumption of an application processor in Low Power Mode.

The voltage scaling circuit consist of JP5,Q1, R7 and R8. The circuit uses a transistor (Q8) to connect a resistor (R8) in parallel to the lower resistor of the feedback network (R11) of DCDC3.

In factory configuration the components JP5, Q1, R7 and R8 are not assembled on the board.

The EVM has a SOT23 footprint for Q1, so any SOT23 transistor can be used.

Note: Modifying the resistor network by paralleling R11 and R8 will reduce the overall resistance of the lower resistor and therefore increase the output voltage of the DCDC converter. See Equation 1 and Equation 2 to design R8.

$$Rx = \frac{(R10 \times VREF)}{(V_{OUTDCDC\_2} - VREF)} \quad (1)$$

$$R8 = \frac{(R11 \times Rx)}{(R11 - Rx)} \quad (2)$$

With:

1. R10: Upper resistor of the feedback driver
2. R11: Lower resistor of the feedback driver
3. Rx = R8 ‖ R11
4. $V_{OUTDCDC2}$: Output voltage when scaling circuit active
5. VREF: Reference voltage

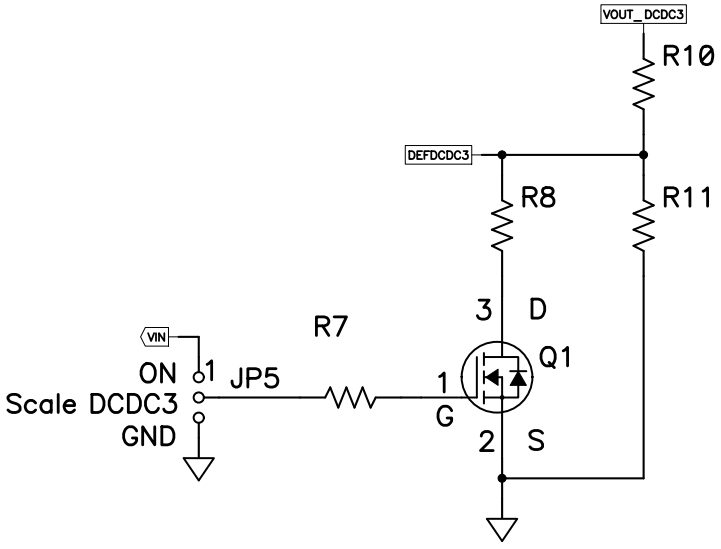

Figure 1. Voltage Scaling Circuit

4 Schematic

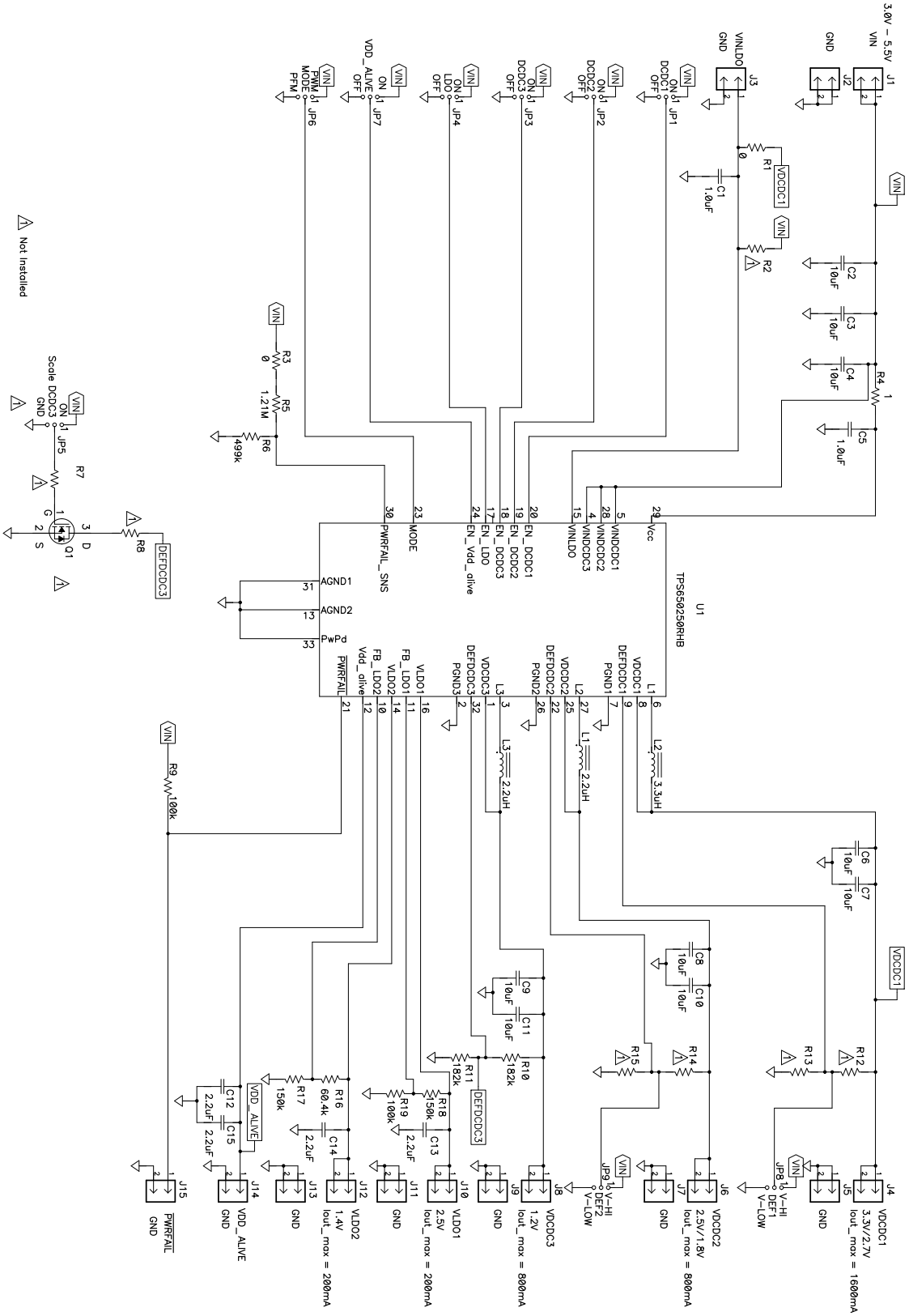

Figure 2. TPS650250 EVM Schematic

5 Connector and Test Point Descriptions

5.1 J1 –VIN

This header is the positive connection to the input power supply. The power supply must be connected between J1 and J2 (GND). The leads to the input supply should be twisted and kept as short as possible. The input voltage has to be between 3.3-V and 6-V.

5.2 J2 – GND

This header is the return connection to the input power supply. Connect the power supply between J12 and J1 (VIN). The leads to the input supply should be twisted and kept as short as possible. The input voltage has to be between 3.3-V and 6-V.

5.3 J3 – VINLDO/GND

This header is the input supply for the LDOs LDO1, LDO2 and VDD_ALIVE. On the EVM VINLDO is directly connected to VIN with R2. It can be also connected to VDCDC1 with R1.

An external power supply can be connected between J3 pin1 (VINLDO) and pin2 (GND). Note that the resistors R1 and R2 should be removed when supplying the LDOs from an external power supply.

5.4 J4 – VDCDC1

This header is the positive output of VDCDC1 step-down converter. The output voltage of DCDC1 can be selected between two default output voltage (3.3-V/2.7-V) with JP8 DEF1. In addition the output voltage of DCDC1 can be adjusted to any voltage between 0.6-V and VINDCDC1 with the external voltage divider R12 and R13.

Note that the shorting jumper JP8 should be removed when using the external voltage divider.

The default setting is 3.3-V. VDCDC1 is capable of sourcing up to 1600-mA. A load can be connected between J4 and J5 (GND)

5.5 J5 – GND

J5 is the return connection of VDCDC1 output rail. A load can be connected between J5 and J4 (VDCDC1).

5.6 J6 – VDCDC2

This header is the positive output of VDCDC2 step-down converter. The output voltage of DCDC2 can be selected between two default output voltage (2.5-V/1.8-V) with JP9 DEF2. In addition the output voltage of DCDC1 can be adjusted to any voltage between 0.6-V and VINDCDC2 with the external voltage divider R14 and R15.

Note that the shorting jumper JP9 should be removed when using the external voltage divider.

The default setting is 1.8-V. VDCDC2 is capable of sourcing up to 800-mA. A load can be connected between J6 and J7 (GND).

5.7 J7 – GND

J7 is the return connection of VDCDC2 output rail. A load can be connected between J7 and J6 (VDCDC2).

5.8 J8 – VDCDC3

This header is the positive output of VDCDC3 step-down converter. This output is externally adjustable for the TPS650250. The default setting is 1.2-V. VDCDC3 is capable of sourcing up to 800-mA. A load can be connected between J8 and J9 (GND).

5.9 J9 – GND

J9 is the return connection of VDCDC2 output rail. A load can be connected between J9 and J8 (VDCDC3).

5.10 J10 – VDLO1

This header is the positive output of LDO1 linear regulator. This output is externally adjustable for the TPS650250 and is programmed to a value of 2.5-V on the EVM. The VLDO1 output is capable of supplying up to 200-mA. A load can be connected between J10 and J11 (GND).

5.11 J11 – GND

J11 is the return connection of VLDO1 output rail. A load can be connected between J11 and J10 (VLDO1).

5.12 J12 – VDLO2

This header is the positive output of LDO2 linear regulator. This output is externally adjustable for the TPS650250 and is programmed to a value of 1.4-V on the EVM. The VLDO2 output is capable of supplying up to 200-mA. A load can be connected between J12 and J13 (GND).

5.13 J13 – GND

J11 is the return connection of VLDO2 output rail. A load can be connected between J13 and J12 (VLDO2).

5.14 J14 – VDD_ALIVE/GND

This header is the positive output of LDO3 VDD_ALIVE. The output voltage is fixed to 1.0V in the TPS650250.

The VDD_ALIVE output is capable of sourcing up to 30mA of load current. A load can be connected between J14 pin1 (VDD_ALIVE) and pin2 (GND).

In applications that use Samsung application processors the VDD_ALIVE output is typically connected to the VDD_ALIVE input of the application processor.

5.15 J15 – PWRFAIL/GND

PWRFAIL is an open drain output, that is pulled up to VIN. PWRFAIL goes low if the PWRFAIL_SNS input falls below 1.0V. On the EVM the default settings is PWRFAIL goes low when VIN falls below 3.4V. This threshold can be changed by modifying the resistor network R5 and R6.

5.16 JP1 – EN_DCDC1

Placing a shorting bar between EN_DCDC1 and ON ties the EN pin of DCDC1 to VIN, thereby enabling DCDC1. Placing a shorting bar between EN_DCDC1 and OFF ties the EN pin of DCDC1 to GND, thereby disabling DCDC1.

5.17 JP2 – EN_DCDC2

Placing a shorting bar between EN_DCDC2 and ON ties the EN pin of DCDC2 to VIN, thereby enabling DCDC2. Placing a shorting bar between EN_DCDC2 and OFF ties the EN pin of DCDC2 to GND, thereby disabling DCDC2.

5.18 JP3 – EN_DCDC3

Placing a shorting bar between EN_DCDC3 and ON ties the EN pin of DCDC3 to VIN, thereby enabling DCDC3. Placing a shorting bar between EN_DCDC3 and OFF ties the EN pin of DCDC3 to GND, thereby disabling DCDC1.

5.19 JP4 – EN_LDO

Placing a shorting bar between EN_ LDO and ON ties the pin EN_LDO to VIN, thereby enabling LDO1 and LDO2. Placing a shorting bar between EN_LDO and OFF ties the pin EN_LDO to GND, thereby disabling LDO1 and LDO2.

5.20 JP5 – SCALE_DCDC3

NO TEXT IN THIS ONE

5.21 JP6 – MODE

JP6 selects the forced PWM or Power Save Mode (PSM) operation for the switching converters DCDC1,DCDC2 and DCDC3.

Placing a shorting bar between MODE and PWM ties the MODE pin of TPS650250 to VIN, thereby selecting forced PWM operating mode for the DCDC converters. Placing a shorting bar between MODE and PSM (Power Save Mode) ties the MODE pin of TPS650250 to GND, thereby selecting Power Save Mode operating mode for the DCDC converters at light-load conditions. If Power Save Mode is selected the DCDC converters will automatically switch to PWM mode at heavier load conditions.

5.22 JP7 – EN_VDD_ALIVE

Placing a shorting bar between EN_ VDD_ALIVE and ON ties the pin EN_VDD_ALIVE to VIN, thereby enabling VDD_ALIVE. Placing a shorting bar between EN_VDD_ALIVE and OFF ties the pin EN_VDD_ALIVE to GND, thereby disabling VDD_ALIVE.

5.23 JP8 – DEF1

JP8 selects the default output voltage for the switching converter DCDC1.

Placing a shorting bar between DEF1 and V-HI sets the default output voltage of DCDC1 to 3.3-V.

Placing a shorting bar between DEF1 and V-LOW sets the default output voltage of DCDC1 to 2.7-V.

5.24 JP9 – DEF2

JP8 selects the default output voltage for the switching converter DCDC2.

Placing a shorting bar between DEF1 and V-HI sets the default output voltage of DCDC2 to 2.5-V.

Placing a shorting bar between DEF1 and V-LOW sets the default output voltage of DCDC2 to 1.8-V.

5.25 Factory Jumper Setup

The EVM comes from the factory with the following default jumper settings.

Table 2. TPS650250 EVM Factory Jumper Setup

Jumper	Shunt Location	
JP1	Between ON and DCDC1	DCDC1 enabled
JP2	Between ON and DCDC2	DCDC2 enabled
JP3	Between ON and DCDC3	DCDC3 enabled
JP4	Between ON and LDO	LDO1 and LDO2 enabled

Table 2. TPS650250 EVM Factory Jumper Setup (continued)

Jumper	Shunt Location	
JP7	Between ON and VDD_ALIVE	VDD_ALIVE enabled
JP8	Between V-HI and DEF1	DCDC1 set to 3.3 V
JP6	Between PWM and MODE	
JP9	Between V-LOW and DEF2	DCDC2 set to 1.8 V

6 EVM Assembly Drawings and Layout

Figure 3 through Figure 8 show the design of the TPS650250EVM printed circuit board. The EVM has been designed using a 4-Layer, 1oz copper-clad circuit board 2.2" × 3.3"

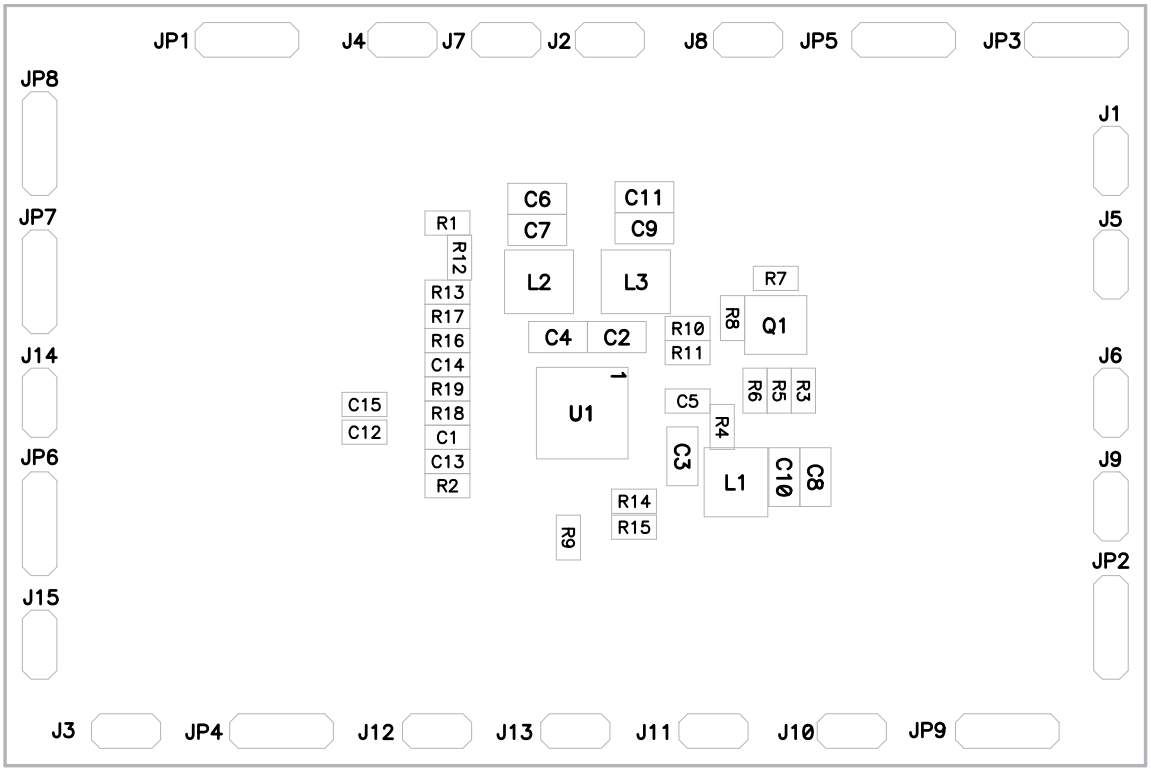

Figure 3. TPS650250 EVM Top Assembly

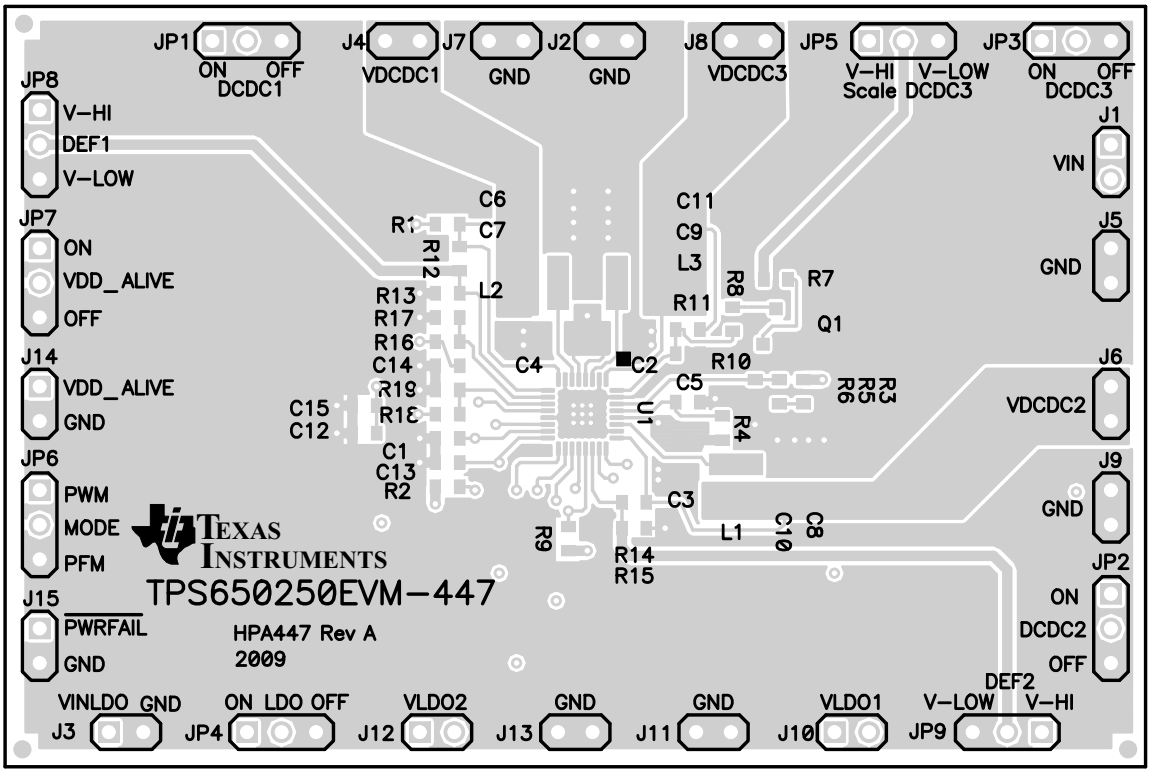

Figure 4. TPS650250EVM Top and Silkscreen (Viewed from Top)

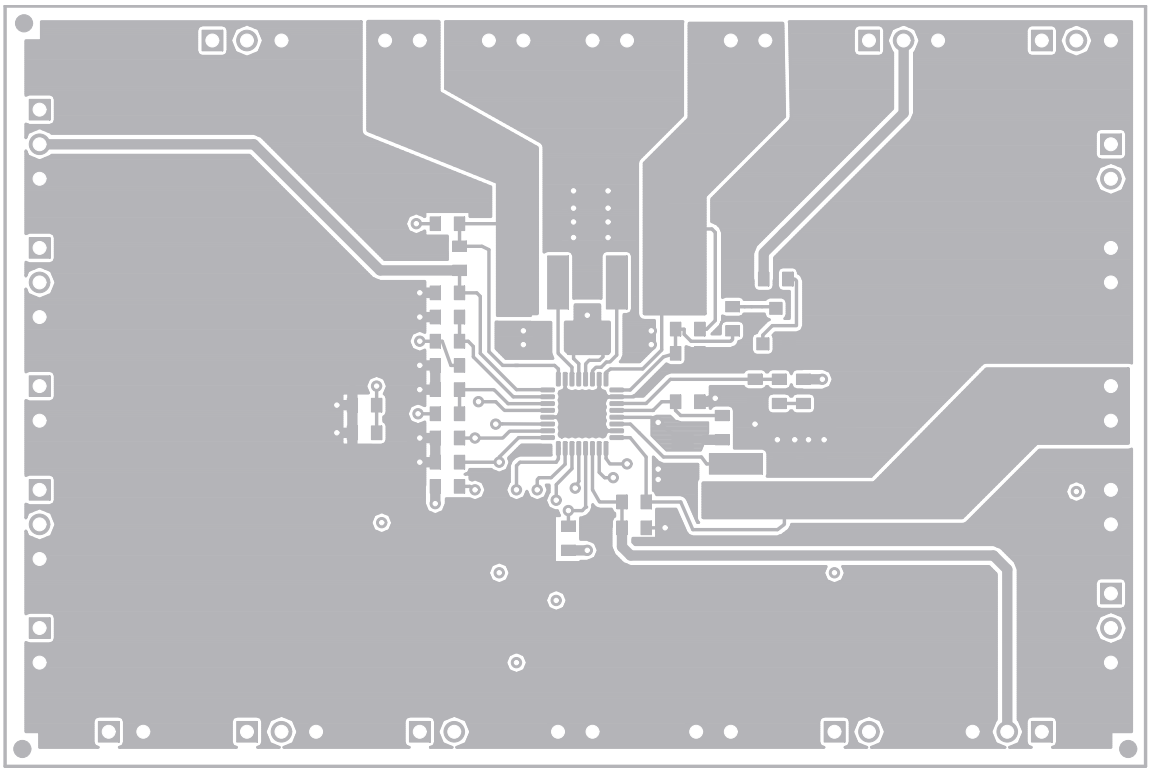

Figure 5. TPS650250EVM Top Copper

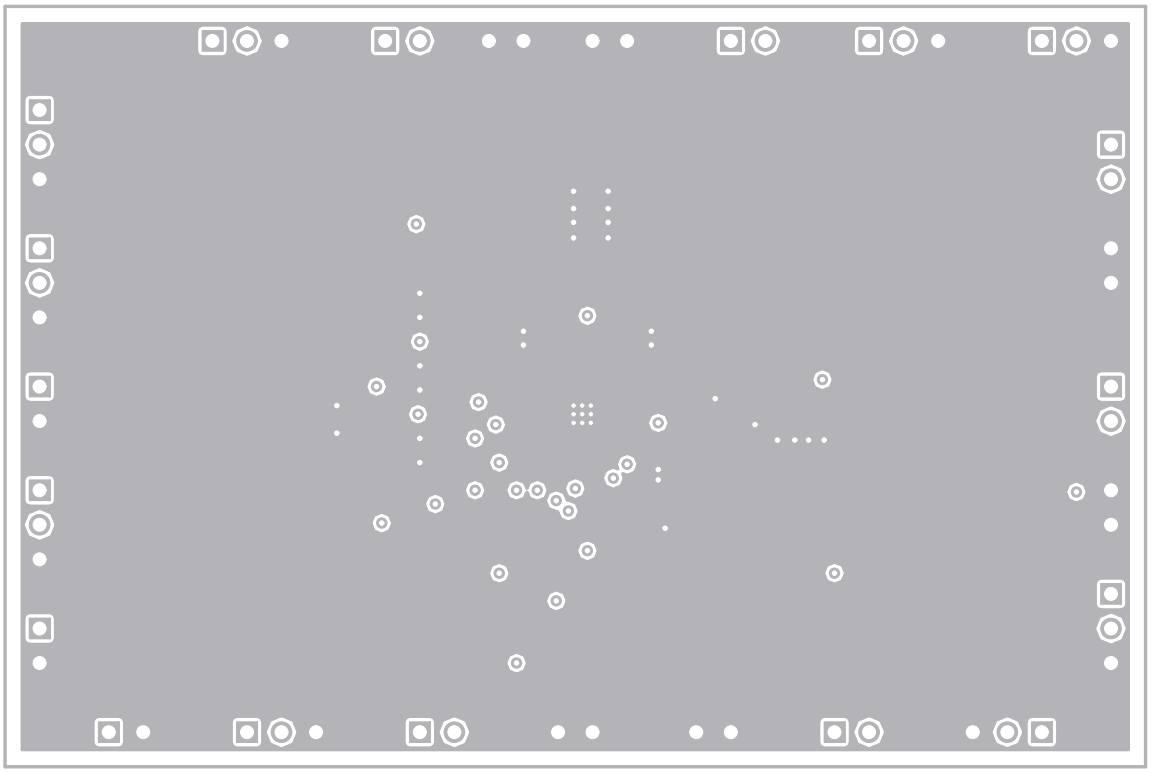

Figure 6. TPS650250 EVM Layer 2 (GND Plane)

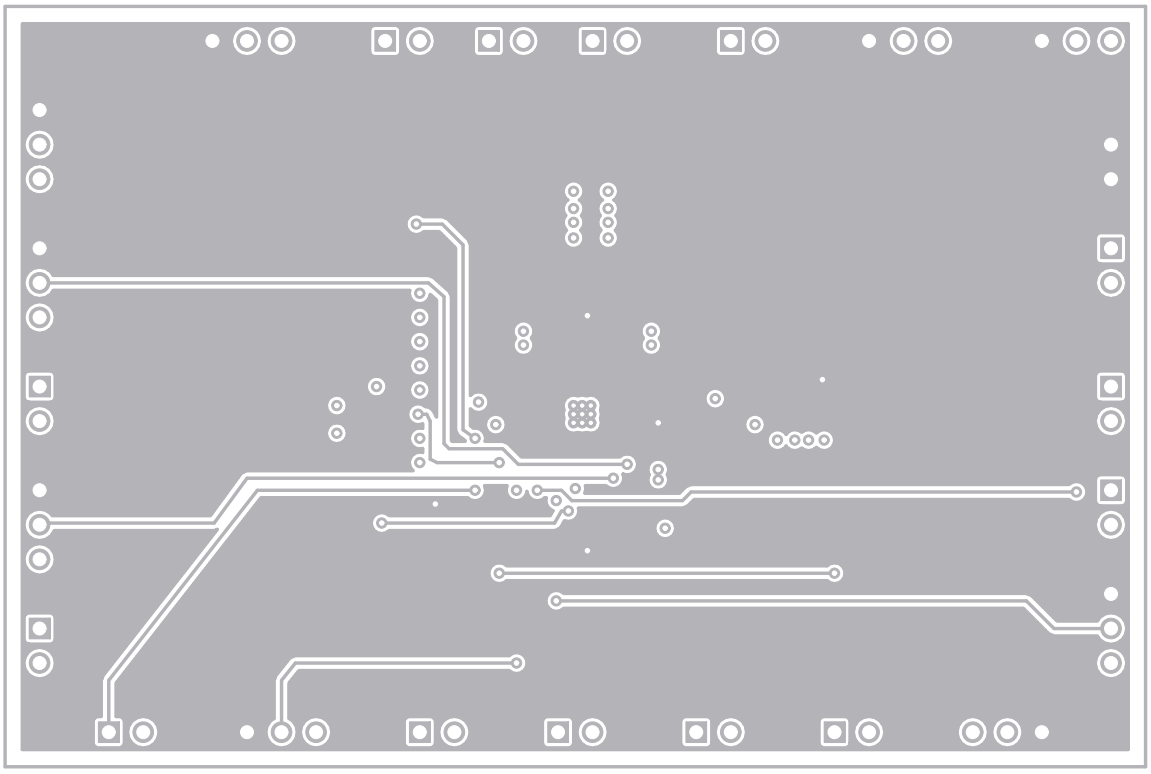

Figure 7. TPS650250EVM Internal Layer 3

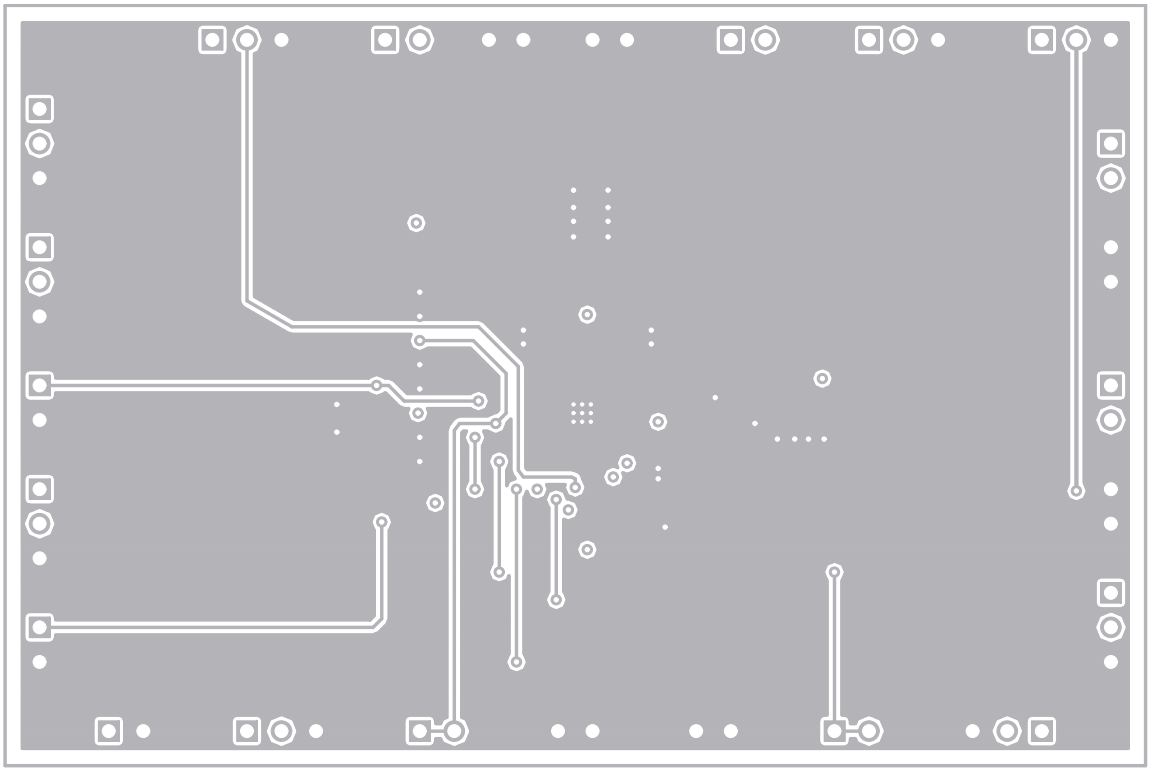

Figure 8. TPS650250 EVM Bottom Layer

6.1 Bill of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 2.

Table 3. TPS650250EVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C5	1.0µF	Capacitor, Ceramic, 6.3V, X5R,10%	0603	C1608X5R0J105K	TDK
4	C12, C13, C14, C15	2.2µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J225K	TDK
9	C2, C3, C4, C6, C7, C8, C9, C10, C11	10uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	C2012X5R0J106K	TDK
15	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
8	JP1, JP2, JP3, JP4, JP6, JP7, JP8, JP9		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
0	JP5	open	Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
2	L1, L3**	2.2µH	Inductor, SMT, 1.72A, 59milliohm	0.157 × 0.157 inch	VLCF4020T-2R2N1R7	TDK
1	L2**	3.3µH	Inductor, SMT, 1.52A, 78milliohm	0.157 × 0.157 inch	VLCF4020T-3R3N1R5	TDK
0	Q1	open	SOT23			
2	R1, R3	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R10, R11	182k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R16	60.4k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R17, R18	150k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R2, R12, R13, R14, R15	Open	Resistor, Chip, 1/16W, 1%	0603		
1	R4	1	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R5	1.21M	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	499k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7, R8	open	Resistor, Chip, 1/16W, 1%	0603		
2	R9, R19	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1**	TPS650250RHB	IC, Power Management ICs for Li-Ion Powered Systems	QFN-32	TPS650250RHB	TI
1	—		PCB, 2.2 In x 3.3 In x 0.064 In		HPA447	Any
8	—		Shunt, 100-mil, Black	0.100	929950-00	3M

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

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