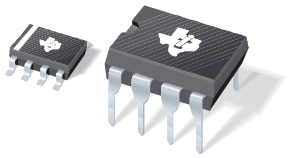


EXTENDED COMMON-MODE RS-485 TRANSCEIVERS

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Common-Mode Voltage Range (−20 V to 25 V) More Than Doubles TIA/EIA-485 Requirement**
- **Receiver Equalization Extends Cable Length, Signaling Rate (HVD23, HVD24)**
- **Reduced Unit-Load for up to 256 Nodes**
- **Bus I/O Protection to Over 16-kV HBM**
- **Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions**
- **Low Standby Supply Current 1.5-μA Max**
- **More Than 100 mV Receiver Hysteresis**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Long Cable Solutions**
  - **Factory Automation**
  - **Security Networks**
  - **Building HVAC**
- **Severe Electrical Environments**
  - **Electrical Power Inverters**
  - **Industrial Drives**
  - **Avionics**

DESCRIPTION

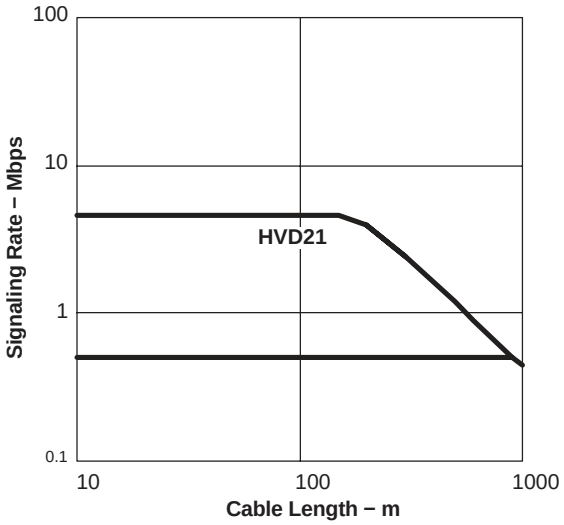
The SN65HVD21M offers performance exceeding typical RS−485 devices. In addition to meeting all requirements of the TIA/EIA−485−A standard, the HVD2x family operates over an extended range of common-mode voltage, and has features such as high ESD protection, wide receiver hysteresis, and failsafe operation. This family of devices is ideally suited for long-cable networks, and other applications where the environment is too harsh for ordinary transceivers.

The SN65HVD21M is designed for bidirectional data transmission on multipoint twisted-pair cables. Example applications are digital motor controllers, remote sensors and terminals, industrial process control, security stations, and environmental control systems.

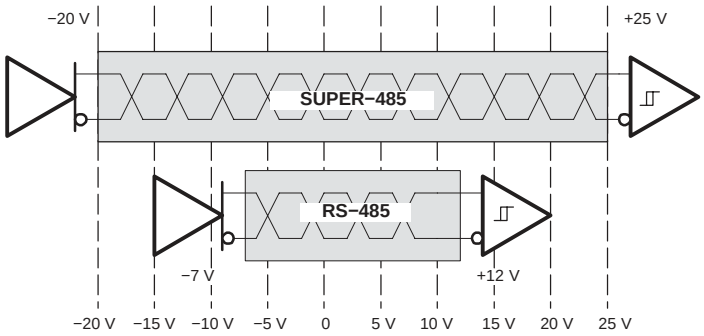
The SN65HVD21M combines a 3-state differential driver and a differential receiver, which operates from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a differential bus port that offers minimum loading to the bus. This port features an extended common-mode voltage range making the device suitable for multipoint applications over long cable runs.

The SN65HVD21M allows up to 256 connected nodes at moderate data rates (up to 5 Mbps). The driver output slew rate is controlled to provide reliable switching with shaped transitions which reduce high-frequency noise emissions.

APPLICATION SPACE



SN65HVDM21 Operates Over a Wider Common-Mode Voltage Range



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (continued)

The receiver also includes a failsafe circuit that provides a high-level output within 250 μs after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or the absence of any active transmitters on the bus. This feature prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling.

The SN65HVD21M is characterized for operation over the temperature range of −55°C to 125°C.

PRODUCT SELECTION GUIDE

PART NUMBERS	CABLE LENGTH AND SIGNALING RATE(1)	NODES	MARKING
SN65HVD21MDREP	Up to 150 m at 5 Mbps (with slew rate limit)	Up to 256	D: V21MEP

(1) Distance and signaling rate predictions based upon Belden 3105A cable and 15% eye pattern jitter.

AVAILABLE OPTIONS

PLASTIC SMALL-OUTLINE(1) D PACKAGE (JEDEC MS-012)
SN65HVD21MDREP

(1) Add R suffix for taped and reeled carriers.

DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	H	L

H = high level, L= low level, X = don't care, Z = high impedance (off), ? = indeterminate

RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
$0.2\ V \le V_{ID}$	L	H
$-0.2\ V < V_{ID} < 0.2\ V$	L	H (see Note A)
$V_{ID} \le -0.2\ V$	L	L
X	H	Z
X	OPEN	Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

H = high level, L= low level, Z = high impedance (off)

NOTE A: If the differential input V_{ID} remains within the transition range for more than 250 μs, the integrated failsafe circuitry detects a bus fault, and set the receiver output to a high state. See Figure 15.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

Supply voltage(2), V_{CC}			−0.5 V to 7 V
Voltage at any bus I/O terminal			−27 V to 27 V
Voltage input, transient pulse, A and B, (through 100 Ω, see Figure 16)			−60 V to 60 V
Voltage input at any D, DE or $\overline{RE}$ terminal			−0.5 V to V_{CC}+ 0.5 V
Receiver output current, I_O			−10 mA to 10 mA
Electrostatic discharge	Human Body Model(3)	A, B, GND	16 kV
		All pins	5 kV
	Charged-Device Model(4)	All pins	1.5 kV
	Machine Model(5)	All pins	200 V
Continuous total power dissipation			See Power Dissipation Rating Table
Junction temperature, T_J			150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(3) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	Low-K(1)	577 mW	4.62 mW/°C	369 mW	300 mW
	High-K(2)	913 mW	7.3 mW/°C	584 mW	474 mW

(1) In accordance with the Low-K thermal metric definitions of EIA/JESD51−3.
(2) In accordance with the High-K thermal metric definitions of EIA/JESD51−7.
(3) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		VALUE	UNITS
θ_{JB}	Junction-to-board thermal resistance			86.2	°C/W
θ_{JC}	Junction-to-case thermal resistance			47.1	
P_D Device power dissipation	Typical	V_{CC} = 5 V, T_J = 25°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	5 Mbps	260	mW
	Worst case	V_{CC} = 5.5 V, T_J = 125°C, R_L = 54 Ω, C_L = 50 pF, C_L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	5 Mbps	342	
T_{SD}	Thermal shut-down junction temperature			170	°C

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Voltage at any bus I/O terminal	A, B	−20		25	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	
Differential input voltage, V_{ID}	A with respect to B	−25		25	V
Output current	Driver	−110		110	mA
	Receiver	−8		8	
Operating free-air temperature, T_A(1)		−55		125	°C
Junction temperature, T_J		−55		130	°C

(1) Maximum free-air temperature operation is allowed as long as the device recommended junction temperature is not exceeded.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA	−1.5	0.75		V
V_O	Open-circuit output voltage	A or B, No load	0		V_{CC}	V
$\lvert V_{OD(SS)} \rvert$	Steady-state differential output voltage magnitude	No load (open circuit)	3.3	4.2	V_{CC}	V
		R_L = 54 Ω, See Figure 1	1.8	2.5		
		With common-mode loading, See Figure 2	1.8			
$\Delta\lvert V_{OD(SS)} \rvert$	Change in steady-state differential output voltage between logic states	See Figure 1 and Figure 3	−0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 1	2.1	2.5	2.9	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage, $V_{OC(H)} - V_{OC(L)}$	See Figure 1 and Figure 4	−0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage, $V_{OC(MAX)} - V_{OC(MIN)}$	R_L = 54 Ω, C_L = 50 pF, See Figure 1 and Figure 4		0.35		V
$V_{OD(RING)}$	Differential output voltage over and under shoot	R_L = 54 Ω, C_L = 50 pF, See Figure 5			10%	
I_I	Input current	D, DE	−100		100	µA
$I_{O(OFF)}$	Output current with power off	V_{CC} < = 2.5 V	−100		125	µA
I_{OZ}	High impedance state output current	DE at 0 V				
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V, See Figure 9	−270		250	mA
C_{OD}	Differential output capacitance		See receiver C_I			

(1) All typical values are at V_{CC} = 5 V and 25°C.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Differential output propagation delay, high-to-low	R_L = 54 Ω, C_L = 50 pF, See Figure 3	15	32	60	ns
t_r	Differential output rise time	R_L = 54 Ω, C_L = 50 pF, See Figure 3	15	40	60	ns
t_f	Differential output fall time					
t_{PZH}	Propagation delay time, high impedance-to-high level output	$\overline{RE}$ at 0 V, See Figure 6			140	ns
t_{PHZ}	Propagation delay time, high level-output-to-high impedance					
t_{PZL}	Propagation delay time, high impedance-to-low level output	$\overline{RE}$ at 0 V, See Figure 7			140	ns
t_{PLZ}	Propagation delay time, low level output-to-high impedance					
$t_{d(standby)}$	Time from an active differential output to standby	$\overline{RE}$ at V_{CC}, See Figure 8			4	µs
$t_{d(wake)}$	Wake-up time from standby to an active differential output				10	µs
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$				10	ns

(1) All typical values are at V_{CC} = 5 V and 25°C.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{IT(+)}$	Positive-going differential input voltage threshold	See Figure 10	V_O = 2.4 V, I_O = −8 mA		60	200	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		V_O = 0.4 V, I_O = 8 mA	−200	−60		
V_{HYS}	Hysteresis voltage (V_{IT+} − V_{IT-})			100	130		mV
$V_{IT(F+)}$	Positive-going differential input failsafe voltage threshold	See Figure 15	V_{CM} = −7 V to 12 V	40	120	200	mV
			V_{CM} = −20 V to 25 V		120	250	
$V_{IT(F-)}$	Negative-going differential input failsafe voltage threshold	See Figure 15	V_{CM} = −7 V to 12 V	−200	−120	−40	mV
			V_{CM} = −20 V to 25 V	−250	−120		
V_{IK}	Input clamp voltage	I_I = −18 mA		−1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −8 mA, See Figure 11		4			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 11				0.4	V
$I_{I(BUS)}$	Bus input current (power on or power off)	V_I = −7 to 12 V, Other input = 0 V		−100		125	µA
I_I	Input current	$\overline{RE}$		−100		125	µA
R_I	Input resistance			96			kΩ
C_{ID}	Differential input capacitance	V_{ID} = 0.5 + 0.4 sine (2π x 1.5 x 10^6t)				20	pF

(1) All typical values are at 25°C.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions

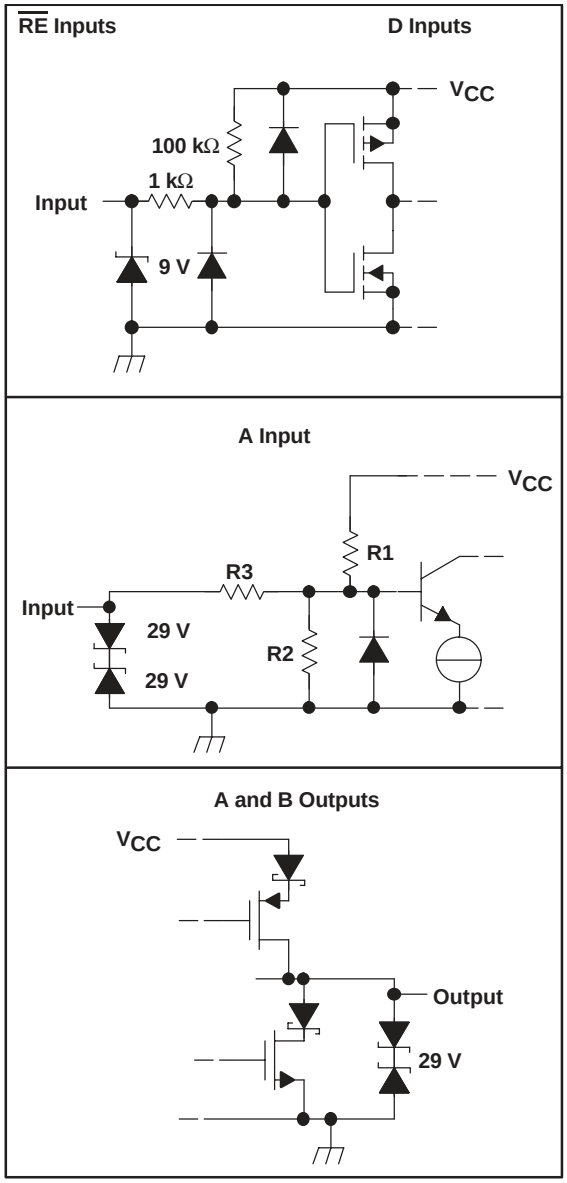
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level output	See Figure 11		25	70	ns
t_r	Receiver output rise time	See Figure 11		2	7	ns
t_f	Receiver output fall time					
t_{PZH}	Receiver output enable time to high level	See Figure 12		90	145	ns
t_{PHZ}	Receiver output disable time from high level			16	45	
t_{PZL}	Receiver output enable time to low level	See Figure 13		90	145	ns
t_{PLZ}	Receiver output disable time from low level			16	45	
$t_{r(standby)}$	Time from an active receiver output to standby	See Figure 14, DE at 0 V			4	µs
$t_{r(wake)}$	Wake-up time from standby to an active receiver output				11	
$t_{sk(p)}$	Pulse skew | t_{PLH} − t_{PHL} |				7	ns
$t_{p(set)}$	Delay time, bus fail to failsafe set	See Figure 15, pulse rate = 1 kHz		250	385	µs
$t_{p(reset)}$	Delay time, bus recovery to failsafe reset				70	ns

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	Driver enabled (DE at V_{CC}), Receiver enabled (RE at 0 V) No load, V_I = 0 V or V_{CC}		8	15	mA
		Driver enabled (DE at V_{CC}), Receiver disabled (RE at V_{CC}) No load, V_I = 0 V or V_{CC}		7	14	mA
		Driver disabled (DE at 0 V), Receiver enabled (RE at 0 V) No load		5	9	mA
		Driver disabled (DE at 0 V), Receiver disabled (RE at V_{CC}) D open			1.5	µA

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
HVD21	36 kΩ	180 kΩ

PARAMETER MEASUREMENT INFORMATION

NOTES:

Test load capacitance includes probe and jig capacitance (unless otherwise specified).

Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle, Z_O = 50 Ω (unless otherwise specified)

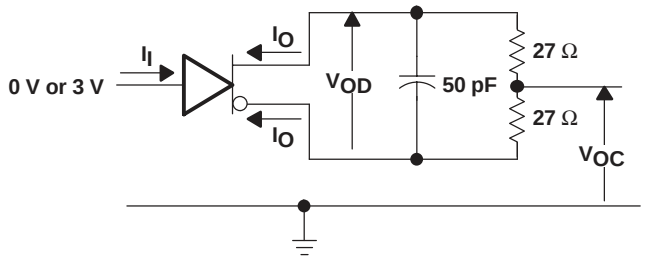


Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

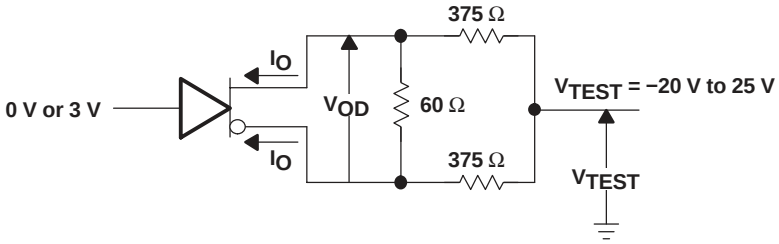


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

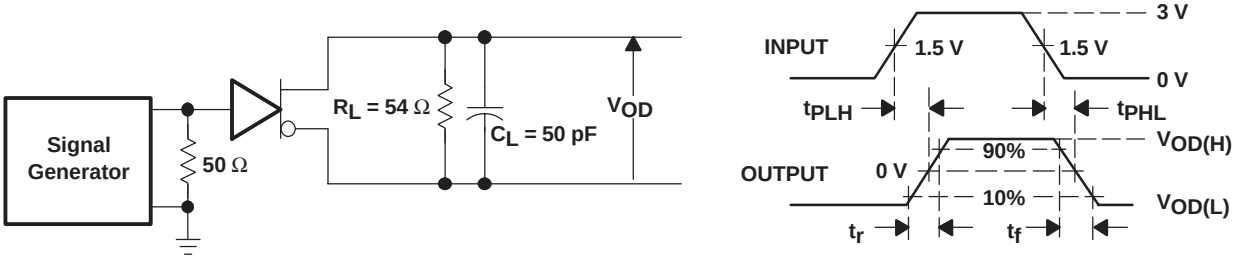


Figure 3. Driver Switching Test Circuit and Waveforms

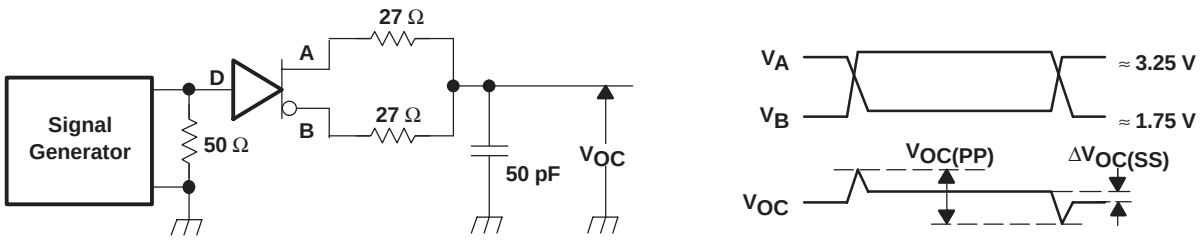
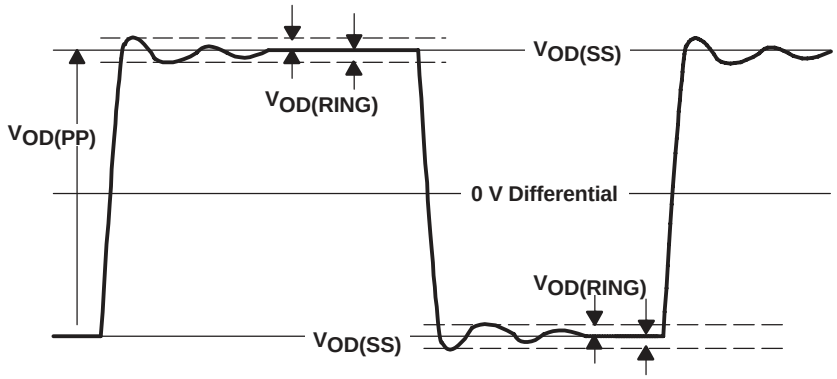


Figure 4. Driver V_{OC} Test Circuit and Waveforms



NOTE: $V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

Figure 5. $V_{OD(RING)}$ Waveform and Definitions

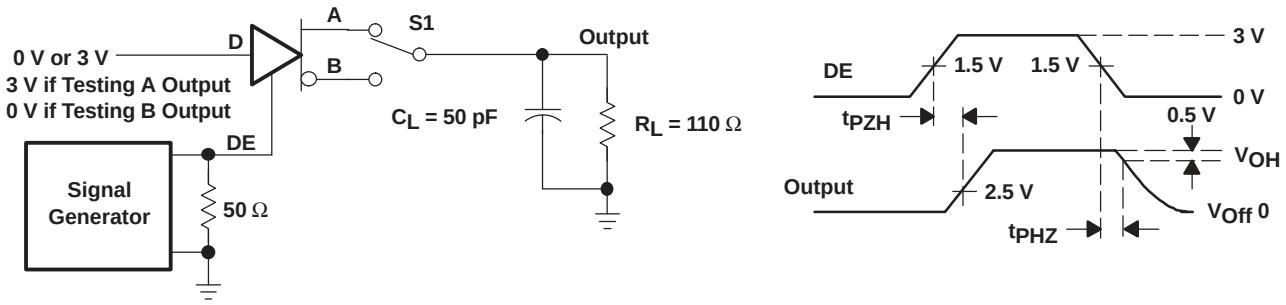


Figure 6. Driver Enable/Disable Test, High Output

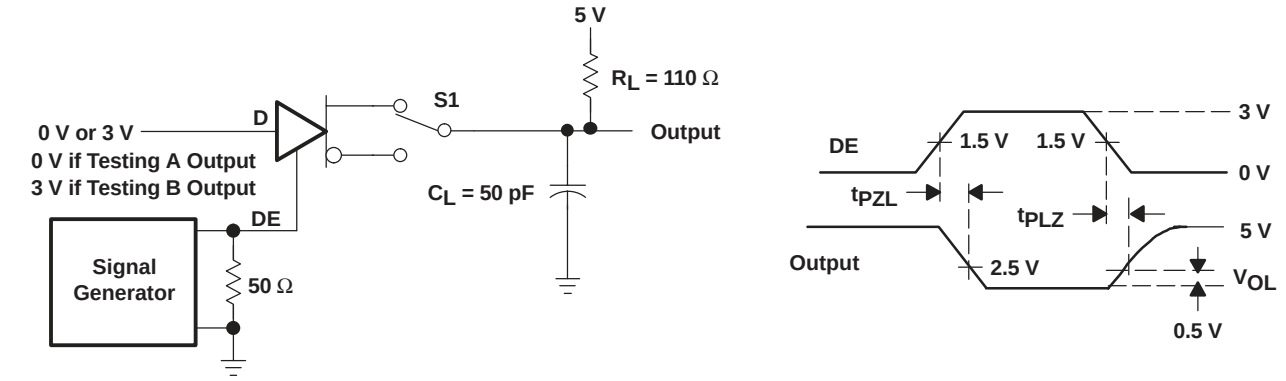


Figure 7. Driver Enable/Disable Test, Low Output

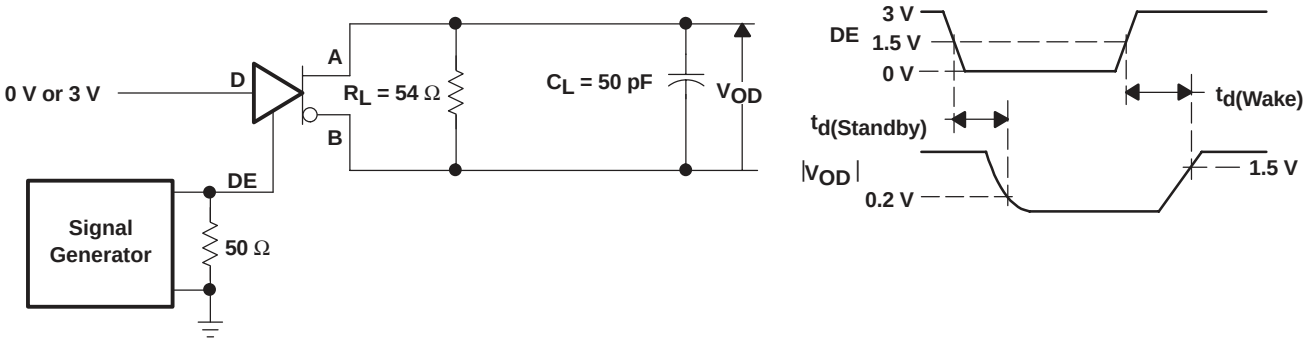


Figure 8. Driver Standby/Wake Test Circuit and Waveforms

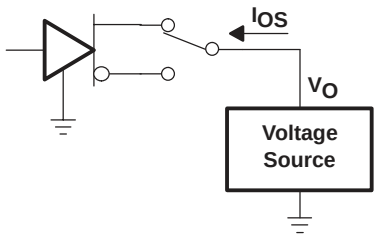


Figure 9. Driver Short-Circuit Test

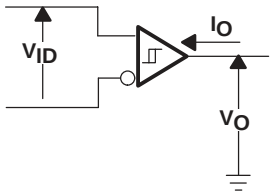


Figure 10. Receiver DC Parameter Definitions

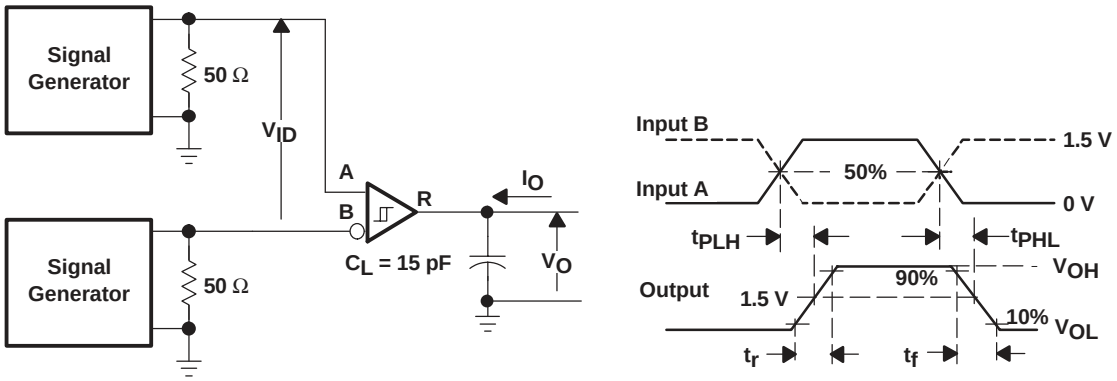


Figure 11. Receiver Switching Test Circuit and Waveforms

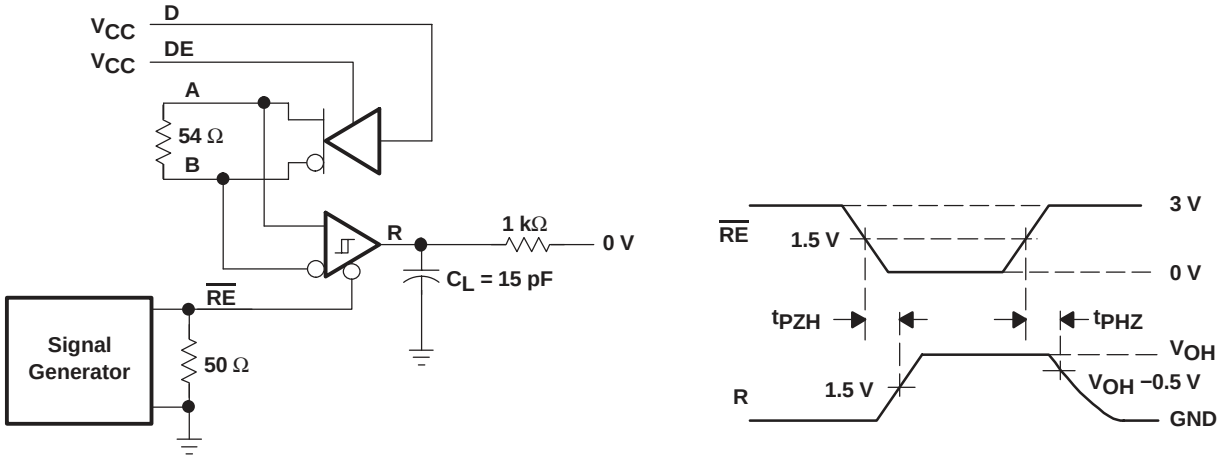


Figure 12. Receiver Enable Test Circuit and Waveforms, Data Output High

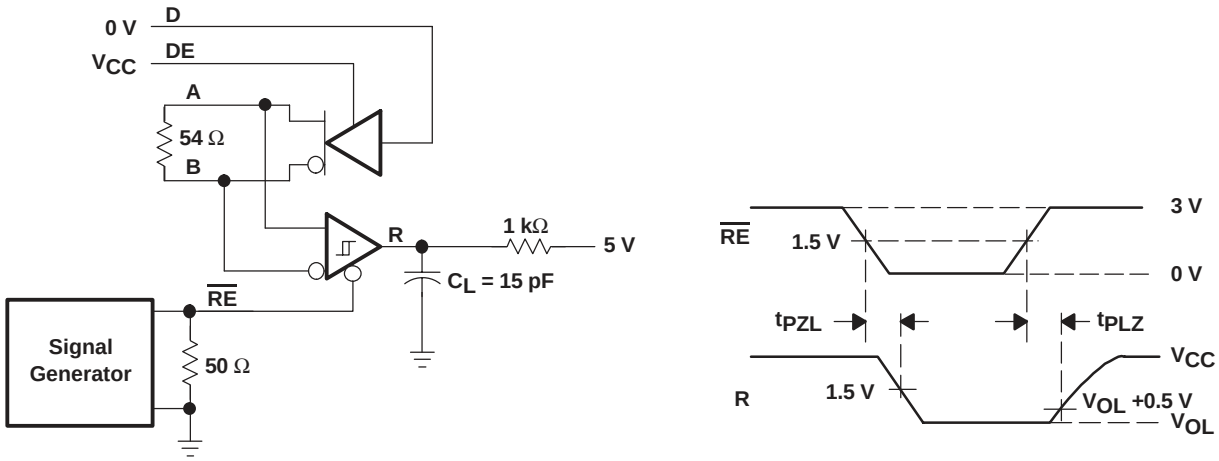


Figure 13. Receiver Enable Test Circuit and Waveforms, Data Output Low

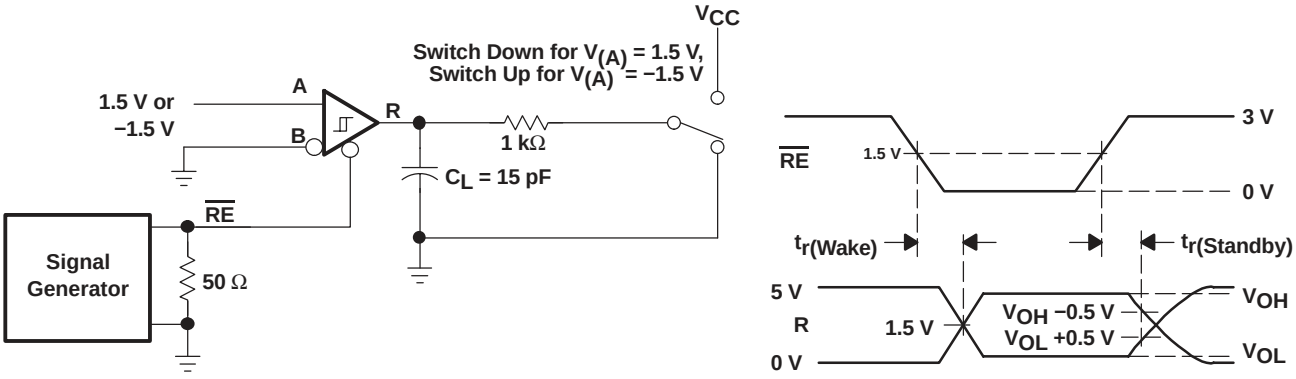


Figure 14. Receiver Standby and Wake Test Circuit and Waveforms

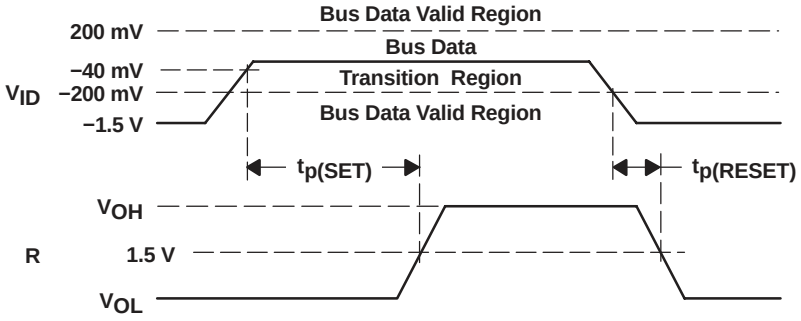


Figure 15. Receiver Active Failsafe Definitions and Waveforms

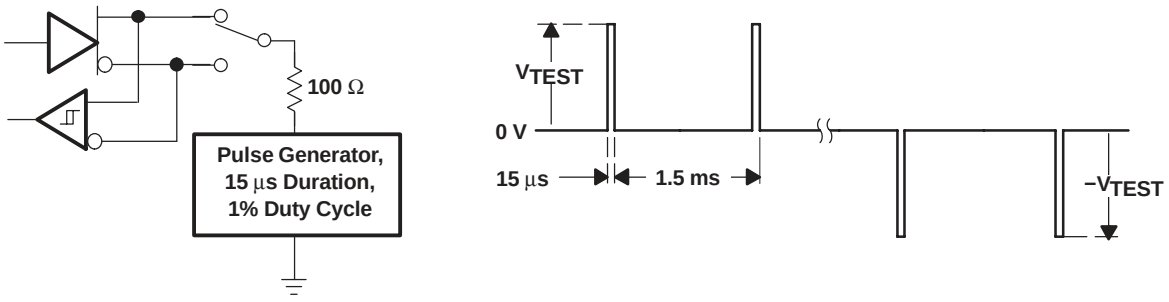
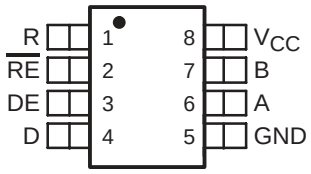


Figure 16. Test Circuit and Waveforms, Transient Overvoltage Test

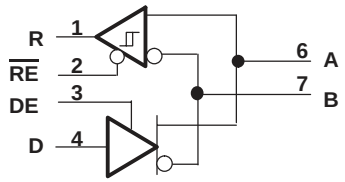
PIN ASSIGNMENTS

D or P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM

POSITIVE LOGIC



TYPICAL CHARACTERISTICS

BUS PIN CURRENT
vs
BUS PIN VOLTAGE

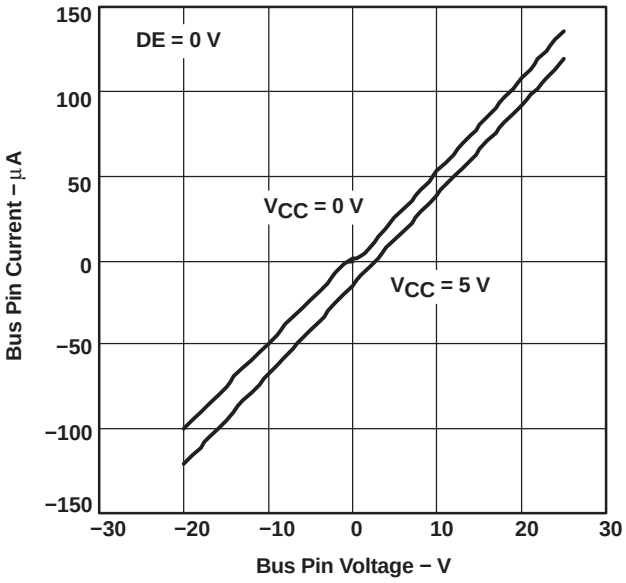


Figure 17

SUPPLY CURRENT vs SIGNALING RATE

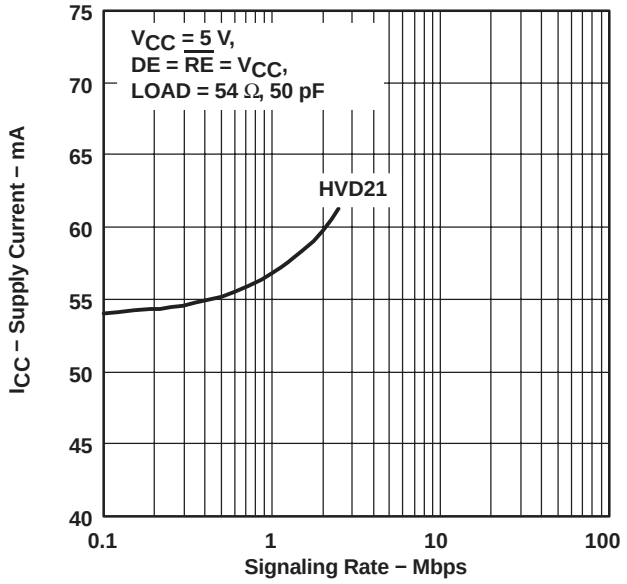


Figure 18

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs DRIVER LOAD CURRENT

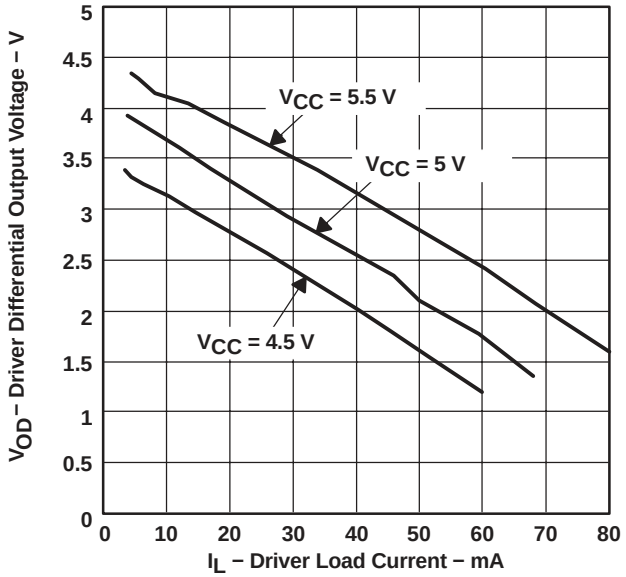


Figure 19

RECEIVER OUTPUT VOLTAGE vs DIFFERENTAL INPUT VOLATGE

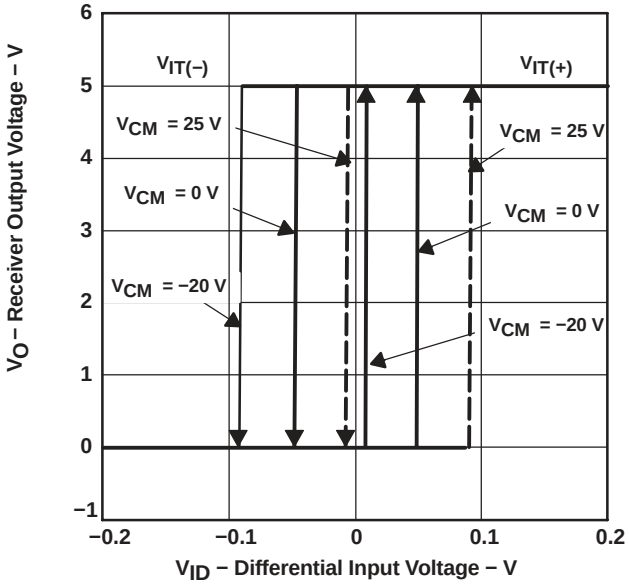


Figure 20

PEAK-TO-PEAK JITTER vs CABLE LENGTH

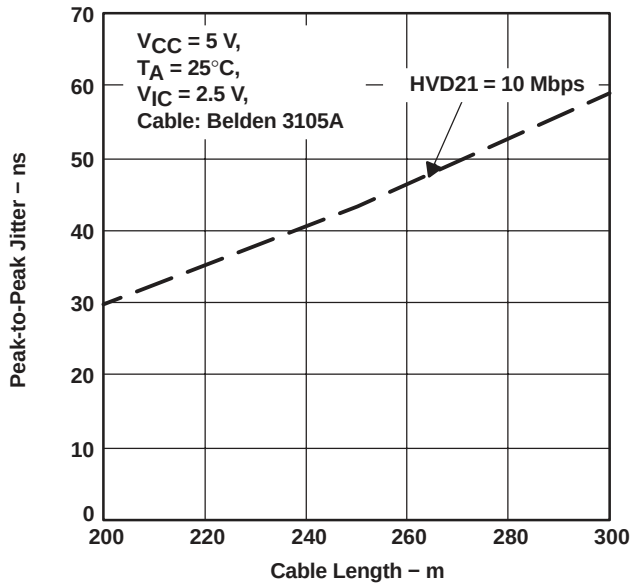


Figure 21

APPLICATION INFORMATION

THEORY OF OPERATION

The SN65HVD21M integrates a differential receiver and differential driver with additional features for improved performance in electrically-noisy, long-cable, or other fault-intolerant applications.

The receiver hysteresis (typically 130 mV) is much larger than found in typical RS-485 transceivers. This helps reject spurious noise signals which would otherwise cause false changes in the receiver output state.

Slew rate limiting on the driver outputs reduces the high-frequency content of signal edges. This decreases reflections from bus discontinuities, and allows longer stub lengths between nodes and the main bus line. Designers should consider the maximum signaling rate and cable length required for a specific application, and choose the transceiver best matching those requirements.

When DE is low, the differential driver is disabled, and the A and B outputs are in high-impedance states. When DE is high, the differential driver is enabled, and drives the A and B outputs according to the state of the D input.

When $\overline{RE}$ is high, the differential receiver output buffer is disabled, and the R output is in a high-impedance state. When $\overline{RE}$ is low, the differential receiver is enabled, and the R output reflects the state of the differential bus inputs on the A and B pins.

If both the driver and receiver are disabled, (DE low and $\overline{RE}$ high) then all nonessential circuitry, including auxiliary functions such as failsafe and receiver equalization is placed in a low-power standby state. This reduces power consumption to less than 5 μW. When either enable input is asserted, the circuitry again becomes active.

In addition to the primary differential receiver, these devices incorporate a set of comparators and logic to implement an active receiver failsafe feature. These components determine whether the differential bus signal is valid. Whenever the differential signal is close to zero volts (neither high nor low), a timer initiates, If the differential input remains within the transition range for more than 250 μs, the timer expires and set the receiver output to the high state. If a valid bus input (high or low) is received at any time, the receiver output reflects the valid bus state, and the timer is reset.

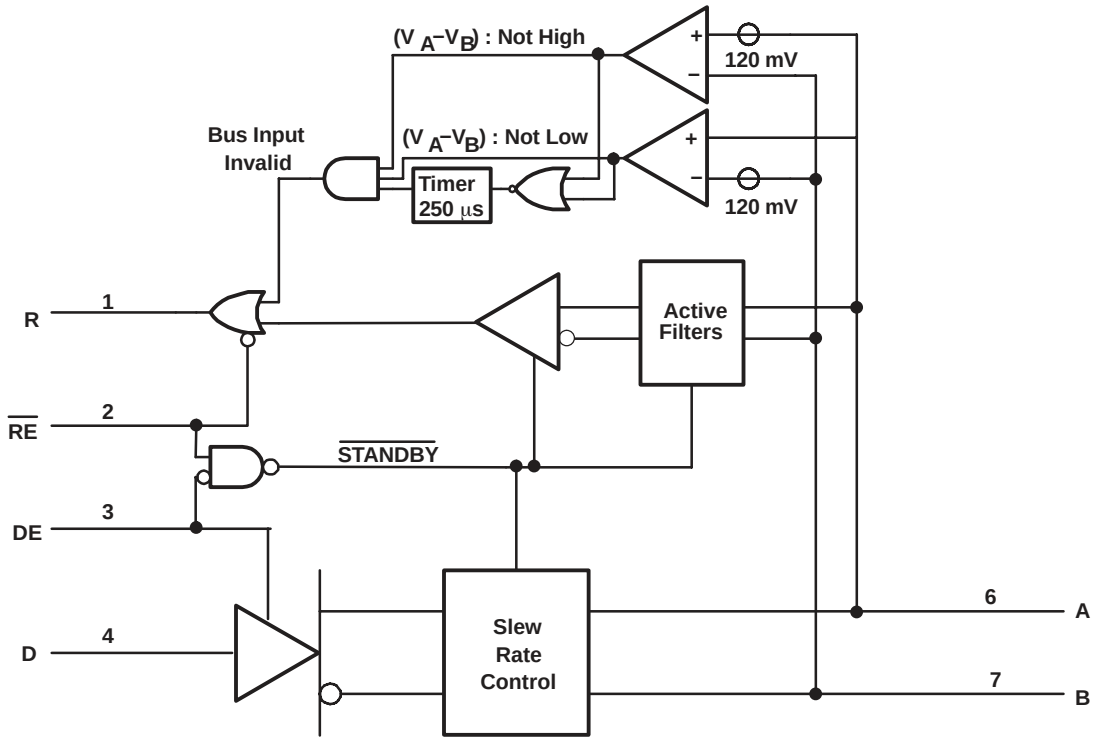


Figure 22. Function Block Diagram

$H(s) = k_0\left[(1-k_1)+\frac{k_1p_1}{(s+p_1)}\right]\left[(1-k_2)+\frac{k_2p_2}{(s+p_2)}\right]\left[(1-k_3)+\frac{k_3p_3}{(s+p_3)}\right]$	k0 (DC loss)	p1 (MHz)	k1	p2 (MHz)	k2	p3 (MHz)	k3
Similar to 160m of Belden 3105A	0.95	0.25	0.3	3.5	0.5	15	1
Similar to 250m of Belden 3105A	0.9	0.25	0.4	3.5	0.7	12	1
Similar to 500m of Belden 3105A	0.8	0.25	0.6	2.2	1	8	1
Similar to 1000m of Belden 3105A	0.6	0.3	1	3	1	6	1

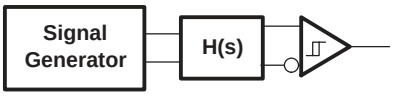


Figure 23. Cable Attenuation Model for Jitter Measurements

NOISE CONSIDERATIONS FOR EQUALIZED RECEIVERS

The simplest way of overcoming the effects of cable losses is to increase the sensitivity of the receiver. If the maximum attenuation of frequencies of interest is 20 dB, increasing the receiver gain by a factor of ten compensates for the cable. However, this means that both signal and noise are amplified. Therefore, the receiver with higher gain is more sensitive to noise and it is important to minimize differential noise coupling to the equalized receiver.

Differential noise is crated when conducted or radiated noise energy generates more voltage on one line of the differential pair than the other. For this to occur from conducted or electric far-field noise, the impedance to ground of the lines must differ.

For noise frequency out to 50 MHz, the input traces can be treated as a lumped capacitance if the receiver is approximately 10 inches or less from the connector. Therefore, matching impedance of the lines is accomplished by matching the lumped capacitance of each.

The primary factors that affect the capacitance of a trace are in length, thickness, width, dielectric material, distance from the signal return path, stray capacitance, and proximity to other conductors. It is difficult to match each of the variables for each line of the differential pair exactly, but a reasonable effort to do so keeps the lines balanced and less susceptible to differential noise coupling.

Another source of differential noise is from near-field coupling. In this situation, an assumption of equal noise-source impedance cannot be made as in the far-field. Familiarly known as crosstalk, more energy from a nearby signal is coupled to one line of the differential pair. Minimization of this differential noise is accomplished by keeping the signal pair close together and physical separation from high-voltage, high-current, or high-frequency signals.

In summary, follow these guidelines in board layout for keeping differential noise to a minimum.

- Keep the differential input traces short.
- Match the length, physical dimensions, and routing of each line of the pair.
- Keep the lines close together.
- Match components connected to each line.
- Separate the inputs from high-voltage, high-frequency, or high-current signals.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD21MDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	V21MEP	Samples
SN65HVD21MDREPG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	V21MEP	Samples
V62/06615-01XE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	V21MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

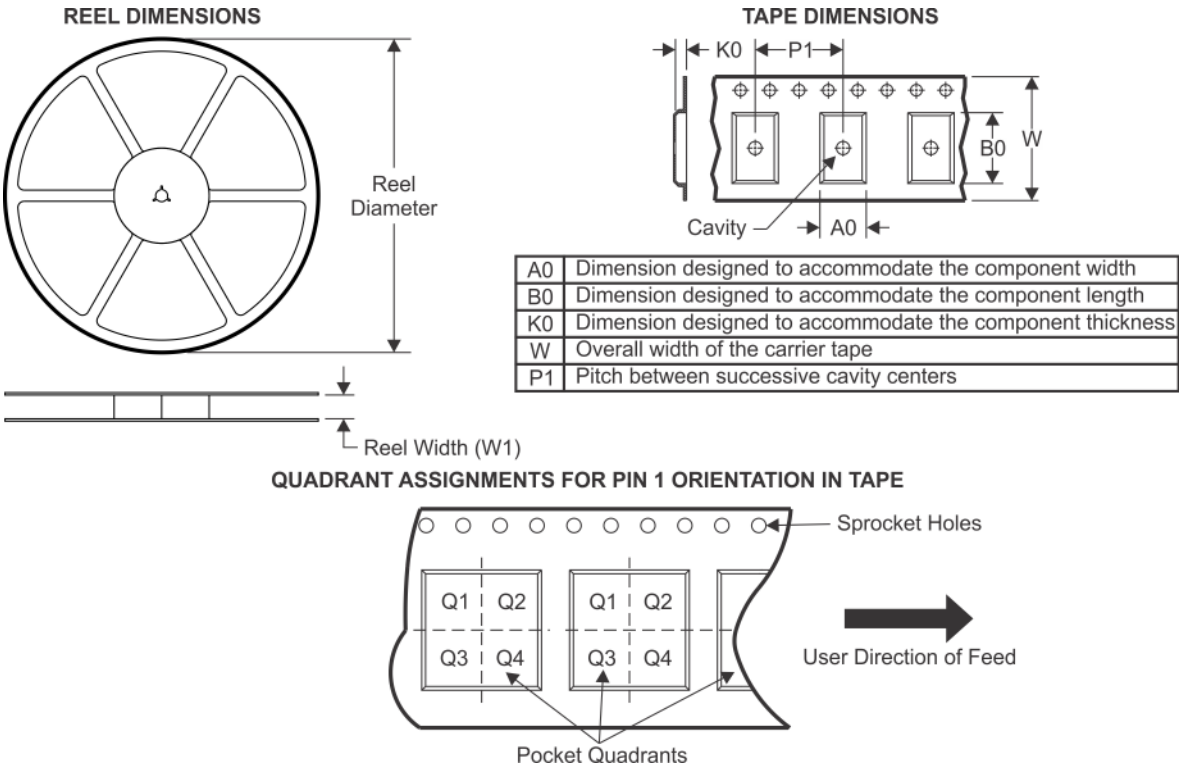
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

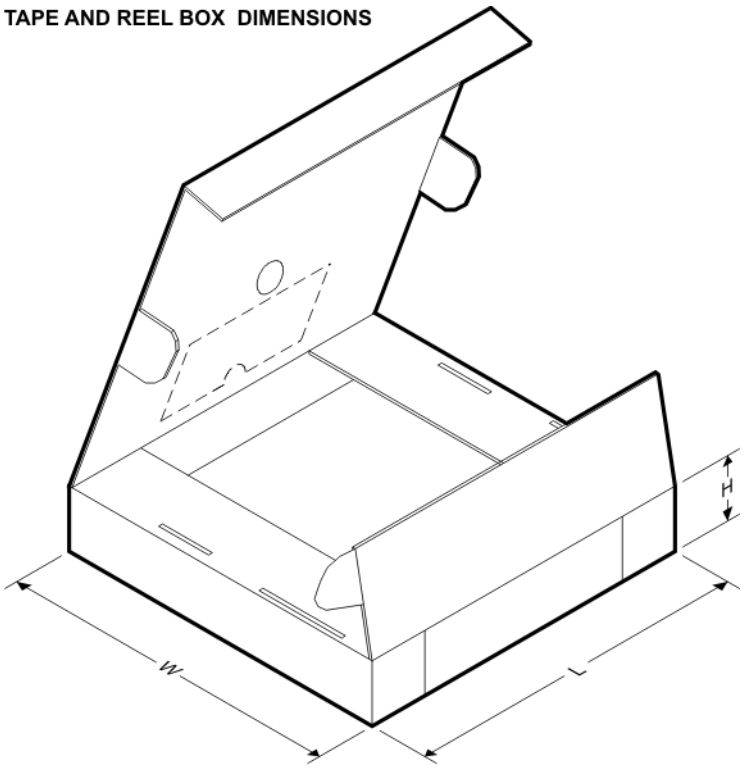


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

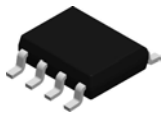
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD21MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD21MDREP	SOIC	D	8	2500	340.5	336.1	25.0

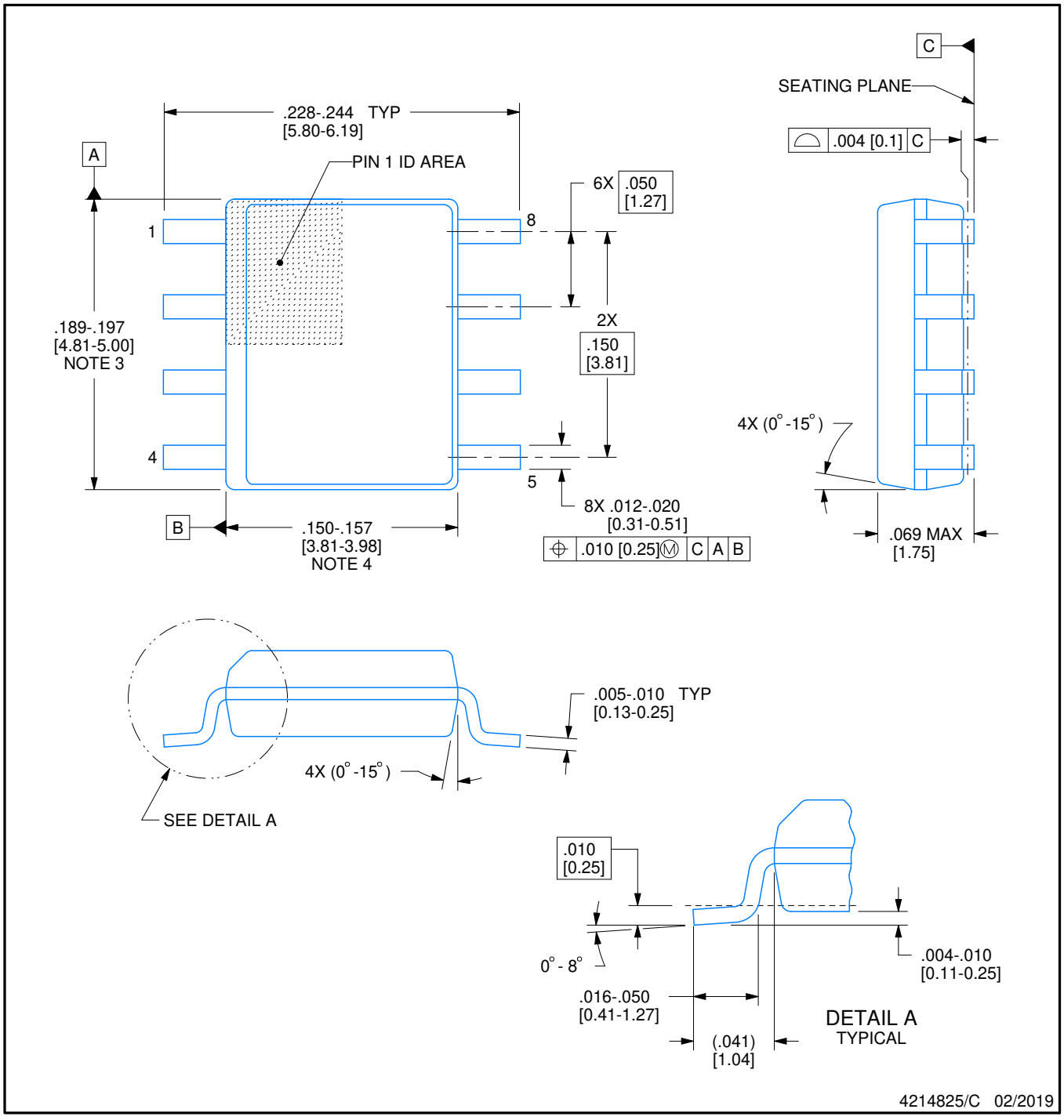


PACKAGE OUTLINE

D0008A

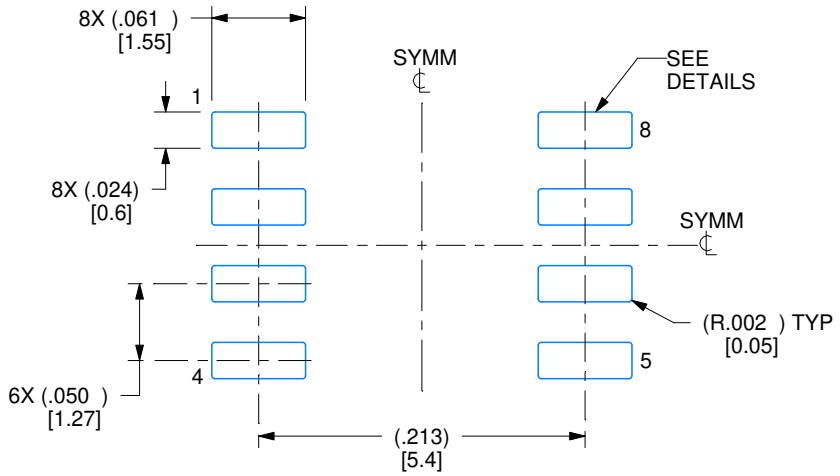
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

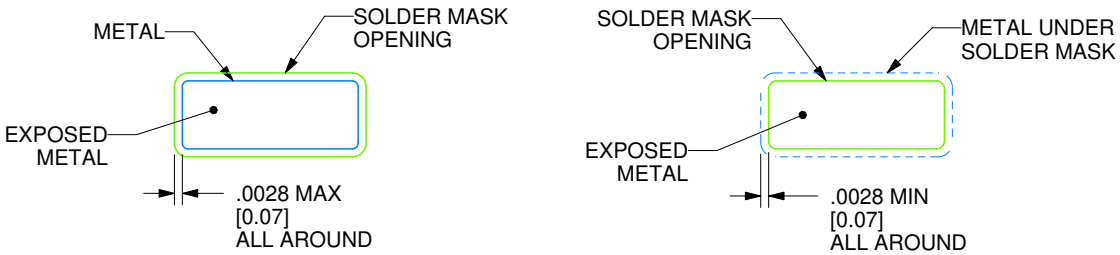


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

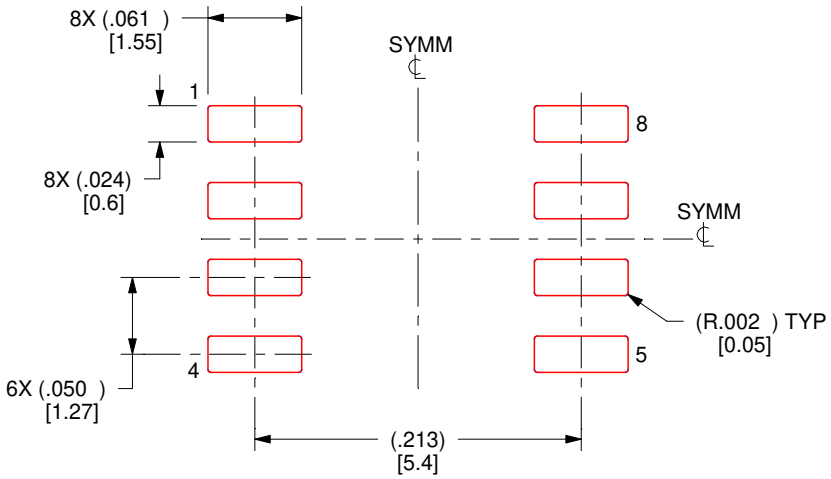
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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