TDA7563

MULTIFUNCTION QUAD POWER AMPLIFIER WITH BUILT-IN DIAGNOSTICS FEATURES

- DMOS POWER OUTPUT
- NON-SWITCHING HI-EFFICIENCY
- HIGH OUTPUT POWER CAPABILITY 4x28W/ 4Ω @ 14.4V, 1KHZ, 10% THD, 4x40W EIAJ
- MAX. OUTPUT POWER 4x72W/2Ω
- FULL I^{2}C BUS DRIVING:
  - ST-BY
  - INDEPENDENT FRONT/REAR SOFT PLAY/ MUTE
  - SELECTABLE GAIN 30dB
  - 16dB (FOR LOW NOISE LINE OUTPUT FUNCTION)
  - HIGH EFFICIENCY ENABLE/DISABLE
  - I^{2}C BUS DIGITAL DIAGNOSTICS
- FULL FAULT PROTECTION
- DC OFFSET DETECTION
- FOUR INDEPENDENT SHORT CIRCUIT PROTECTION
- CLIPPING DETECTOR PIN WITH SELECTABLE THRESHOLD (2%/10%)
- ST-BY/MUTE PIN
- LINEAR THERMAL SHUTDOWN
- ESD PROTECTION

MULTIPOWER BCD TECHNOLOGY

MOSFET OUTPUT POWER STAGE

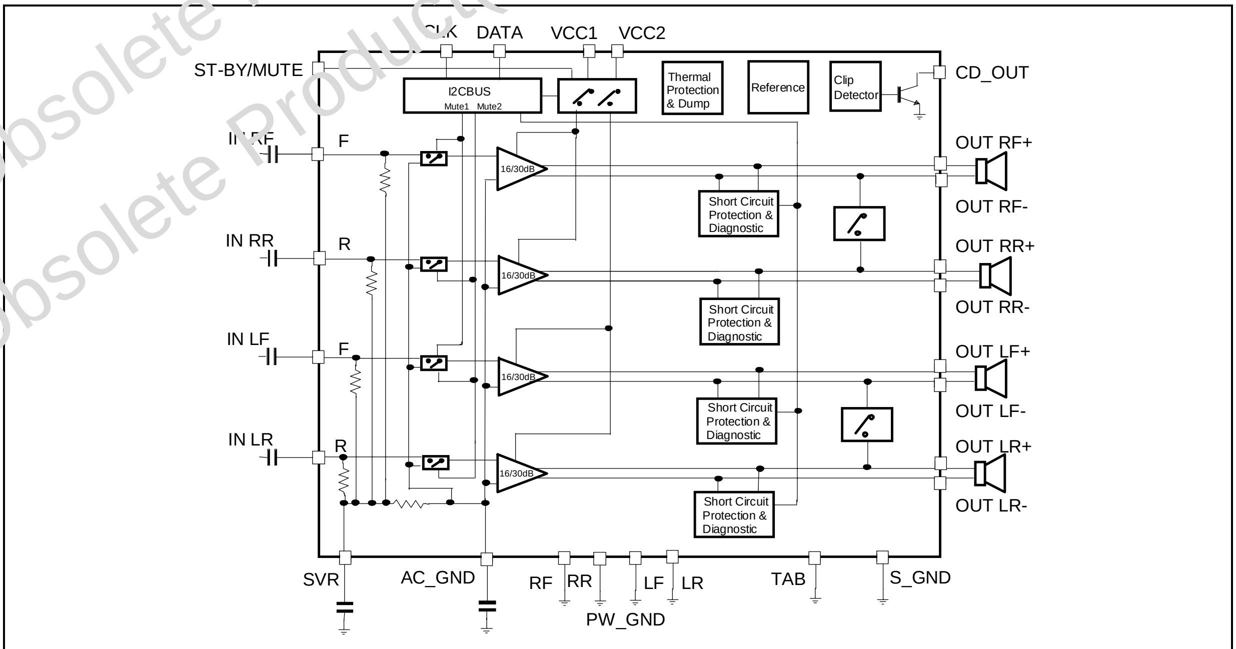
FLEXIWATT27

ORDERING NUMBER: TDA7563

DESCRIPTION

The TDA7563 is a new BCD technology Quad Bridge type of car radio amplifier in Flexiwatt27 package specially intended for car radio applications. Thanks to the DMOS output stage the TDA7563 has a very low distortion allowing a clear powerful sound. Among the features, its superior efficiency performance coming from the internal exclusive structure, makes it the most suitable device to simplify the thermal management in high power sets.The dissipated output power under average listening condition is in fact reduced up to 50% when compared to the level provided by conventional class AB solutions.This device is equipped with a full diagnostics array that communicates the status of each speaker through the I^{2}C bus.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{op}	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_{peak}	Peak Supply Voltage (for t = 50ms)	50	V
V_{CK}	CK pin Voltage	6	V
V_{DATA}	Data Pin Voltage	6	V
I_O	Output Peak Current (not repetitive t = 100ms)	8	A
I_O	Output Peak Current (repetitive f > 10Hz)	6	A
P_{tot}	Power Dissipation T_{case} = 70°C	85	W
T_{stg}, T_j	Storage and Junction Temperature	-55 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to case	Max.	1	°C/W

PIN CONNECTION (Top view)

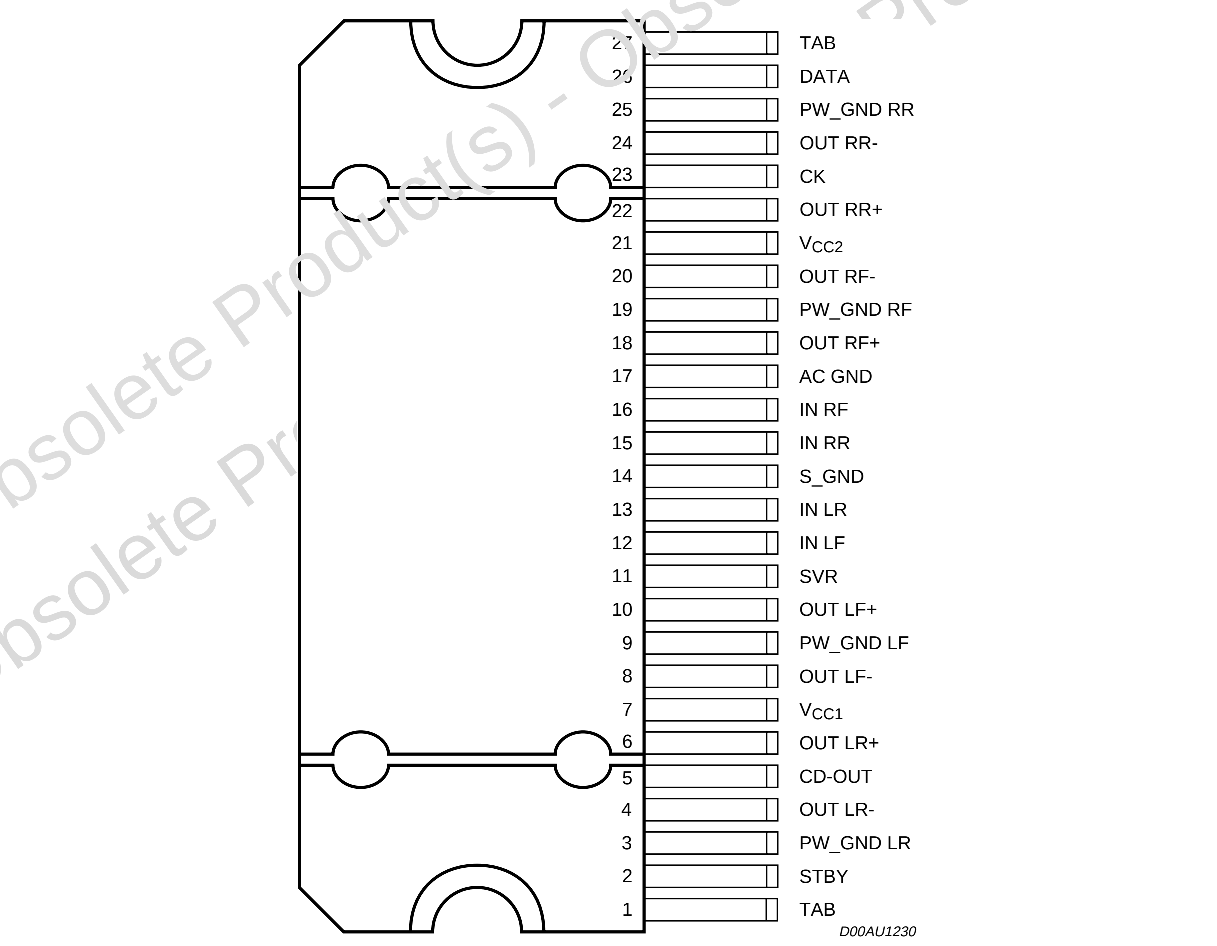
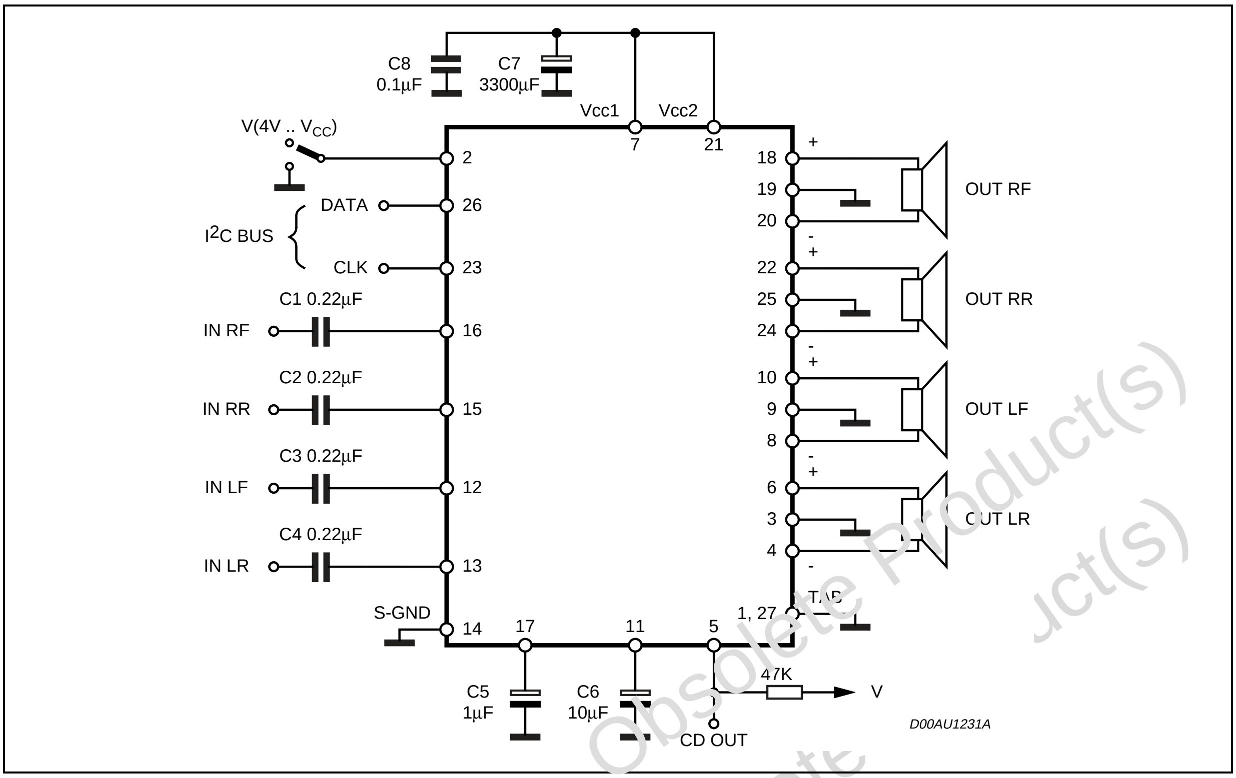


Figure 1. Application Circuit



ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, V_S = 14.4V; R_L = 4Ω; f = 1KHz; G_V = 30dB; T_{amb} = 25°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER AMPLIFIER						
V_S	Supply Voltage Range		8		18	V
I_d	Total Quiescent Drain Current			170	300	mA
P_O	Output Power	EIAJ (V_S = 13.7V)	35	40		W
		THD = 10% THD = 1%	25	28 22		W W
		R_L = 2Ω; EIAJ (V_S = 13.7V) R_L = 2Ω; THD 10% R_L = 2Ω; THD 1% R_L = 2Ω; MAX POWER	55 40	62 46 35 72		W W W W
THD	Total Harmonic Distortion	P_O = 1W to 10W; STD MODE HE MODE; P_O = 1.5W HE MODE; P_O = 8W		0.03 0.02 0.15	0.1 0.1 0.5	% % %
		P_O = 1-10W, f = 10kHz		0.2	0.5	%
		G_V = 16dB; STD Mode V_O = 0.1 to 5VRMS		0.02	0.05	%
C_T	Cross Talk	f = 1KHz to 10KHz, R_g = 600Ω	50	60		dB
R_{IN}	Input Impedance		60	100	130	KΩ
G_{V1}	Voltage Gain 1		29.5	30	30.5	dB
ΔG_{V1}	Voltage Gain Match 1		-1		1	dB
G_{V2}	Voltage Gain 2		15.5	16	16.5	dB
ΔG_{V2}	Voltage Gain Match 2		-1		1	dB
E_{IN1}	Output Noise Voltage 1	R_g = 600Ω 20Hz to 22kHz		50	100	mV
E_{IN2}	Output Noise Voltage 2	R_g = 600Ω; GV = 16dB 20Hz to 22kHz		15	30	mV
SVR	Supply Voltage Rejection	f = 100Hz to 10kHz; V_r = 1Vpk; R_g = 600Ω	50	60		dB
BW	Power Bandwidth		100			KHz
A_{SB}	Stand-by Attenuation		90	110		dB
I_{SB}	Stand-by Current			2	20	µA
A_M	Mute Attenuation		80	100		dB
V_{OS}	Offset Voltage	Mute & Play	-100	0	100	mV
V_{AM}	Min. Supply Mute Threshold		7	7.5	8	V
T_{ON}	Turn ON Delay	D2/D1 (IB1) 0 to 1		5	20	ms
T_{OFF}	Turn OFF Delay	D2/D1 (IB1) 1 to 0		5	20	ms
V_{SBY}	St-By/Mute pin for St-By		0		1.5	V
V_{MU}	St-By/Mute pin for Mute		3.5		5	V
V_{OP}	St-By/Mute pin for Operating		7		V_S	V
I_{MU}	St-By/Mute pin Current	$V_{STBY/MUTE}$ = 8.5V		20	40	µA
		$V_{STBY/MUTE}$ < 1.5V		0	10	µA
CD_{LK}	Clip Det High Leakage Current	CD off		0	15	µA
CD_{SAT}	Clip Det Sat. Voltage	CD on; I_{CD} = 1mA		300		mV
CD_{THD}	Clip Det THD level	D0 (IB1) = 1	5	10	15	%

ELECTRICAL CHARACTERISTICS (continued)
(Refer to the test circuit, V_S = 14.4V; R_L = 4Ω; f = 1KHz; G_V = 30dB; T_{amb} = 25°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
		D0 (IB1) = 0	1	2	3	%
TURN ON DIAGNOSTICS 1 (Power Amplifier Mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power Amplifier in st-by			1.2	V
Pvs	Short to Vs det. (above this limit, the Output isconsidered in Short Circuit to VS)		Vs -1.2			V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).		1.8		Vs -1.8	V
Lsc	Shorted Load det.				0.5	Ω
Lop	Open Load det.		130			Ω
Lnop	Normal Load det.		1.5		70	Ω
TURN ON DIAGNOSTICS 2 (Line Driver Mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power Amplifier in st-by			1.2	V
Pvs	Short to Vs det. (above this limit, the Output isconsidered in Short Circuit to VS)		Vs -1.2			V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).		1.8		Vs -1.8	V
Lsc	Shorted Load det.				1.5	Ω
Lop	Open Load det.		400			Ω
Lnop	Normal Load det.		4.5		200	Ω
PERMANENT DIAGNOSTICS 2 (Power Amplifier Mode or Line Driver Mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power Amplifier in Mute or Play, one or more short circuits protection activated			1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)		Vs -1.2			V
Pnop	Normal operation thresholds. (Within these limits, the Output is considered without faults).		1.8		Vs -1.8	V
L_{SC}	Shorted Load Det.	Pow. Amp. mode			0.5	Ω
		Line Driver mode			1.5	Ω
V_O	Offset Detection	Power Amplifier in play, AC Input signals = 0	±1.5	±2	±2.5	V
I_2C BUS INTERFACE						
S_{CL}	Clock Frequency				400	KHz
V_{IL}	Input Low Voltage				1.5	V
V_{IH}	Input High Voltage		2.3			V

Figure 2. Quiescent Current vs. Supply Voltage

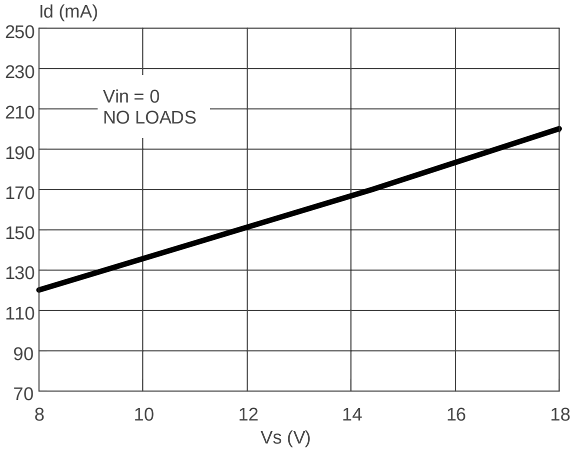


Figure 5. Distortion vs. Output Power (4Ω, STD)

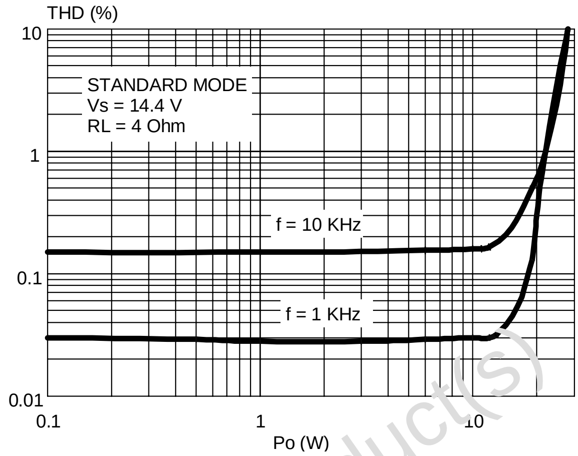


Figure 3. Output Power vs. Supply Voltage (4Ω)

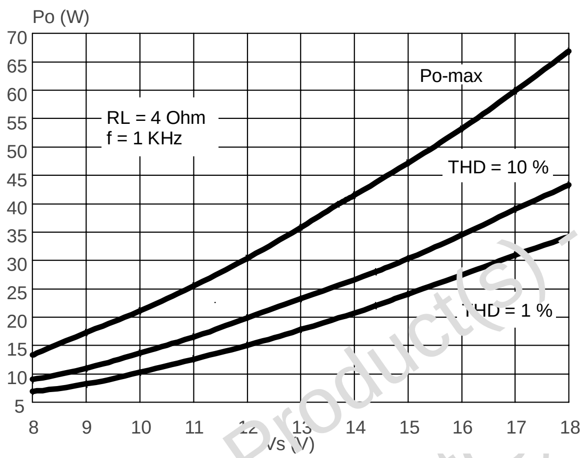


Figure 6. Distortion vs. Output Power (4Ω, HI-EFF)

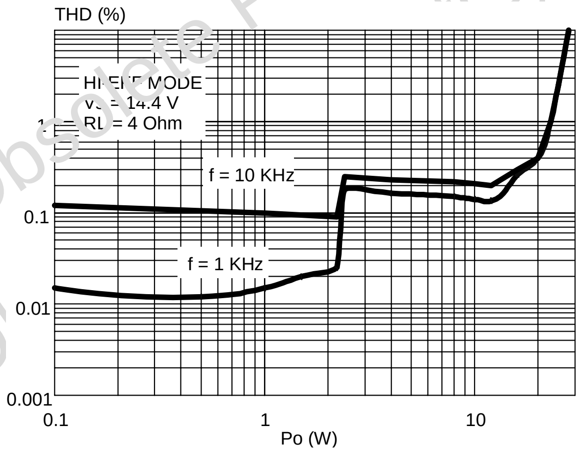


Figure 4. Output Power vs. Supply Voltage (2Ω)

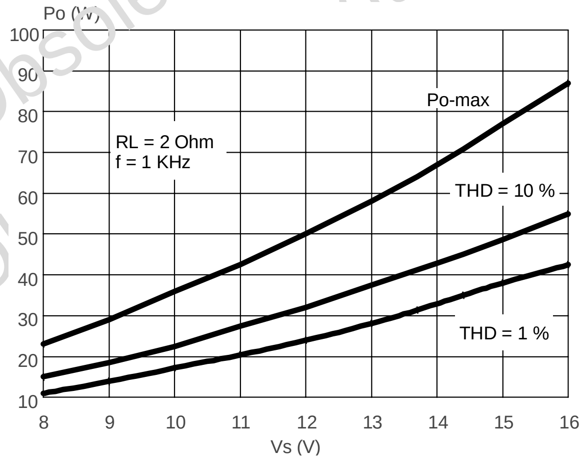


Figure 7. Distortion vs. Output Power (2Ω, STD)

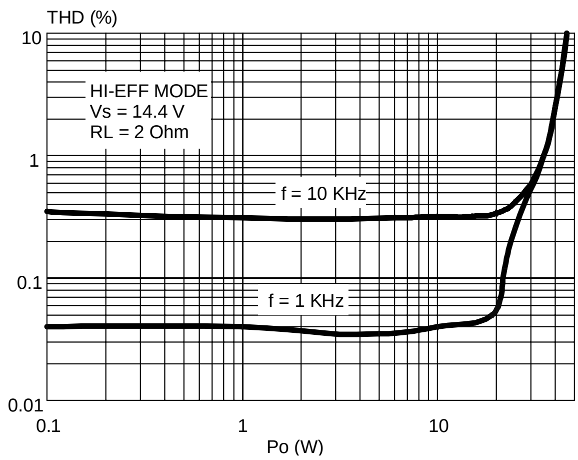


Figure 8. Distortion vs. Frequency (4Ω)

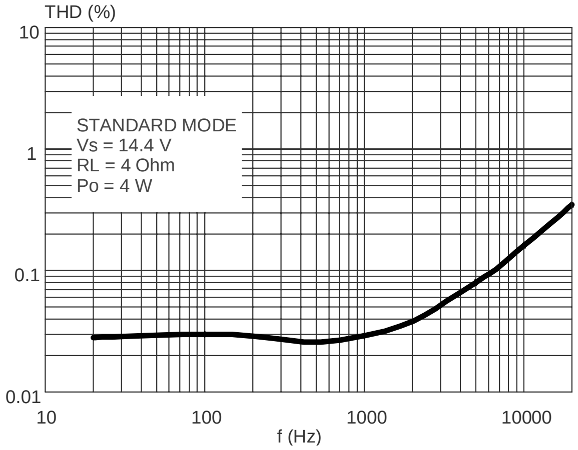


Figure 9. Distortion vs. Frequency (2Ω)

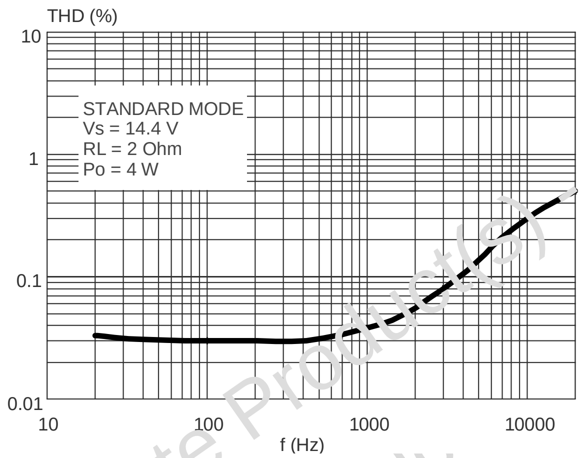


Figure 10. Crosstalk vs. Frequency

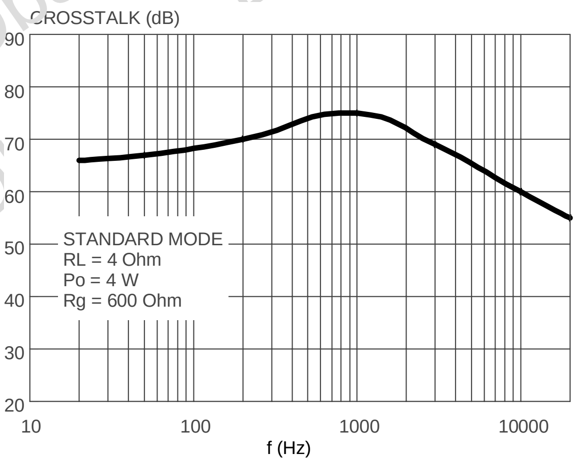


Figure 11. Supply Voltage Rejection vs. Freq.

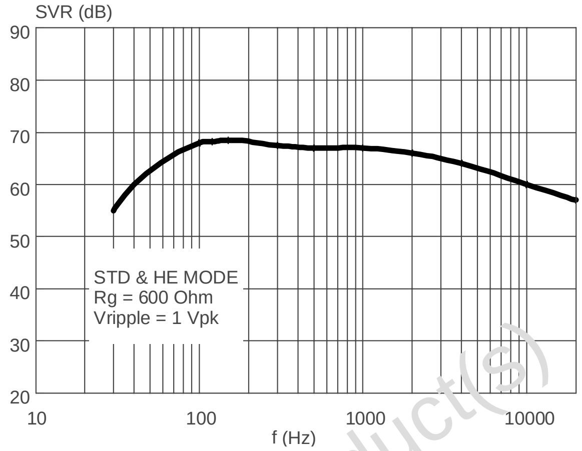


Figure 12. Power Dissipation & Efficiency vs. Output Power (4Ω, STD, SINE)

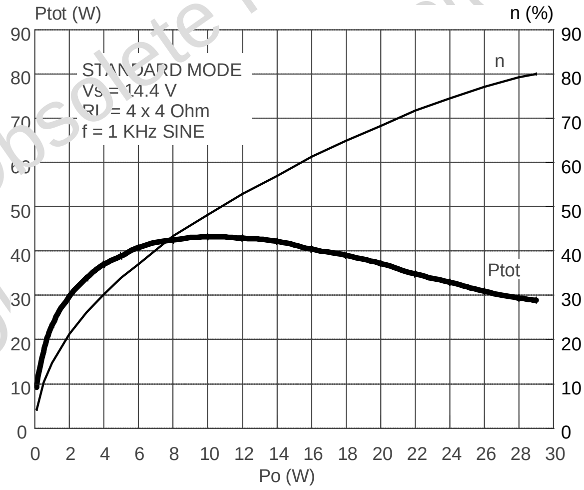


Figure 13. Power Dissipation & Efficiency vs. Output Power (4W, HI-EFF, SINE)

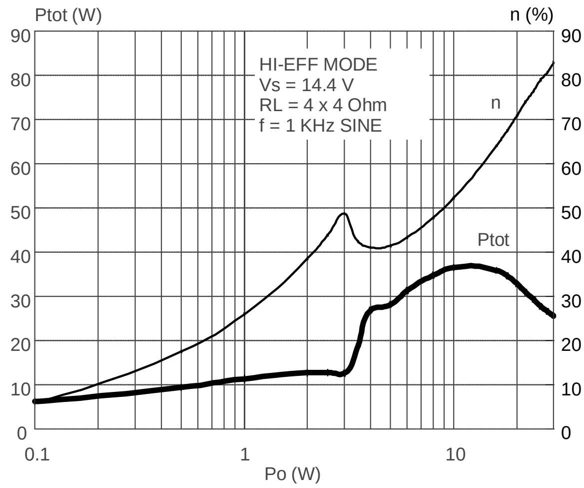


Figure 14. Power Dissipation vs. Average Ouput Power (Audio Program Simulation, 4Ω)

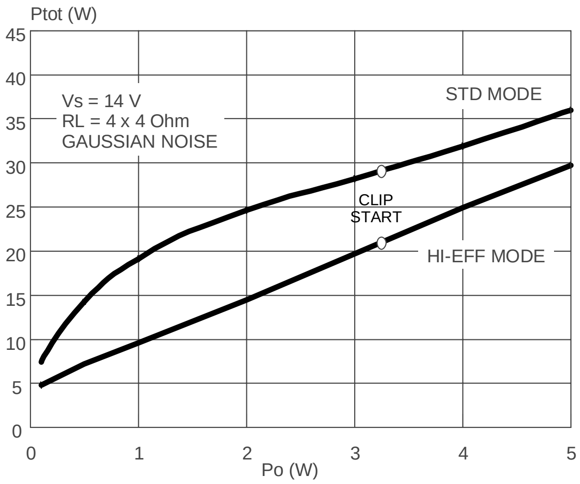
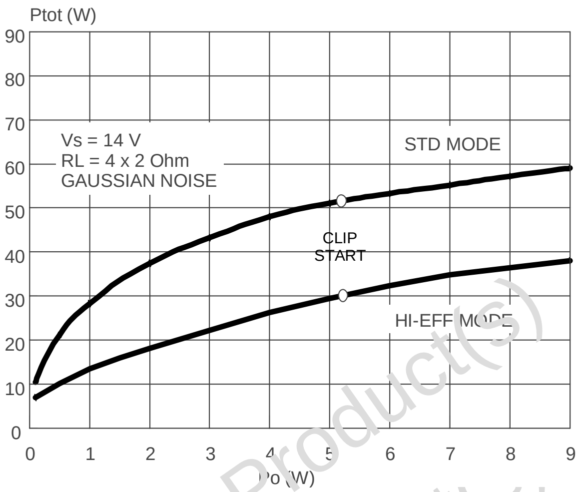


Figure 15. Power Dissipation vs. Average Ouput Power (Audio Program Simulation, 2Ω)



DIAGNOSTICS FUNCTIONAL DESCRIPTION:

a) TURN-ON DIAGNOSTIC

It is activated at the turn-on (stand-by out) under I^{2}Cbus request. Detectable output faults are:

– SHORT TO GND

– SHORT TO Vs

– SHORT ACROSS THE SPEAKER

– OPEN SPEAKER

To verify if any of the above misconnections are in place, a subsonic (inaudible) current pulse (fig. 16) is internally generated, sent through the speaker(s) and sunk back.The Turn On diagnostic status is internally stored until a successive diagnostic pulse is requested (after a I2C reading).

If the "stand-by out" and "diag. enable" commands are both given through a single programming step, the pulse takes place first (power stage still in stand-by mode, low, outputs= high impedance).

Afterwards, when the Amplifier is biased, the PERMANENT diagnostic takes place. The previous Turn On state is kept until a short appears at the outputs.

Figure 16. Turn - On diagnostic: working principle

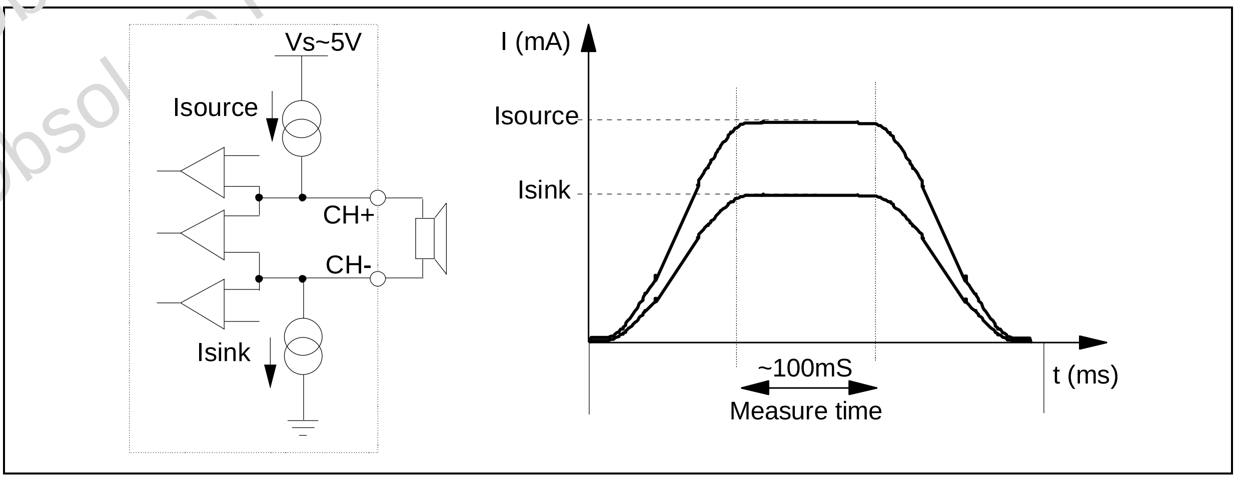


Fig. 17 and 18 show SVR and OUTPUT waveforms at the turn-on (stand-by out) with and without TURN-ON DIAGNOSTIC.

Figure 17. SVR and Output behaviour (CASE 1: without turn-on diagnostic)

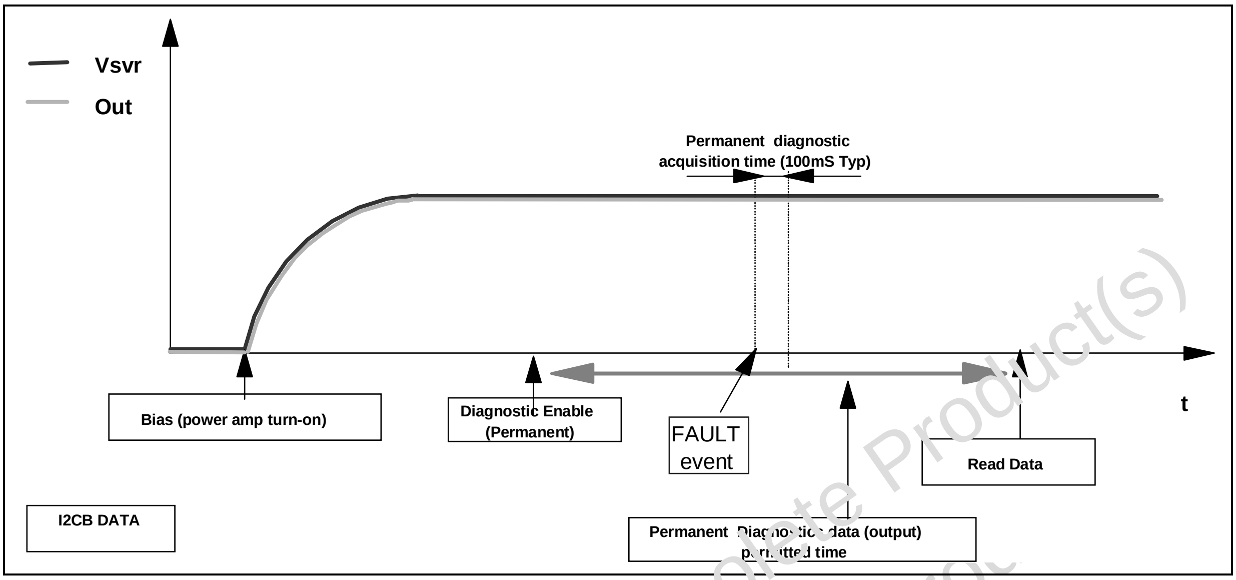
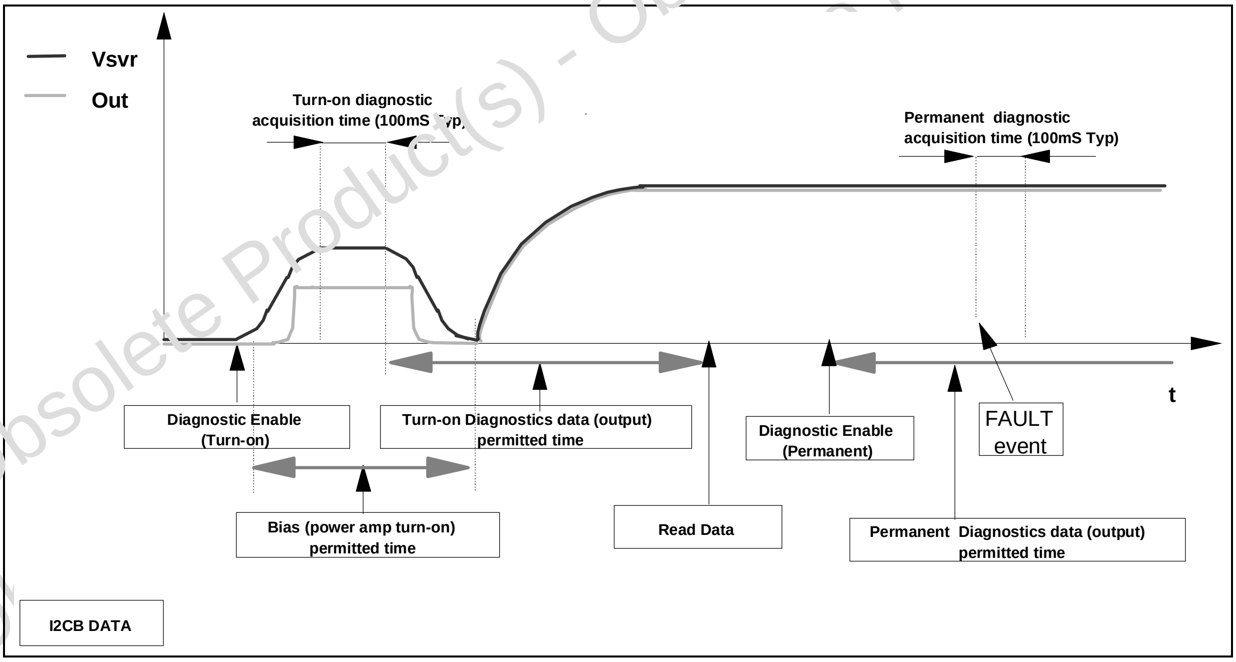
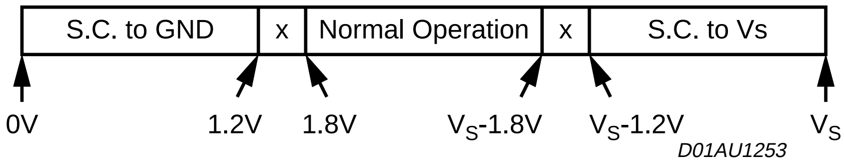


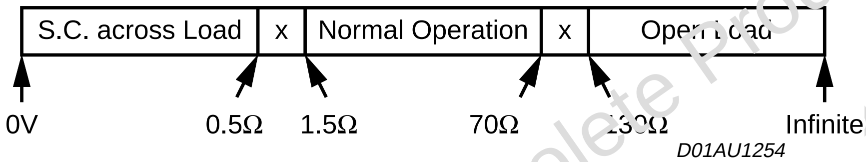
Figure 18. SVR and Output pin behaviour (CASE 2: with turn-on diagnostic)



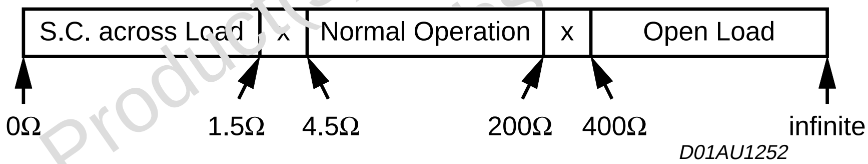
The information related to the outputs status is read and memorized at the end of the current pulse top. The acquisition time is 100 ms (typ.). No audible noise is generated in the process. As for SHORT TO GND / Vs the fault-detection thresholds remain unchanged from 30 dB to 16 dB gain setting. They are as follows:



Concerning SHORT ACROSS THE SPEAKER / OPEN SPEAKER, the threshold varies from 30 dB to 16 dB gain setting, since different loads are expected (either normal speaker's impedance or high impedance). The values in case of 30 dB gain are as follows:



If the Line-Driver mode (Gv= 16 dB and Line Driver Mode diagnostic = 1) is selected, the same thresholds will change as follows:



b) PERMANENT DIAGNOSTICS.

Detectable conventional faults are:

- SHORT TO GND
- SHORT TO Vs
- SHORT ACROSS THE SPEAKER

The following additional features are provided:

- OUTPUT OFFSET DETECTION

The TDA7563 has 2 operating statuses:

1 RESTART mode. The diagnostic is not enabled. Each audio channel operates independently from each other. If any of the a.m. faults occurs, only the channel(s) interested is shut down. A check of the output status is made every 1 ms (fig. 19). Restart takes place when the overload is removed.

2 DIAGNOSTIC mode. It is enabled via I^2C bus and self activates if an output overload (such to cause the intervention of the short-circuit protection) occurs to the speakers outputs . Once activated, the diagnostics procedure develops as follows (fig. 20):

– To avoid momentary re-circulation spikes from giving erroneous diagnostics, a check of the output status is made after 1ms: if normal situation (no overloads) is detected, the diagnostic is not performed and the channel returns back active.
– Instead, if an overload is detected during the check after 1 ms, then a diagnostic cycle having a duration of about 100 ms is started.
– After a diagnostic cycle, the audio channel interested by the fault is switched to RESTART mode. The relevant data are stored inside the device and can be read by the microprocessor. When one cycle has terminated, the next one is activated by an I^2C reading. This is to ensure continuous diagnostics throughout the car-radio operating time.
– To check the status of the device a sampling system is needed. The timing is chosen at microprocessor level (over half a second is recommended).

Figure 19. Restart timing without Diagnostic Enable (Permanent) - Each 1mS time, a sampling of the fault is done

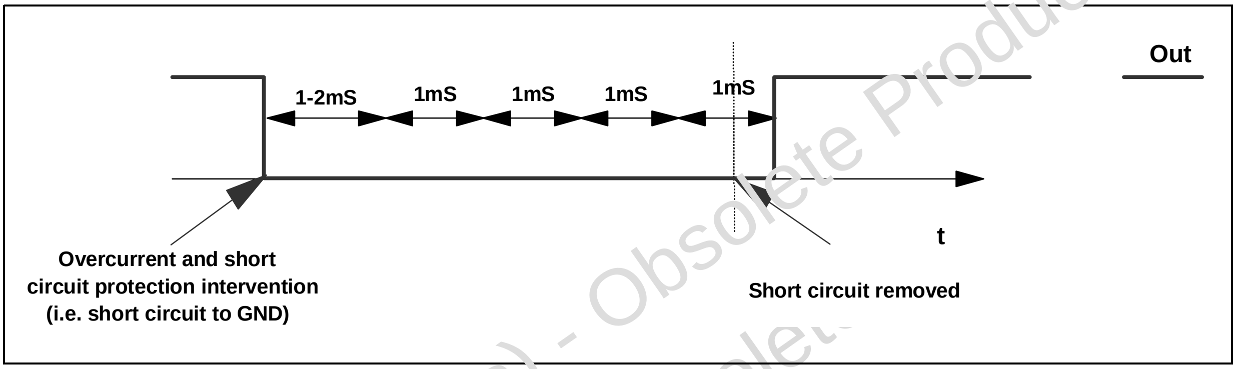
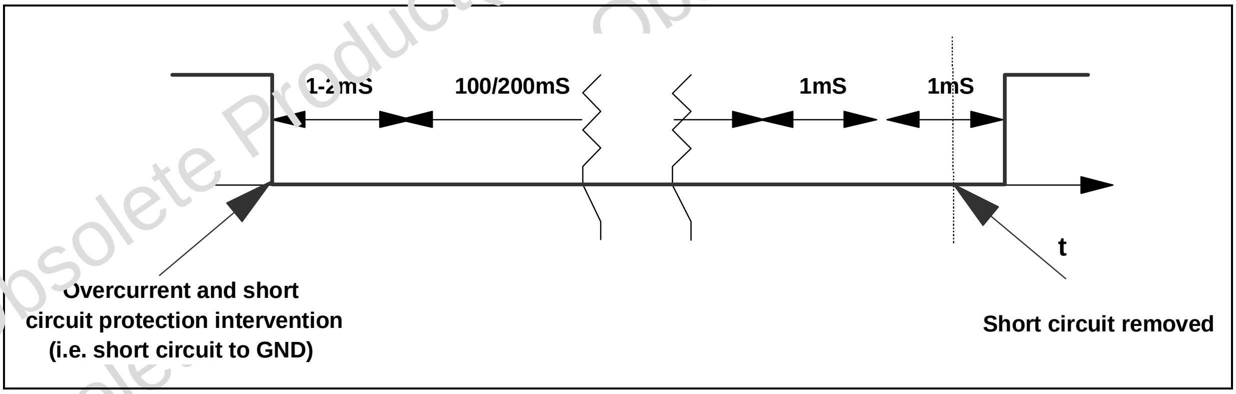


Figure 20. Restart timing with Diagnostic Enable (Permanent)



OUTPUT DC OFFSET DETECTION

Any DC output offset exceeding +/- 2 V are signalled out. This inconvenient might occur as a consequence of initially defective or aged and worn-out input capacitors feeding a DC component to the inputs, so putting the speakers at risk of overheating.

This diagnostic has to be performed with low-level output AC signal (or Vin = 0).

The test is run with selectable time duration by microprocessor (from a "start" to a "stop" command):

– START = Last reading operation or setting IB1 - D5 - (OFFSET enable) to 1

– STOP = Actual reading operation

Excess offset is signalled out if persistent throughout the assigned testing time. This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

MULTIPLE FAULTS

When more misconnections are simultaneously in place at the audio outputs, it is guaranteed that at least one of them is initially read out. The others are notified after successive cycles of I^2C reading and faults removal, provided that the diagnostic is enabled. This is true for both kinds of diagnostic (Turn on and Permanent).

The table below shows all the couples of double-fault possible. It should be taken into account that a short circuit with the 4 ohm speaker unconnected is considered as double fault.

Double fault table for Turn On Diagnostic					
	S. GND (so)	**S. GND (sk)**	**S. Vs**	**S. Across L.**	**Open L.**
S. GND (so)	S. GND	S. GND	S. Vs + S. GND	S. GND	S. GND
S. GND (sk)	/	S. GND	S. Vs	S. GND	Open L. (*)
S. Vs	/	/	S. Vs	S. Vs	S. Vs
S. Across L.	/	/	/	S. Across L.	N.A.
Open L.	/	/	/	/	Open L. (*)

S. GND (so) / S. GND (sk) in the above table make a distinction according to which of the 2 outputs is shorted to ground (test-current source side= so, test-current sink side = sk). More precisely, in Channels LF and RR, so = CH+, sk = CH-; in Channels LR and RF, so = CH-, sk = CH+ .

In Permanent Diagnostic the table is the same, with only a difference concerning Open Load(*) , which is not among the recognisable faults. Should an Open Load be present during the device's normal working, it would be detected at a subsequent Turn on Diagnostic cycle (i.e. at the successive Car Radio Turn on).

FAULTS AVAILABILITY

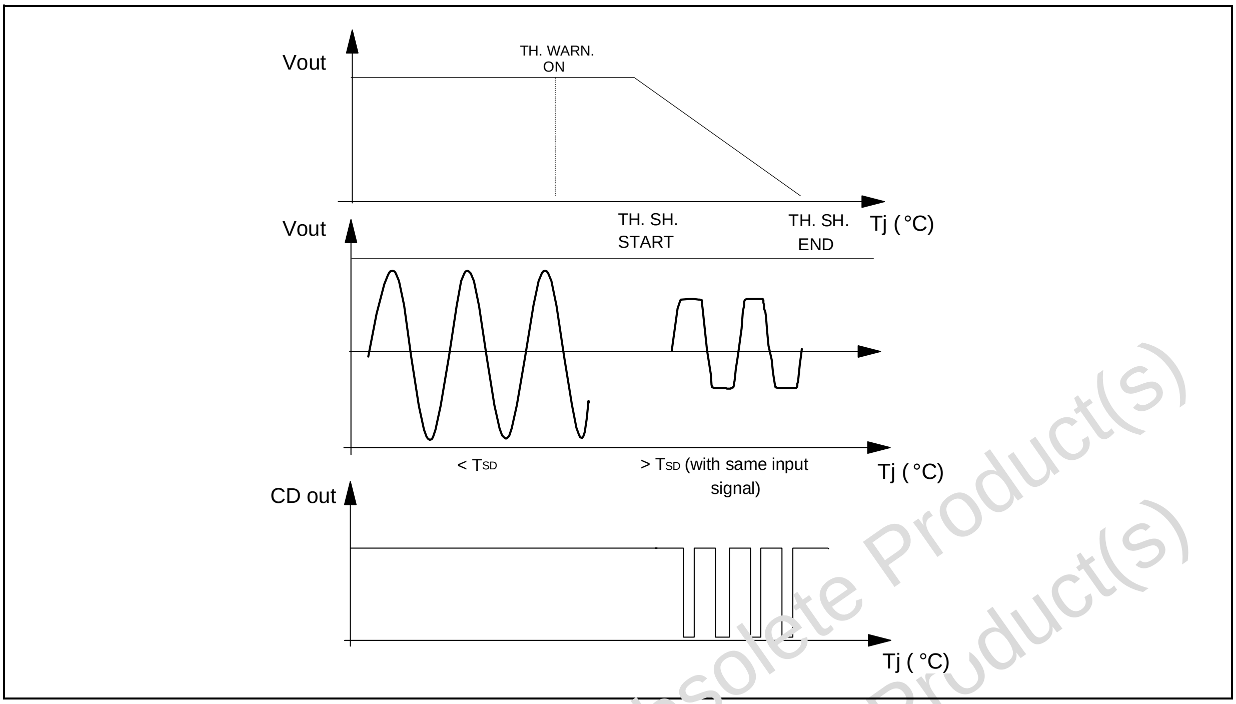
All the results coming from I^2Cbus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out.

To guarantee always resident functions, every kind of diagnostic cycles (Turn on, Permanent, Offset) will be reactivate after any I^2C reading operation. So, when the micro reads the I^2C, a new cycle will be able to start, but the read data will come from the previous diag. cycle (i.e. The device is in Turn On state, with a short to Gnd, then the short is removed and micro reads I^2C. The short to Gnd is still present in bytes, because it is the result of the previous cycle. If another I^2C reading operation occurs, the bytes do not show the short). In general to observe a change in Diagnostic bytes, two I^2C reading operations are necessary.

THERMAL PROTECTION

Thermal protection is implemented through thermal foldback (fig. 21). Thermal foldback begins limiting the audio input to the amplifier stage as the junction temperatures rise above the normal operating range. This effectively limits the output power capability of the device thus reducing the temperature to acceptable levels without totally interrupting the operation of the device. The output power will decrease to the point at which thermal equilibrium is reached. Thermal equilibrium will be reached when the reduction in output power reduces the dissipated power such that the die temperature falls below the thermal foldback threshold. Should the device cool, the audio level will increase until a new thermal equilibrium is reached or the amplifier reaches full power. Thermal foldback will reduce the audio output level in a linear manner.

Figure 21. Thermal Foldback Diagram



I²C PROGRAMMING/READING SEQUENCES

A correct turn on/off sequence respectful of the diagnostic timings and producing no audible noises could be as follows (after battery connection):

TURN-ON: PIN2 > 7V --- 10ms --- (STAND-BY OUT + DIAG ENABLE) --- 500 ms (min) --- MUTING OUT

TURN-OFF: MUTING IN --- 20 ms --- (DIAG DISABLE + STAND-BY IN) --- 10ms --- PIN2 = 0

Car Radio Installation: PIN2 > 7V --- 10ms DIAG ENABLE (write) --- 200 ms --- I²C read (repeat until All faults disappear).

OFFSET TEST: Device in Play (no signal) -- OFFSET ENABLE - 30ms - I²C reading (repeat I²C reading until high-offset message disappears).

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7563 and viceversa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown by fig. 22, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown by fig. 23 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The transmitter* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 24). The receiver** the acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDAline is stable LOW during this clock pulse.

* Transmitter

- master (µP) when it writes an address to the TDA7563
- slave (TDA7563) when the µP reads a data byte from TDA7563

** Receiver

- slave (TDA7563) when the µP writes an address to the TDA7563
- master (µP) when it reads a data byte from TDA7563

Figure 22. Data Validity on the I²CBUS

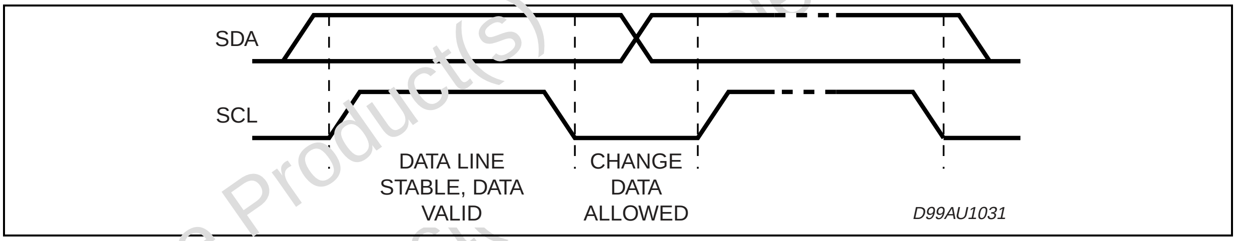


Figure 23. Timing Diagram on the I²CBUS

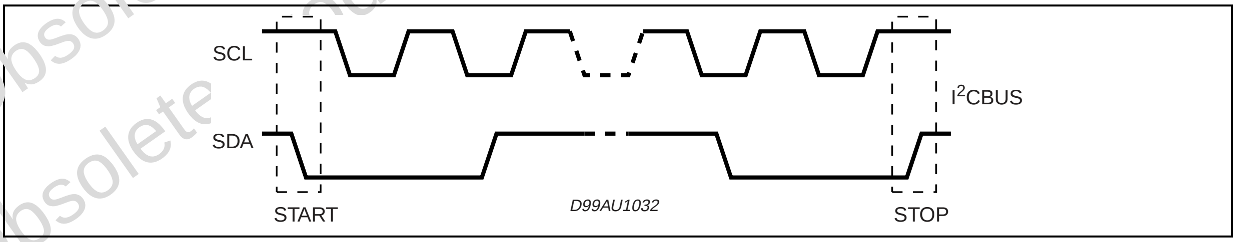
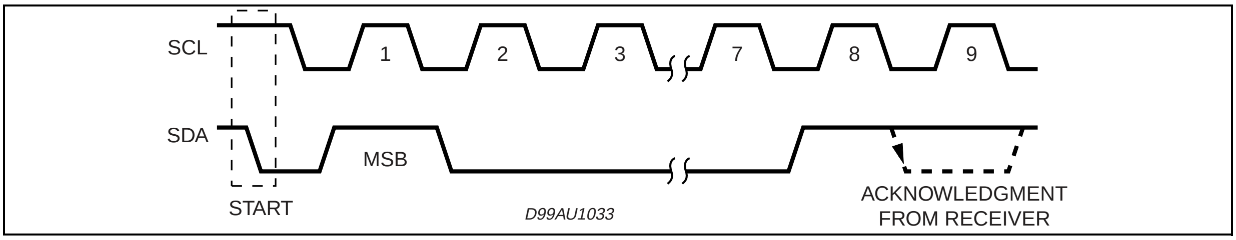


Figure 24. Acknowledge on the I²CBUS



SOFTWARE SPECIFICATIONS

All the functions of the TDA7563 are activated by I^2C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from µP to TDA7563) or read instruction (from TDA7563 to µP).

Chip Address:

D7							D0	
1	1	0	1	1	0	0	X	D8 Hex

X = 0 Write to device
X = 1 Read from device

If R/W = 0, the µP sends 2 "Instruction Bytes": IB1 and IB2.

IB1

D7	X
D6	Diagnostic enable (D6 = 1) Diagnostic defeat (D6 = 0)
D5	Offset Detection enable (D5 = 1) Offset Detection defeat (D5 = 0)
D4	Front Channel Gain = 30dB (D4 = 0) Gain = 16dB (D4 = 1)
D3	Rear Channel Gain = 30dB (D3 = 0) Gain = 16dB (D3 = 1)
D2	Mute front channels (D2 = 0) Unmute front channels (D2 = 1)
D1	Mute rear channels (D1 = 0) Unmute rear channels (D1 = 1)
D0	CD 2% (D0 = 0) CD 10% (D0 = 1)

IB2

D7	X
D6	used for testing
D5	used for testing
D4	Stand-by on - Amplifier not working - (D4 = 0)Stand-by off - Amplifier working - (D4 = 1)
D3	Power amplifier mode diagnostic (D3 = 0)Line driver mode diagnostic (D3 = 1)
D2	X
D1	Right ChannelPower amplifier working in standard mode (D1 = 0)Power amplifier working in high efficiency mode (D1 = 1)
D0	Left ChannelPower amplifier working in standard mode (D0 = 0)Power amplifier working in high efficiency mode (D0 = 1)

If R/W = 1, the TDA7563 sends 4 "Diagnostics Bytes" to µP: DB1, DB2, DB3 and DB4.

DB1

D7	Thermal warning active (D7 = 1)
D6	Diag. cycle not activated or not terminated (D6 = 0) Diag. cycle terminated (D6 = 1)
D5	X
D4	Channel LF Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel LF Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel LF Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Offset diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel LF No short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel LFNo short to GND (D1 = 0)Short to GND (D1 = 1)

DB2

D7	Offset detection not activated (D7 = 0) Offset detection activated (D7 = 1)
D6	X
D5	X
D4	Channel LR Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel LR Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel LR Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Permanent diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel LRNo short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel LRNo short to GND (D1 = 0) Short to GND (D1 = 1)

B3

D7	Stand-by status (= IB1 - D4)
D6	Diagnostic status (= IB1 - D6)
D5	X
D4	Channel RF Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel RF Normal load (D3 = 0) Short load (D3 = 1)
D2	Channel RF Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Permanent diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel RF No short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel RF No short to GND (D1 = 0) Short to GND (D1 = 1)

DB4

D7	X
D6	X
D5	X
D4	Channel RR Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)
D3	Channel R RNormal load (D3 = 0) Short load (D3 = 1)
D2	Channel RR Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Permanent diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)
D1	Channel RR No short to Vcc (D1 = 0) Short to Vcc (D1 = 1)
D0	Channel RR No short to GND (D1 = 0) Short to GND (D1 = 1)

Examples of bytes sequence

1 - Turn-On diagnostic - Write operation

Start	Address byte with D0 = 0	ACK	IB1 with D6 = 1	ACK	IB2	ACK	STOP

2 - Turn-On diagnostic - Read operation

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	DB3	ACK	DB4	ACK	STOP

The delay from 1 to 2 can be selected by software, starting from T.B.D. ms

3a - Turn-On of the power amplifier with 30dB gain, mute on, diagnostic defeat, CD = 2%.

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X0000000		XXX1XX11		

3b - Turn-Off of the power amplifier

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X0XXXXXX		XXX0XXXX		

4 - Offset detection procedure enable

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX1XX11X		XXX1XXXX		

5 - Offset detection procedure stop and reading operation (the results are valid only for the offset detection bits (D2 of the bytes DB1, DB2, DB3, DB4).

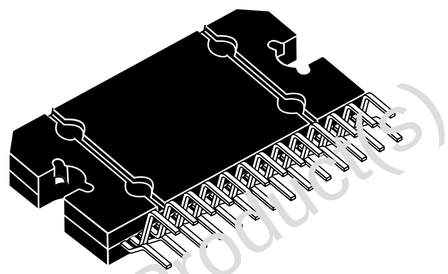
Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	DB3	ACK	DB4	ACK	STOP

- The purpose of this test is to check if a D.C. offset (2V typ.) is present on the outputs, produced by input capacitor with anomalous leackage current or humidity between pins.
- The delay from 4 to 5 can be selected by software, starting from T.B.D. ms

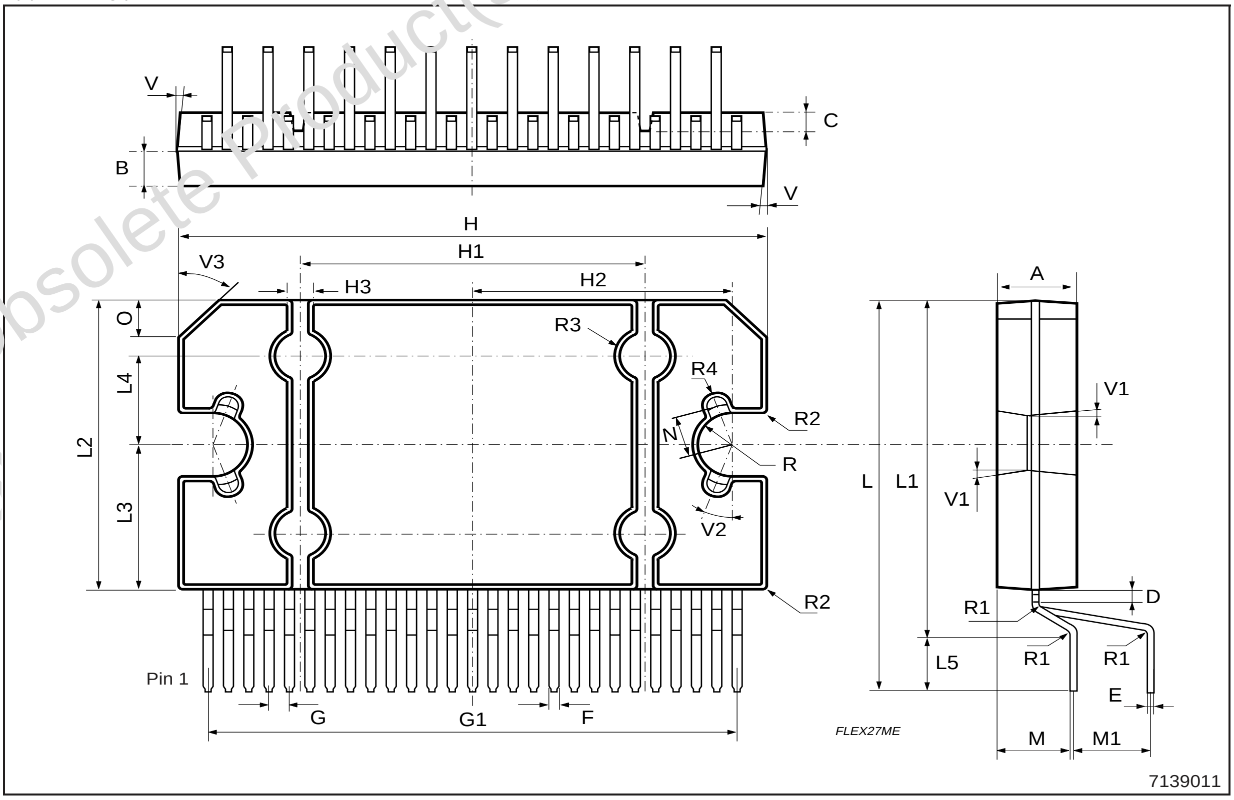
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



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