SN54LV123A
SN74LV123A
SCLS393Q – APRIL 1998 – REVISED AUGUST 2015

# SNx4LV123A Dual Retriggerable Monostable Multivibrators With Schmitt-Trigger Inputs

## 1 Features

- 2-V to 5.5-V $V_{CC}$ Operation
- Maximum $t_{pd}$ of 11 ns at 5 V
- Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class 11
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop PCs or Notebook PCs
- Digital Radio and Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Attached Storage (NAS)
- Personal Digital Assistant (PDA)
- Server PSU
- Solid-State Drive (SSD): Client and Enterprise
- Video Analytics Servers
- Wireless Headsets, Keyboard, and Mice

## 3 Description

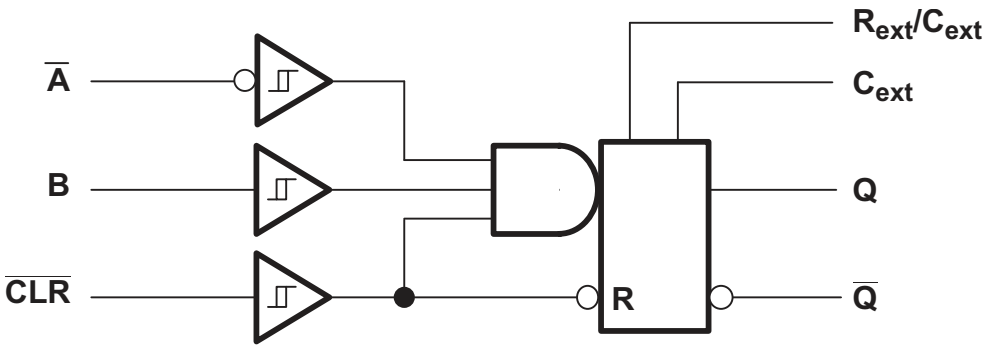
The 'LV123A devices are dual retriggerable monostable multivibrators designed for 2-V to 5.5-V $V_{CC}$ operation.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LV123AD | SOIC (16) | 6.00 mm x 9.90 mm |
| SN74LV123ADB | SSOP (16) | 7.80 mm x 6.20 mm |
| SN74LV123ANS | SO (16) | 7.80 mm x 10.20 mm |
| SN74LV123APW | TSSOP (16) | 6.40 mm x 5.00 mm |
| SN74LV123ARGY | VQFN (16) | 3.50 mm x 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram, Each Multivibrator (Positive Logic)**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision P (November 2013) to Revision Q** — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision O (April 1998) to Revision P** — **Page**

- Updated document to new TI datasheet format - no specification changes ... 1
- Removed *Ordering Information* table ... 3
- Updated operating temperature range. ... 5

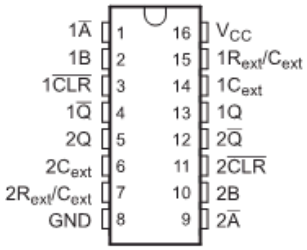
## 5 Description (continued)

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

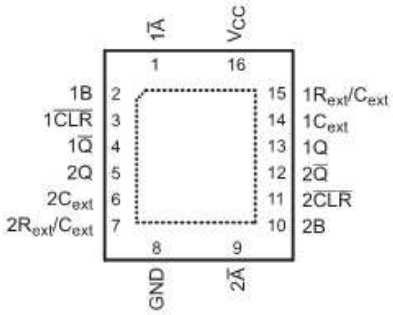
The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between $C_{ext}$ and $R_{ext}/C_{ext}$ (positive) and an external resistor connected between $R_{ext}/C_{ext}$ and $V_{CC}$. To obtain variable pulse durations, connect an external variable resistance between $R_{ext}/C_{ext}$ and $V_{CC}$. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

## 6 Pin Configuration and Functions

**D, DB, DGV, NS, or PW Package**
**16-Pin SOIC, SSOP, SO, TSSOP**
**Top View**




**RGY Package**
**16-Pin VQFN**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $1\overline{A}$ | 1 | I | Channel 1 falling edge trigger input when 1B = L; Hold low for other input methods |
| 1B | 2 | I | Channel 1 rising edge trigger input when $1\overline{A}$ = H; Hold high for other input methods |
| $1\overline{CLR}$ | 3 | I | Channel 1 rising edge trigger when $1\overline{A}$ = H and 1B = L; Hold high for other input methods; Can cut pulse length short by driving low during output |
| $1\overline{Q}$ | 4 | O | Channel 1 inverted output |
| 2Q | 5 | O | Channel 2 output |
| $2C_{ext}$ | 6 | — | Channel 2 external capacitor negative connection |
| $2R_{ext}/C_{ext}$ | 7 | — | Channel 2 external capacitor and resistor junction connection |
| GND | 8 | — | Ground |
| $2\overline{A}$ | 9 | I | Channel 2 falling edge trigger input when 2B = L; Hold low for other input methods |
| 2B | 10 | I | Channel 2 rising edge trigger input when $2\overline{A}$ = H; Hold high for other input methods |
| $2\overline{CLR}$ | 11 | I | Channel 2 rising edge trigger when $2\overline{A}$ = H and 2B = L; Hold high for other input methods; Can cut pulse length short by driving low during output |
| $2\overline{Q}$ | 12 | O | Channel 2 inverted output |
| 1Q | 13 | O | Channel 1 output |
| $1C_{ext}$ | 14 | — | Channel 1 external capacitor negative connection |
| $1R_{ext}/C_{ext}$ | 15 | — | Channel 1 external capacitor and resistor junction connection |
| $V_{CC}$ | 16 | — | Power supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage in power-off state(2) | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_j$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value is limited to 5.5 V maximum.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

See (1).

| | | | SN54LV123A (2) | | | SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | | 5.5 | 2 | | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | | $V_{CC}$ × 0.7 | | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | | $V_{CC}$ × 0.7 | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | | $V_{CC}$ × 0.7 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | $V_{CC}$ × 0.3 | | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | | $V_{CC}$ × 0.3 | | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | $V_{CC}$ × 0.3 | | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | | 5.5 | 0 | | 5.5 | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | | –50 | | | –50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | –2 | | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | | –6 | | | –6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | –12 | | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | | 50 | | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | 2 | | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | | 6 | | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | 12 | | | 12 | |
| $R_{ext}$ | External timing resistance | $V_{CC}$ = 2 V | 5 | | | 5 | | | kΩ |
| | | $V_{CC}$ ≥ 3 V | 1 | | | 1 | | | |
| $C_{ext}$ | External timing capacitance | | No restriction | | | No restriction | | | pF |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 1 | | | 1 | | | ms/V |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) Product Preview

## 7.4 Thermal Information

| THERMAL METRIC (1) | | SNx4LV123A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | NS (SO) | PW (TSSOP) | RGY (VQFN) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73 | 82 | 120 | 64 | 108 | 39 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | –55°C to 125°C SN54LV123A(1) | | | –40°C to 85°C SN74LV123A | | | Recommended –40°C to 125°C SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 µA | 2 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | 2 | | | 2 | | | |
| | | $I_{OH}$ = –6 mA | 3 V | 2.48 | | | 2.48 | | | 2.48 | | | |
| | | $I_{OH}$ = –12 mA | 4.5 V | 3.8 | | | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | | | 0.1 | V |
| | | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.44 | | | 0.44 | |
| | | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.55 | | | 0.55 | |
| $I_I$ | $R_{ext}/C_{ext}$(2) | $V_I$ = 5.5 V or GND | 5.5 V | | | ±2.5 | | | ±2.5 | | | ±25 | µA |
| | $\overline{A}$, B, and $\overline{CLR}$ | $V_I$ = 5.5 V or GND | 0 V | | | ±1 | | | ±1 | | | ±1 | |
| | | | 0 to 5.5 V | | | ±1 | | | ±1 | | | ±1 | |
| $I_{CC}$ | Quiescent | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | | | 20 | µA |
| $I_{CC}$ | Active state (per circuit) | $V_I = V_{CC}$ or GND, $R_{ext}/C_{ext}$ = 0.5 $V_{CC}$ | 3 V | | | 280 | | | 280 | | | 280 | µA |
| | | | 4.5 V | | | 650 | | | 650 | | | 650 | |
| | | | 5.5 V | | | 975 | | | 975 | | | 975 | |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 to 5.5 V | 0 V | | | | | | 5 | | | 5 | µA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 3.3 V | | 1.9 | | | 1.9 | | | 1.9 | | pF |
| | | | 5 V | | 1.9 | | | 1.9 | | | 1.9 | | |

(1) Product Preview
(2) This test is performed with the terminal in the off-state condition.

## 7.6 Timing Requirements, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 5)

| PARAMETER | | | TEST CONDITIONS | | $T_A$ = 25°C | | | –55°C to 125°C SN54LV123A(1) | | | –40°C to 85°C SN74LV123A | | | –40°C to 125°C SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ | | | 6 | | | 6.5 | | | 6.5 | | | 6.5 | | | ns |
| | | $\overline{A}$ or B trigger | | | 6 | | | 6.5 | | | 6.5 | | | 6.5 | | | |
| $t_{rr}$ | Pulse retrigger time | | $R_{ext}$ = 1 kΩ | $C_{ext}$ = 100 pF | See(2) | 94 | | See(2) | | | See(2) | | | See(2) | | | ns |
| | | | | $C_{ext}$ = 0.01 µF | See(2) | 2 | | See(2) | | | See(2) | | | See(2) | | | µs |

(1) Product Preview
(2) See retriggering data in the *Application Information* section.

## 7.7 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | –55°C to 125°C SN54LV123A(1) | | | –40°C to 85°C SN74LV123A | | | –40°C to 125°C SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_w$ Pulse duration | $\overline{CLR}$ | | | 5 | | | 5 | | | 5 | | | 5 | | | ns |
| | $\overline{A}$ or B trigger | | | 5 | | | 5 | | | 5 | | | 5 | | | |
| $t_{rr}$ Pulse retrigger time | | $R_{ext}$ = 1 kΩ | $C_{ext}$ = 100 pF | See(2) | 76 | | See(2) | | | See(2) | | | See(2) | | | ns |
| | | | $C_{ext}$ = 0.01 µF | See(2) | 1.8 | | See(2) | | | See(2) | | | See(2) | | | µs |

(1) Product Preview
(2) See retriggering data in the *Application Information* section.

## 7.8 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | –55°C to 125°C SN54LV123A(1) | | | –40°C to 85°C SN74LV123A | | | –40°C to 125°C SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_w$ Pulse duration | $\overline{CLR}$ | | | 5 | | | 5 | | | 5 | | | 5 | | | ns |
| | $\overline{A}$ or B trigger | | | 5 | | | 5 | | | 5 | | | 5 | | | |
| $t_{rr}$ Pulse retrigger time | | $R_{ext}$ = 1 kΩ | $C_{ext}$ = 100 pF | See(2) | 59 | | See(2) | | | See(2) | | | See(2) | | | ns |
| | | | $C_{ext}$ = 0.01 µF | See(2) | 1.5 | | See(2) | | | See(2) | | | See(2) | | | µs |

(1) Product Preview
(2) See retriggering data in the *Application Information* section.

## 7.9 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | –55°C to 125°C SN54LV123A(1) | | | –40°C to 85°C SN74LV123A | | | –40°C to 125°C SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 14.5 | 31.4(2) | 1(2) | | 37(2) | 1 | | 37 | 1 | | 37 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 13 | 25(2) | 1(2) | | 29.5(2) | 1 | | 29.5 | 1 | | 29.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 15.1 | 33.4(2) | 1(2) | | 39(2) | 1 | | 39 | 1 | | 39 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 16.6 | 36 | 1 | | 42 | 1 | | 42 | 1 | | 42 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 14.7 | 32.8 | 1 | | 34.5 | 1 | | 34.5 | 1 | | 34.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 17.4 | 38 | 1 | | 44 | 1 | | 44 | 1 | | 44 | |
| $t_w$(3) | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 197 | 260 | | | 320 | | | 320 | | | 320 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | | 110 | 90 | | 110 | 90 | | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | | 1.1 | 0.9 | | 1.1 | 0.9 | | 1.1 | ms |
| $\Delta t_w$(4) | | | $C_L$ = 50 pF | | ±1% | | | | | | | | | | | |

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) $t_w$ = Duration of pulse at Q and $\overline{Q}$ outputs
(4) $\Delta t_w$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

## 7.10 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | –55°C to 125°C SN54LV123A(1) | | | –40°C to 85°C SN74LV123A | | | –40°C to 125°C SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 10.2 | 20.6(2) | 1(2) | | 24(2) | 1 | | 24 | 1 | | 24 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 9.3 | 15.8(2) | 1(2) | | 18.5(2) | 1 | | 18.5 | 1 | | 18.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 10.6 | 22.4(2) | 1(2) | | 26(2) | 1 | | 26 | 1 | | 26 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 11.8 | 24.1 | 1 | | 27.5 | 1 | | 27.5 | 1 | | 27.5 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 10.5 | 19.3 | 1 | | 22 | 1 | | 22 | 1 | | 22 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 12.3 | 25.9 | 1 | | 29.5 | 1 | | 29.5 | 1 | | 29.5 | |
| $t_w$(3) | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 182 | 240 | | | 300 | | | 300 | | | 300 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | | 110 | 90 | | 110 | 90 | | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | | 1.1 | 0.9 | | 1.1 | 0.9 | | 1.1 | ms |
| $\Delta t_w$(4) | | | $C_L$ = 50 pF | | ±1% | | | | | | | | | | | |

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) $t_w$ = Duration of pulse at Q and $\overline{Q}$ outputs
(4) $\Delta t_w$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

## 7.11 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | –55°C to 125°C SN54LV123A(1) | | | –40°C to 85°C SN74LV123A | | | –40°C to 125°C SN74LV123A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.1 | 12(2) | 1(2) | | 14(2) | 1 | | 14 | 1 | | 14 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 6.5 | 9.4(2) | 1(2) | | 11(2) | 1 | | 11 | 1 | | 11 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 7.4 | 12.9(2) | 1(2) | | 15(2) | 1 | | 15 | 1 | | 15 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 8.3 | 14 | 1 | | 16 | 1 | | 16 | 1 | | 16 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 7.4 | 11.4 | 1 | | 13 | 1 | | 13 | 1 | | 13 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 8.7 | 14.9 | 1 | | 17 | 1 | | 17 | 1 | | 17 | |
| $t_w$(3) | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 167 | 200 | | | 240 | | | 240 | | | 240 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | | 110 | 90 | | 110 | 90 | | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | | 1.1 | 0.9 | | 1.1 | 0.9 | | 1.1 | ms |
| $\Delta t_w$(4) | | | $C_L$ = 50 pF | | ±1% | | | | | | | | | | | |

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) $t_w$ = Duration of pulse at Q and $\overline{Q}$ outputs
(4) $\Delta t_w$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

## 7.12 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 10 MHz | 3.3 V | 44 | pF |
| | | | | 5 V | 49 | |

## 7.13 Typical Characteristics

Operation of the devices at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied.

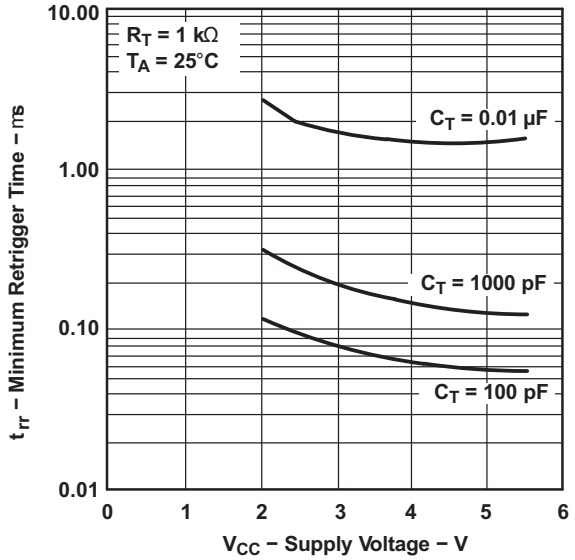



**Figure 1. Minimum Trigger vs $V_{CC}$ Characteristics**

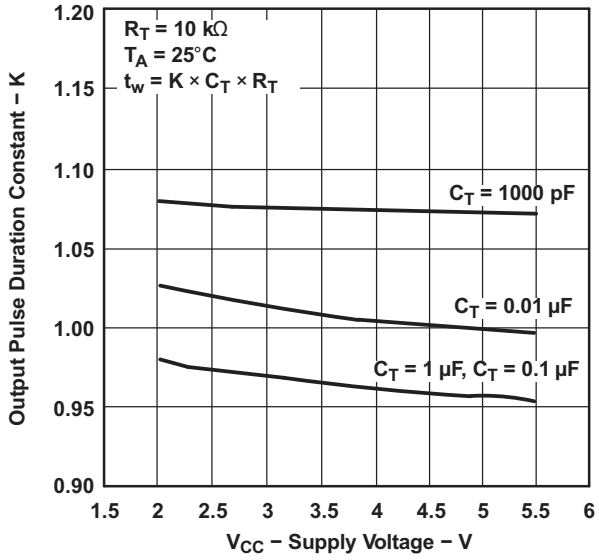



**Figure 2. Output Pulse-Duration Constant vs Supply Voltage**

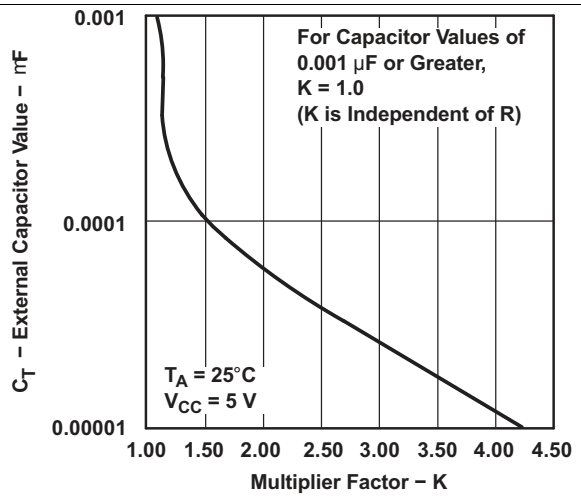



**Figure 3. External Capacitance vs Multiplier Factor**

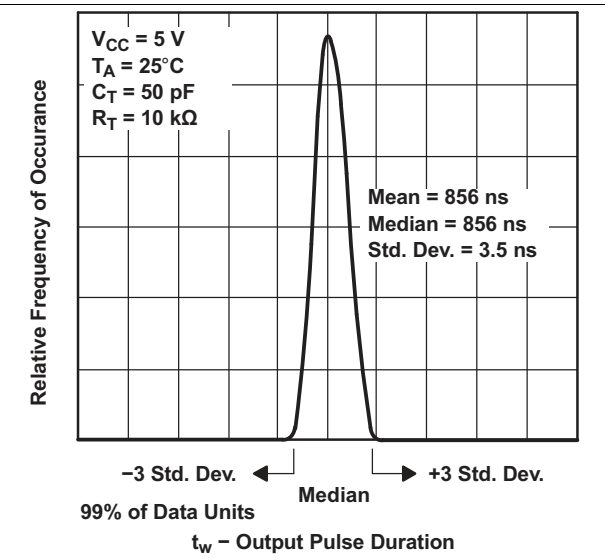
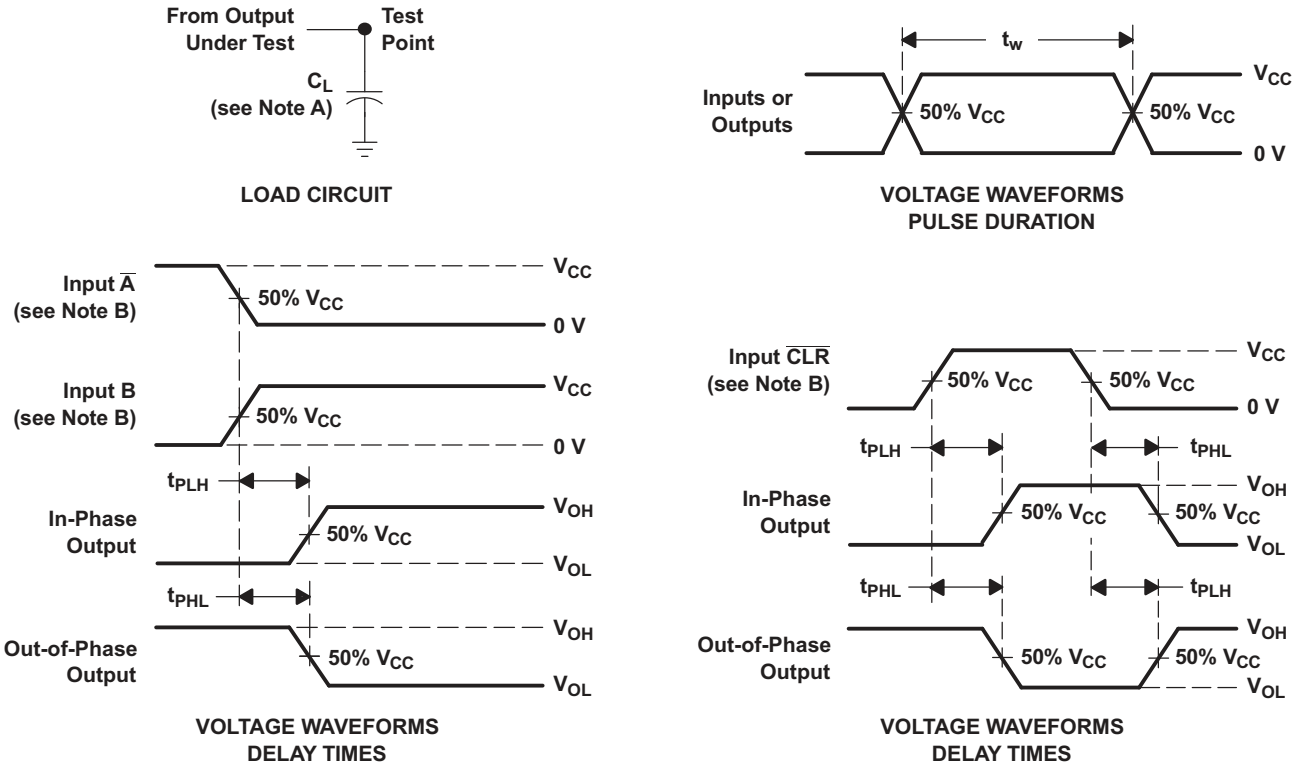



**Figure 4. Distribution of Units vs Output Pulse Duration**

## 8 Parameter Measurement Information




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ – 3 ns, $t_f$ – 3 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

**Figure 5. Load Circuit and Voltage Waveforms**

# 9 Detailed Description

## 9.1 Overview

The SNx4LV123A devices contain two independent monostable multivibrators. They produce a specific width high output pulse when triggered ($\overline{Q}$ is normally high, pulse is low). The device uses an external RC circuit to determine the output pulse length, which is explained in detail in the *Application Information* section.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. The Figure 7 illustrates pulse control by retriggering the inputs and early clearing.

During power-up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Pin assignments for these devices are identical to those of the 'AHC123A and 'AHCT123A devices for interchangeability, when allowed.

## 9.2 Functional Block Diagrams

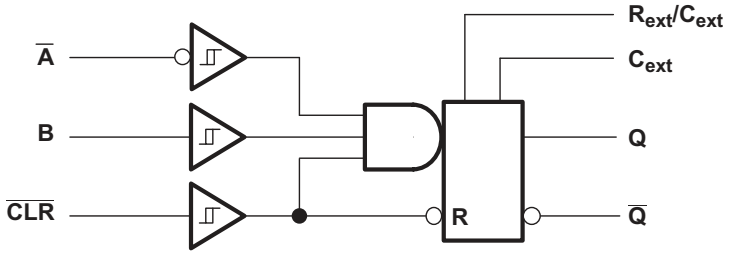



**Figure 6. Logic Diagram, Each Multivibrator (Positive Logic)**

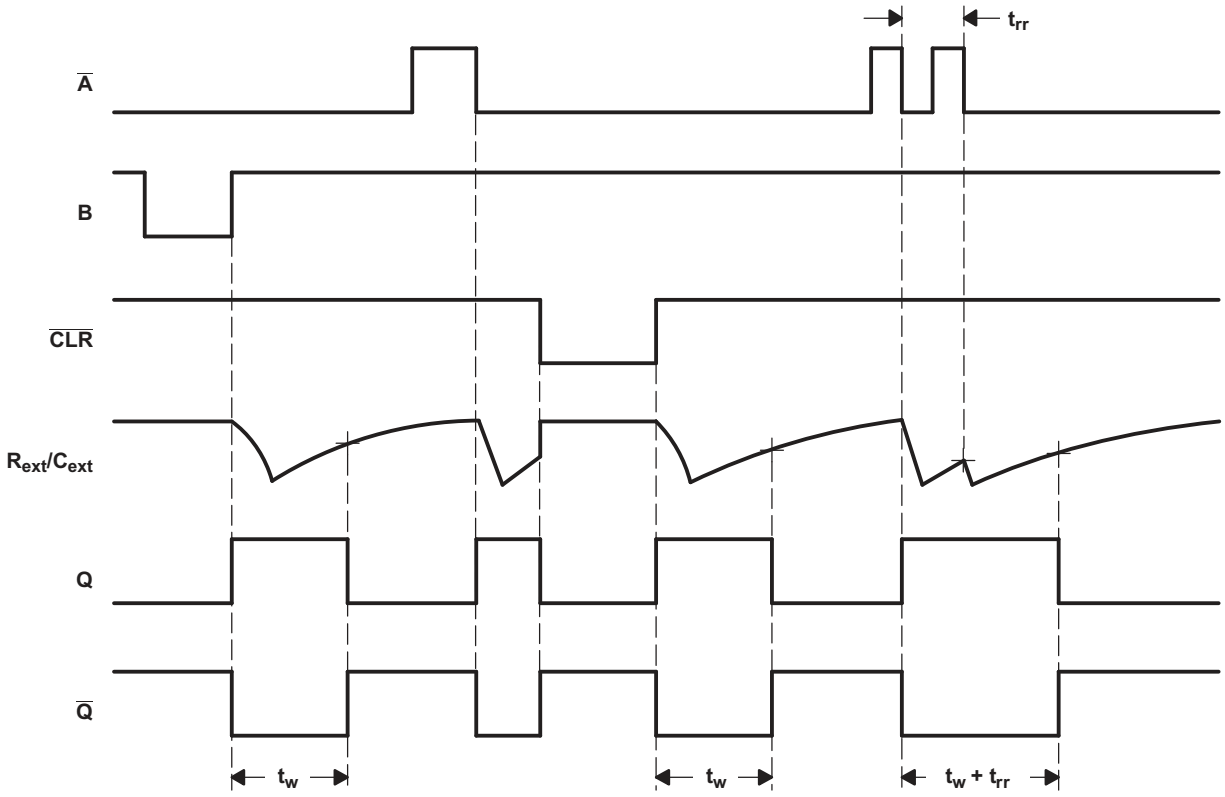



**Figure 7. Input and Output Timing Diagram**

## 9.3 Feature Description

The 'LV123A devices operate over a wide supply range from 2 V to 5.5 V. The propagation delay has a maximum of 11 ns at 5-V supply. The typical output ground bounce is less than 0.8 V at 3.3-V supply and 25°C. The typical output $V_{OH}$ undershoot is greater than 2.3 V at 3.3-V supply and 25°C.

These parts support mixed-mode voltage operation on all ports.

Schmitt-trigger circuitry on the $\overline{A}$, B, and $\overline{CLR}$ inputs allow for slow input transition rates and noisy input signals.

This device can be configured for rising or falling edge triggering.

This device supports partial-power-down mode operation.

This device is retriggerable for very long output pulses up to 100% duty cycle.

The clear signal overrides an output pulse and terminates it early.

Glitch-free power-up reset on outputs.

## 9.4 Device Functional Modes

Table 1 lists the functional modes of the 'LV123A devices.

**Table 1. Function Table (Each Multivibrator)**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{A}$ | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎏ |
| H | ↓ | H | ⎍ | ⎏ |
| ↑ | L | H | ⎍ | ⎏ |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The SNx4LV123A device is a dual monostable multivibrator. It can be configured for many pulse width outputs and rising- or falling-edge triggering. The application shown here could be used to signal separate interruptable inputs on a microcontroller when an input had a rising or falling edge.

## 10.2 Typical Application

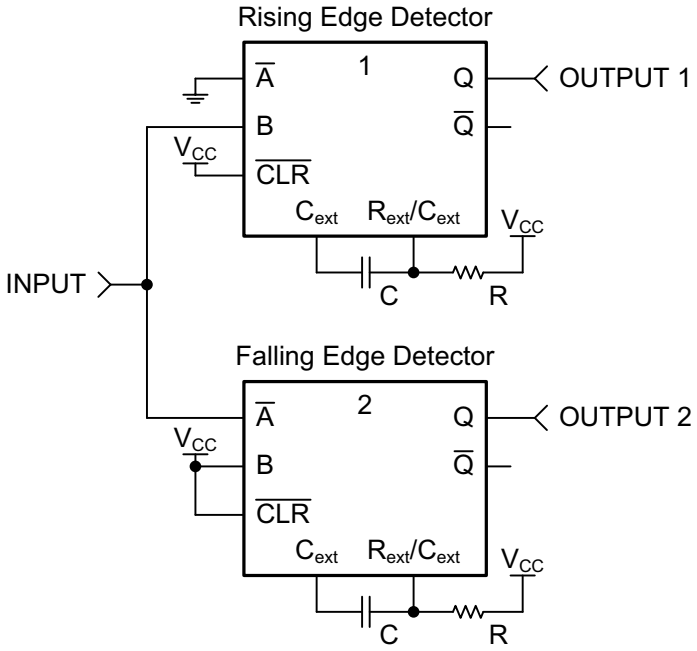



**Figure 8. Simplified Application Schematic**

### 10.2.1 Design Requirements

**CAUTION**

To prevent malfunctions due to noise, connect a high-frequency capacitor between $V_{CC}$ and GND, and keep the wiring between the external components and $C_{ext}$ and $R_{ext}/C_{ext}$ terminals as short as possible.

## Typical Application (continued)

### 10.2.1.1 Power-Down Considerations

Large values of $C_{ext}$ can cause problems when powering down the 'LV123A devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from $V_{CC}$ through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the $V_{CC}$ power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if $V_{CC}$ = 5 V and $C_{ext}$ = 15 pF, the $V_{CC}$ supply must turn off no faster than $t = (5\ V) \times (15\ pF)/30\ mA = 2.5$ ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of $V_{CC}$ to zero occurs, the 'LV123A devices can sustain damage. To avoid this possibility, use external clamping diodes.

### 10.2.1.2 Output Pulse Duration

The output pulse duration, $t_w$, is determined primarily by the values of the external capacitance ($C_T$) and timing resistance ($R_T$). The timing components are connected as shown in Figure 9.

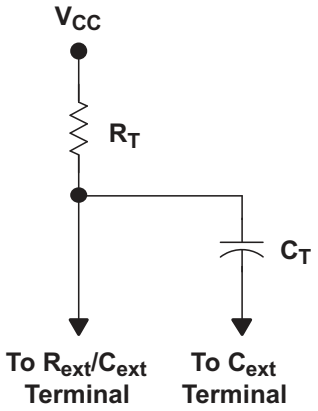



**Figure 9. Timing-Component Connections**

If $C_T$ is ≥1000 pF and K = 1.0, the pulse duration is given by:

$$t_w = K \times R_T \times C_T$$

where

- $t_w$ = pulse duration in ns
- $R_T$ = external timing resistance in kΩ
- $C_T$ = external capacitance in pF
- K = multiplier factor (1)

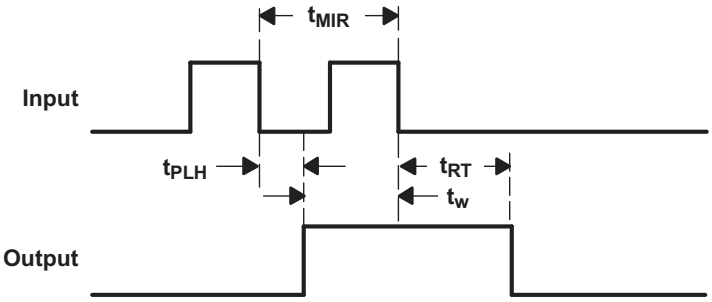
if $C_T$ is <1000 pF, K can be determined from Figure 3

Equation 1 and Figure 13 can be used to determine values for pulse duration, external resistance, and external capacitance.

### 10.2.1.3 Retriggering Data

The minimum input retriggering time ($t_{MIR}$) is the minimum time required after the initial signal before retriggering the input. After $t_{MIR}$, the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals must be $t_{MIR}$ apart, where $t_{MIR} = 0.30 \times t_w$. The retrigger pulse duration is calculated as shown in Figure 10.

## Typical Application (continued)



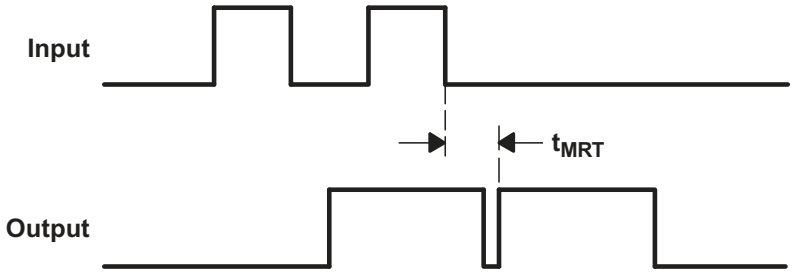

$t_{RT} = t_w + t_{PLH} = (K \times R_T \times C_T) + t_{PLH}$

**Where:**

$t_{MIR}$ = Minimum Input Retriggering Time
$t_{PLH}$ = Propagation Delay
$t_{RT}$ = Retrigger Time
$t_w$ = Output Pulse Duration Before Retriggering

**Figure 10. Retrigger Pulse Duration**

The minimum value from the end of the input pulse to the beginning of the retriggered output must be approximately 15 ns to ensure a retriggered output (see Figure 11).




$t_{MRT}$ = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output
$t_{MRT}$ = 15 ns

**Figure 11. Input and Output Requirements**

### 10.2.2 Detailed Design Procedure

- Timing requirements:
  - The pulse width must be long enough to be read by the desired output system, but short enough so that the output pulse completes prior to the next trigger event. It is recommended to make the output pulse just 10% longer than the minimum required for the output system.
- Recommended input conditions:
  - Slow or noisy inputs are allowed on $\overline{A}$, B, and $\overline{CLR}$ due to Schmitt-trigger input circuitry.
  - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in *Recommended Operating Conditions*.
- Recommended output conditions:
  - Load currents must not exceed the values listed in *Absolute Maximum Ratings*.

## Typical Application (continued)

### 10.2.3 Application Curves

Operation of the devices at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied.

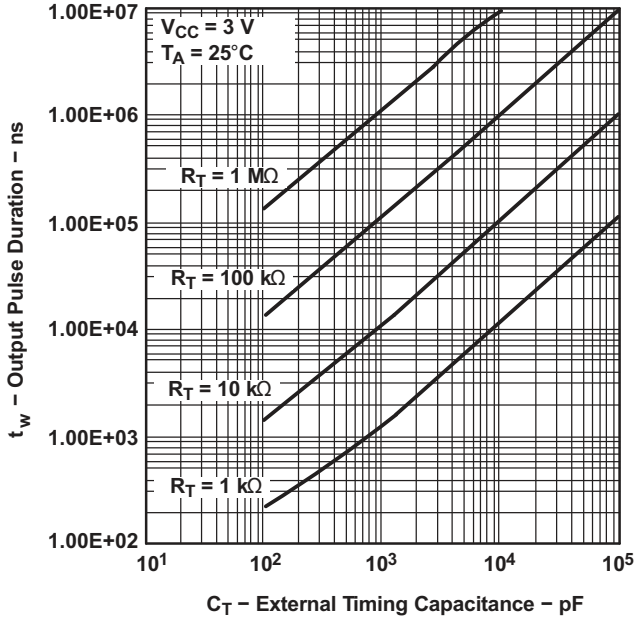



**Figure 12. Output Pulse Duration vs. External Timing Capacitance**

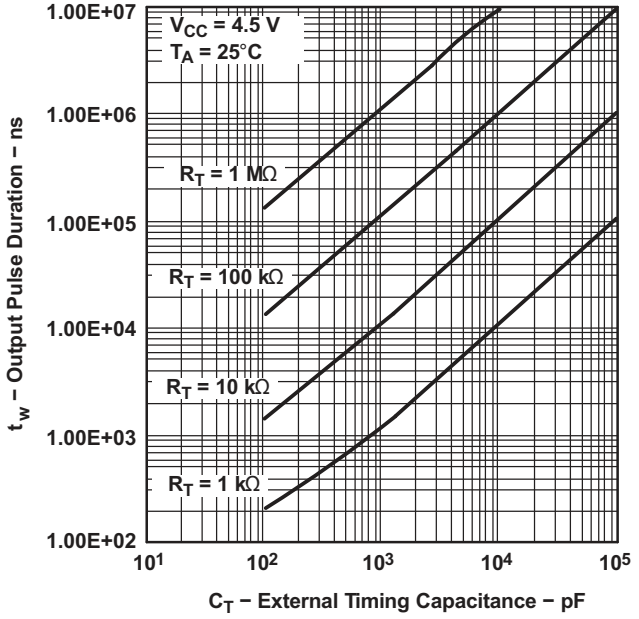



**Figure 13. Output Pulse Duration vs. External Timing Capacitance**

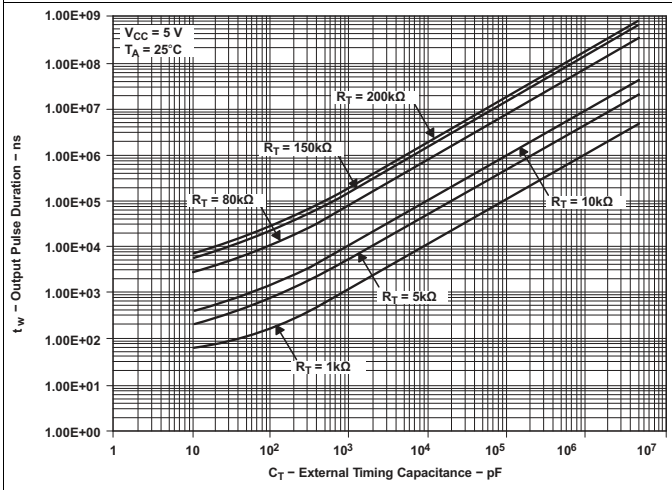



**Figure 14. Output Pulse Duration vs External Timing Capacitance**

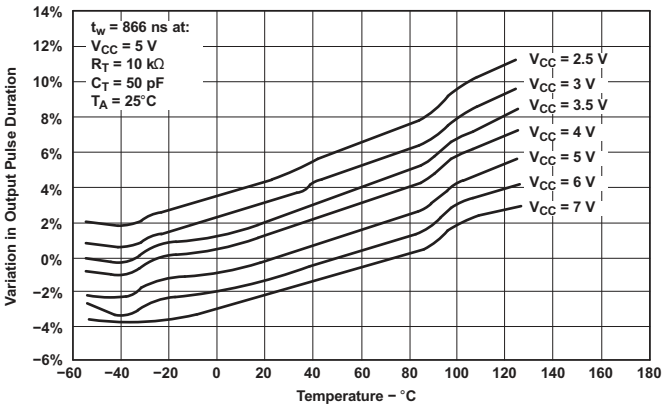



**Figure 15. Variations in Output Pulse Duration vs Temperature**

# 11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings*. Each $V_{CC}$ terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple VCC terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

# 12 Layout

## 12.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$ whichever makes more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver.

## 12.2 Layout Example

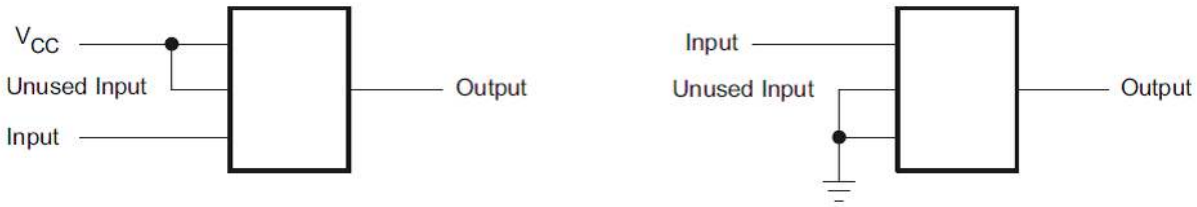



**Figure 16. Layout Recommendation**

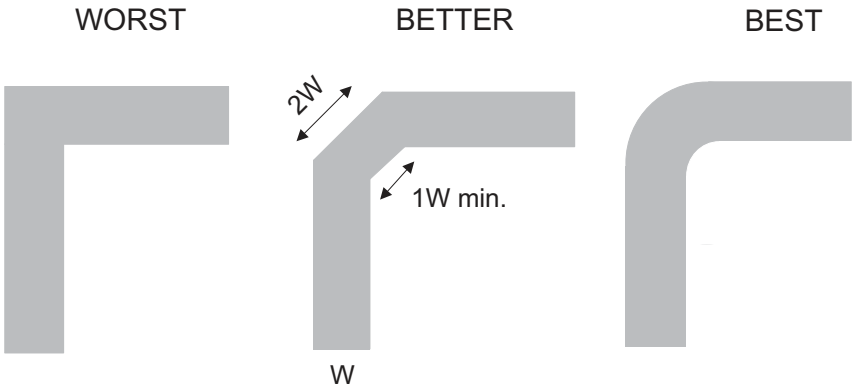



**Figure 17. Trace Example**

# 13 Device and Documentation Support

## 13.1 Documentation Support

### 13.1.1 Related Documentation

For related documentation, please see the following:

*Implications of Slow or Floating CMOS Inputs*, SCBA004

## 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54LV123A | Click here | Click here | Click here | Click here | Click here |
| SN74LV123A | Click here | Click here | Click here | Click here | Click here |

## 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV123ADBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV123A | Samples |
| SN74LV123ADGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV123A | Samples |
| SN74LV123ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV123A | Samples |
| SN74LV123ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV123A | Samples |
| SN74LV123ANSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV123A | Samples |
| SN74LV123APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV123A | Samples |
| SN74LV123APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV123A | Samples |
| SN74LV123ARGYR | ACTIVE | VQFN | RGY | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV123A | Samples |
| SN74LV123ARGYRG4 | ACTIVE | VQFN | RGY | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV123A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN74LV123A :**

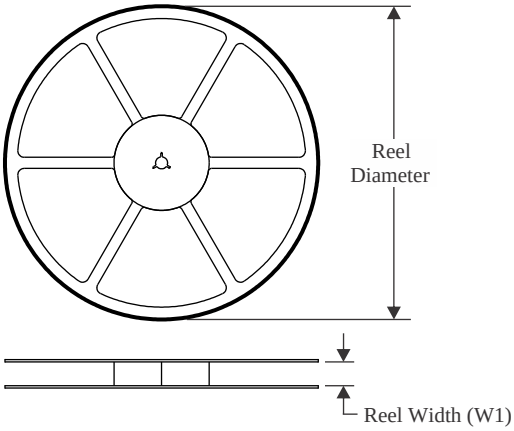
- Automotive : SN74LV123A-Q1
- Enhanced Product : SN74LV123A-EP

NOTE: Qualified Version Definitions:

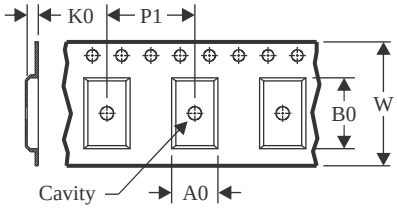
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

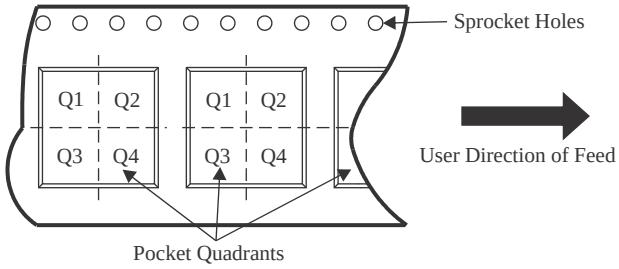



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

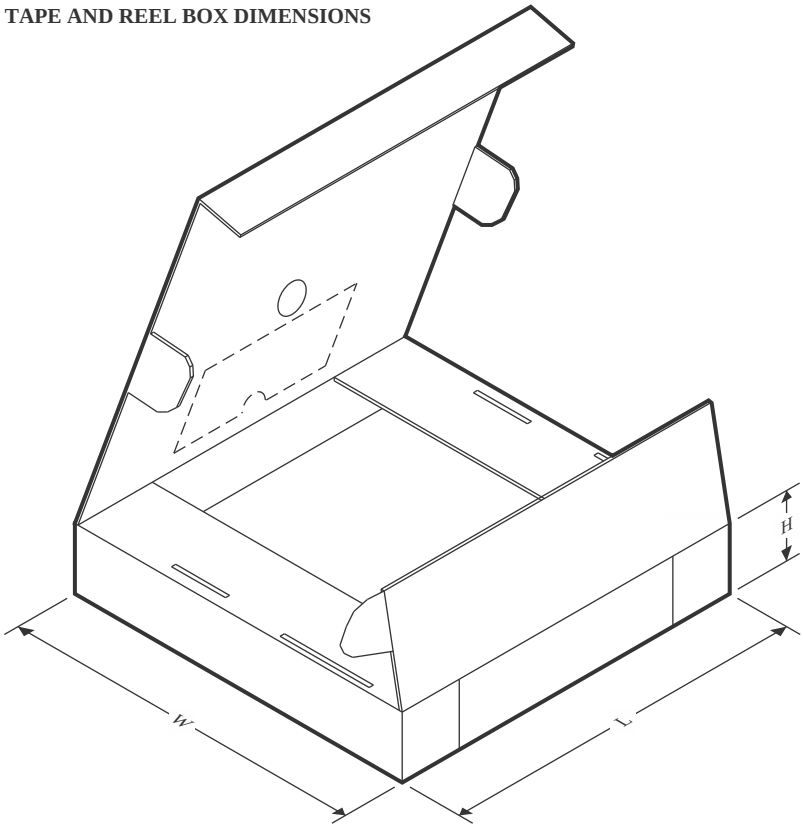
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

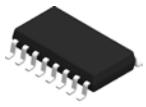
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV123ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV123ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV123ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV123ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV123ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV123ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV123APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV123APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV123ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV123ADBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV123ADGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV123ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV123ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV123ADRG4 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV123ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV123APWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV123APWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV123ARGYR | VQFN | RGY | 16 | 3000 | 356.0 | 356.0 | 35.0 |

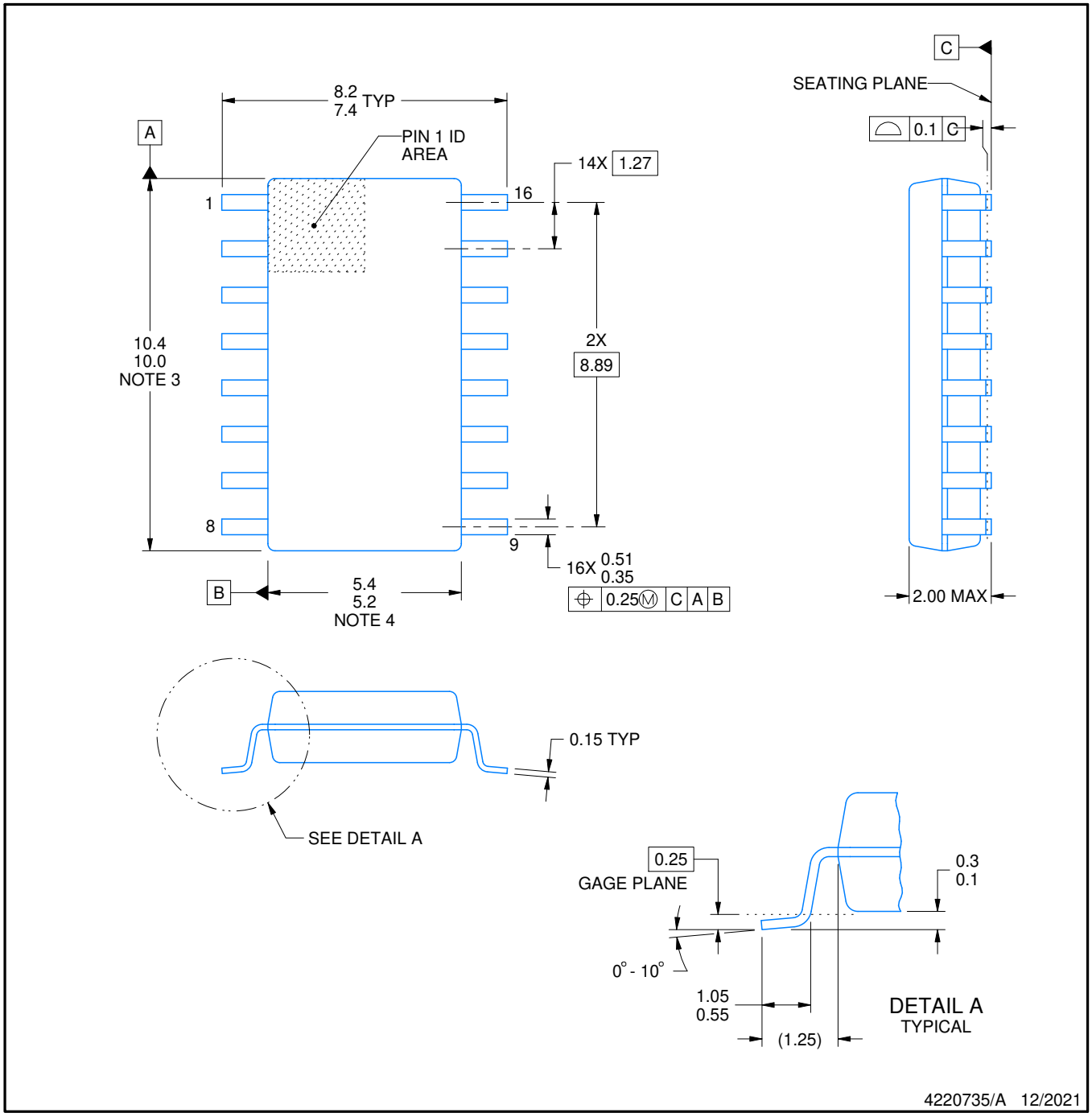


# PACKAGE OUTLINE

## NS0016A

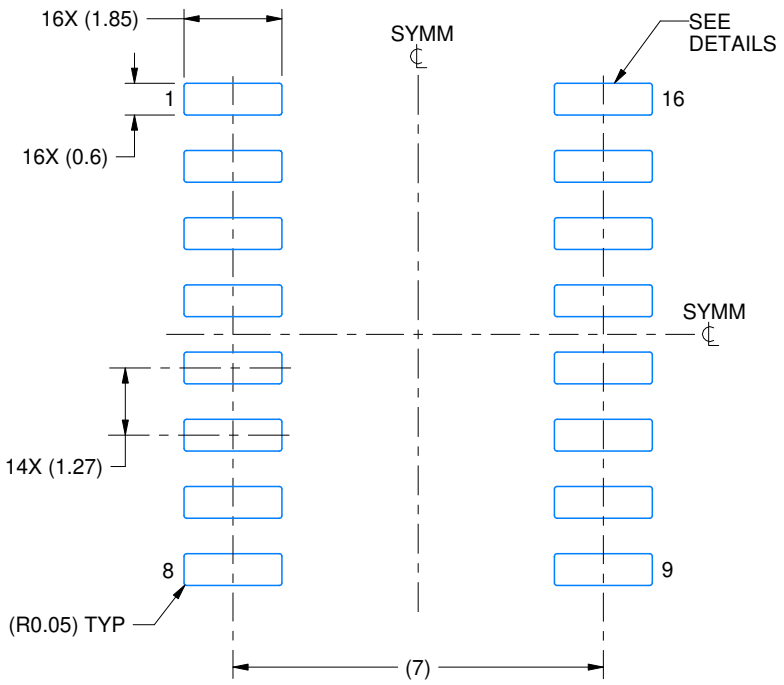
## SOP - 2.00 mm max height

SOP

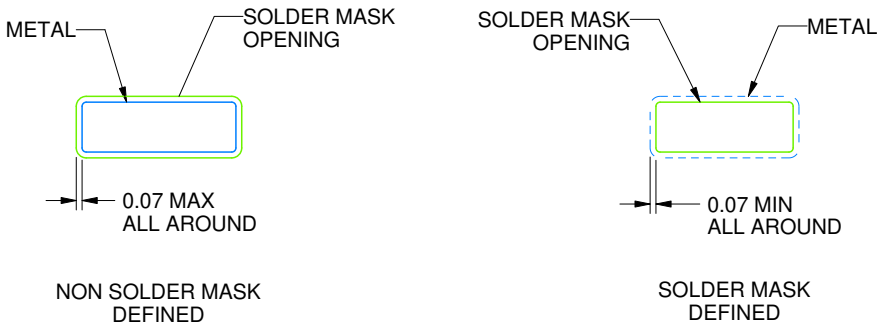



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X

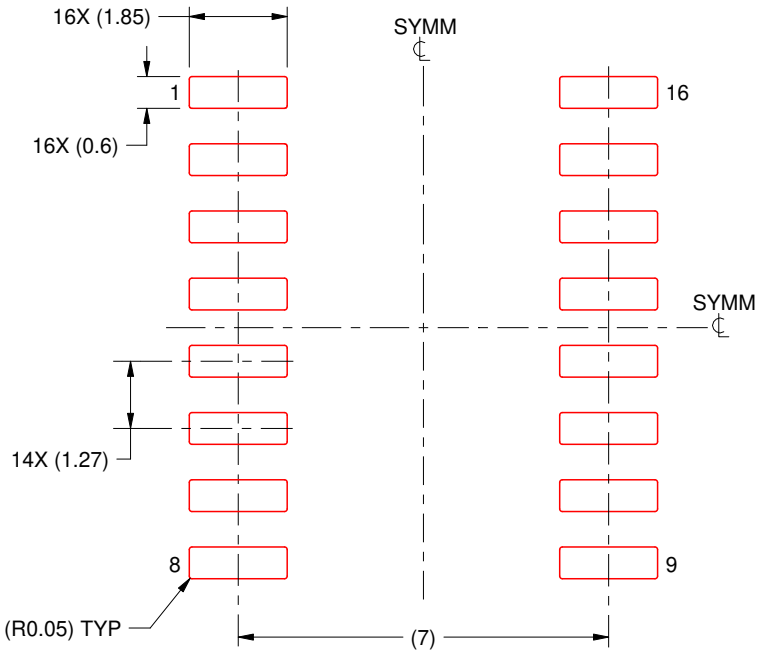



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



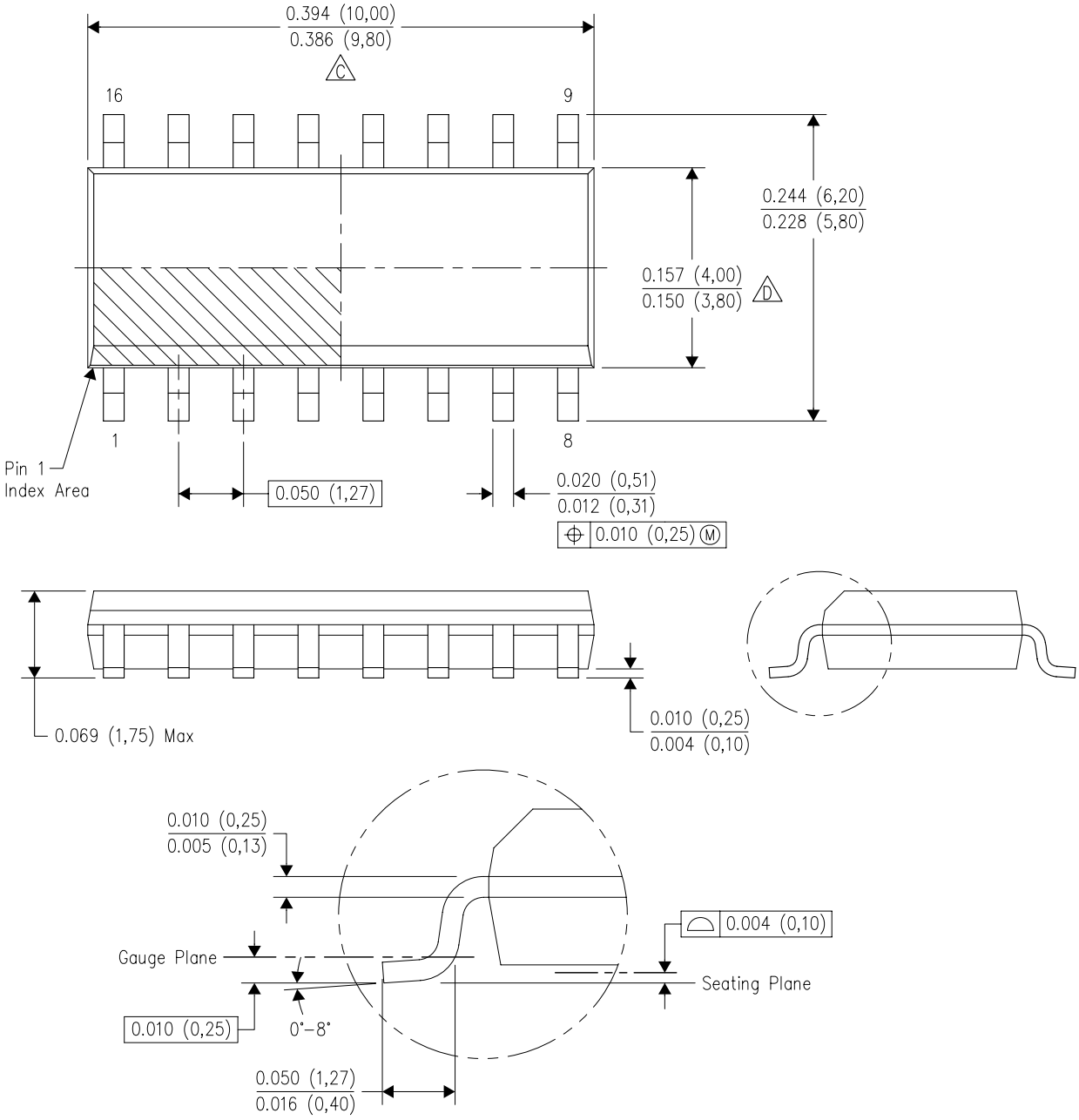

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

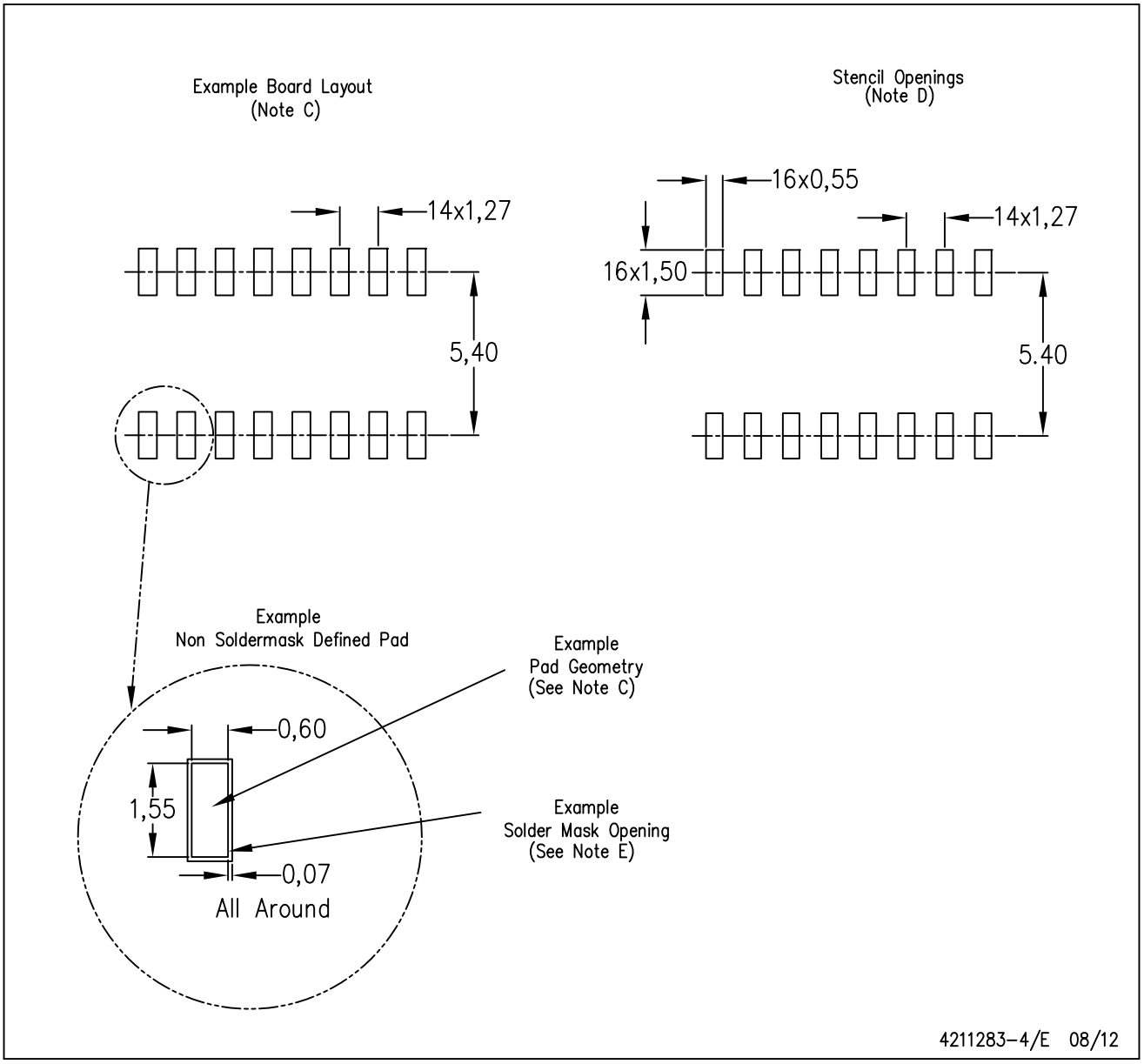
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

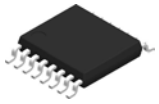
D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

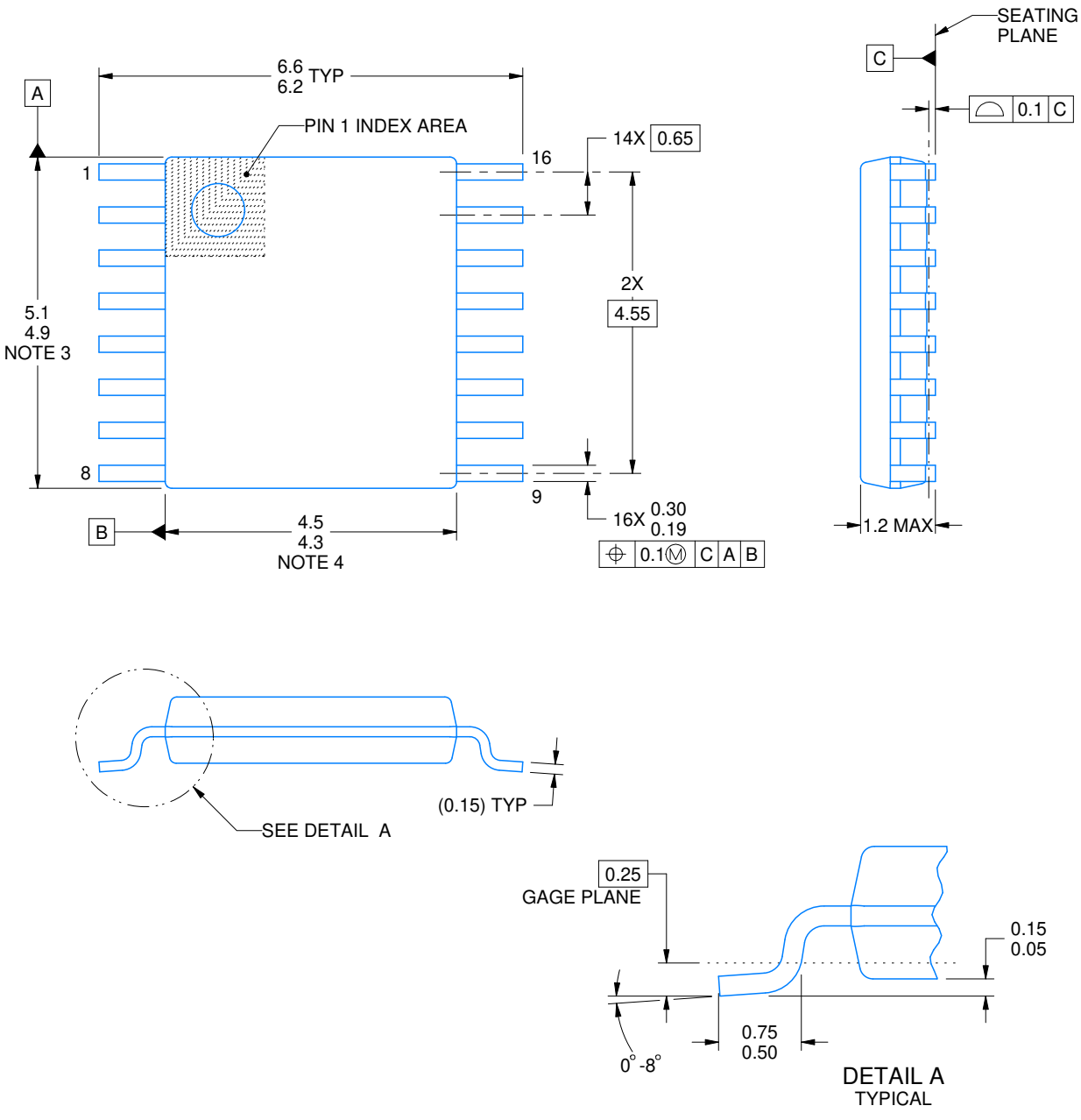
# PACKAGE OUTLINE

## PW0016A



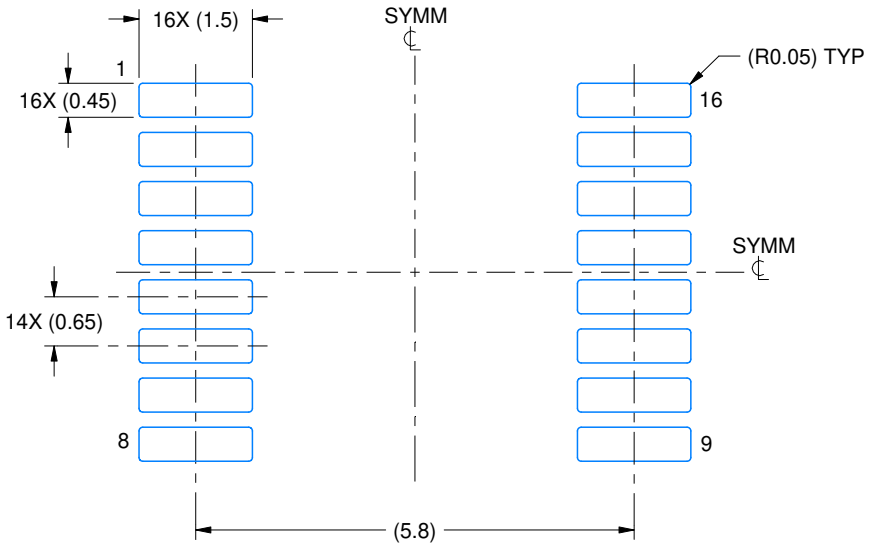
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

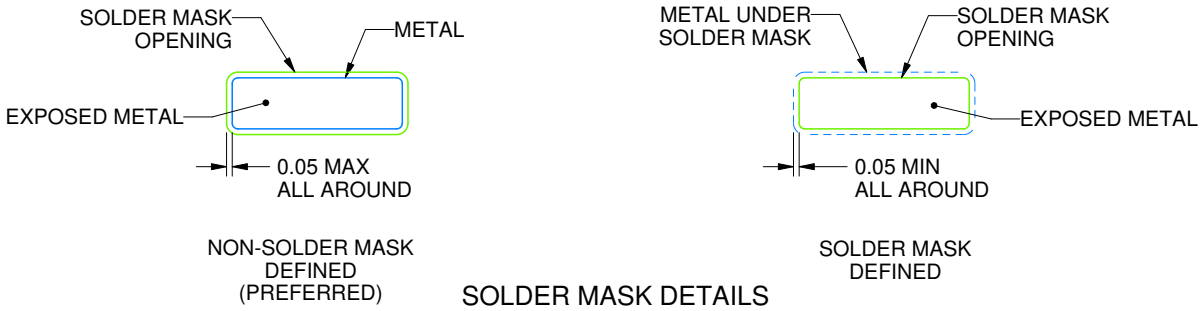



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

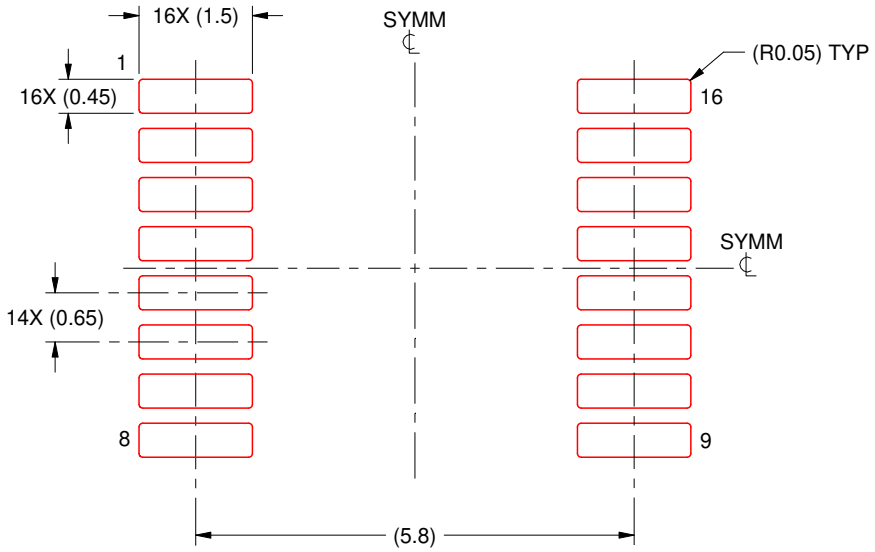



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

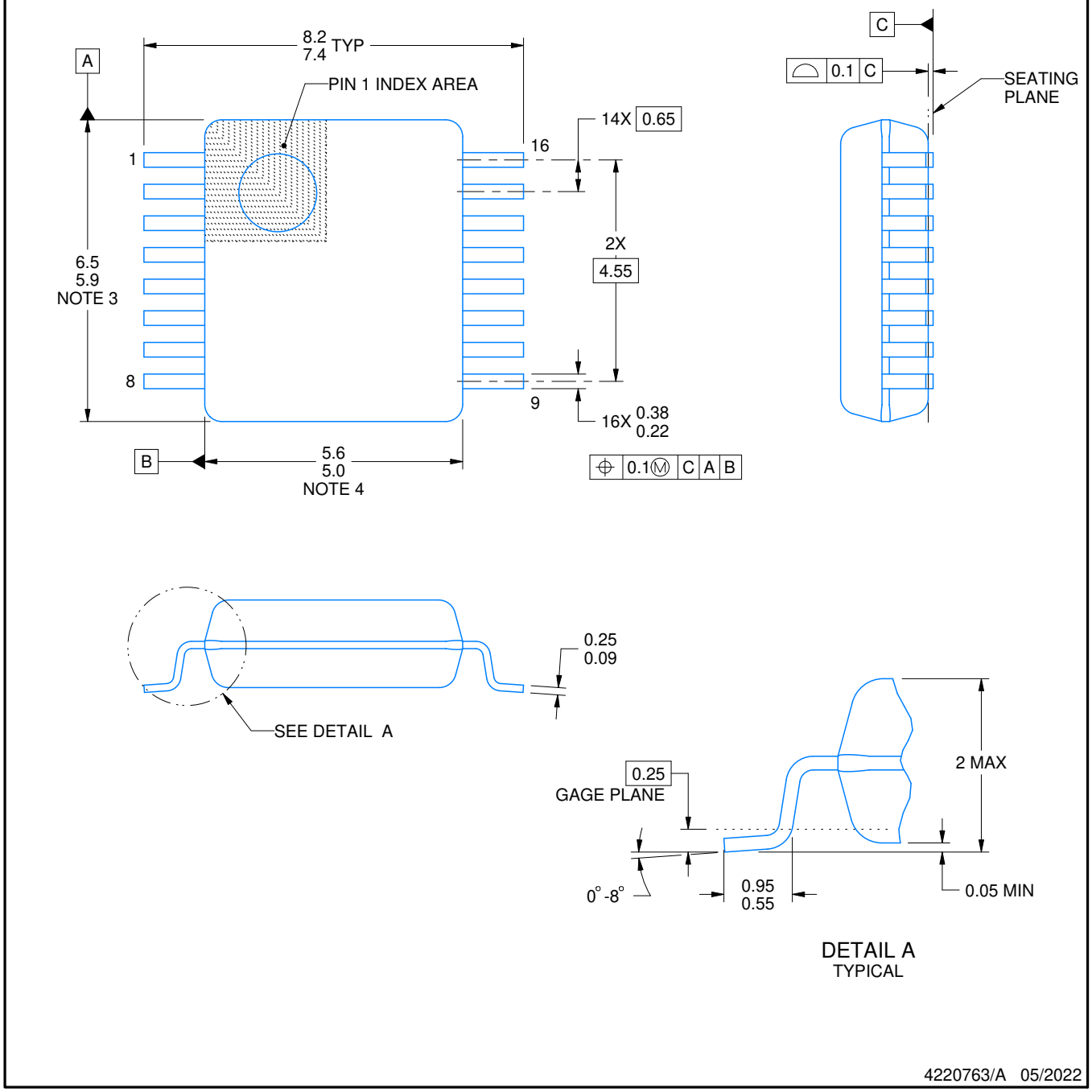
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DB0016A

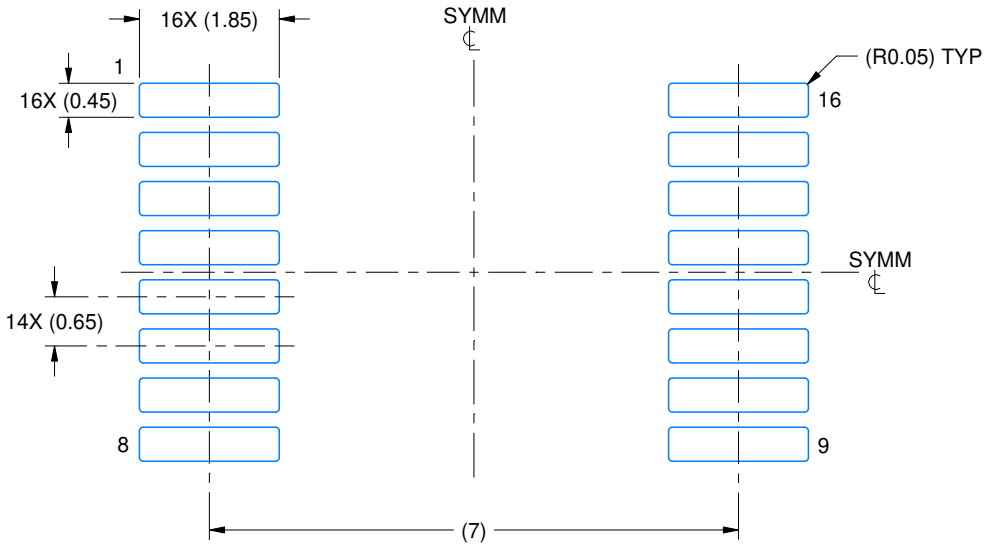
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

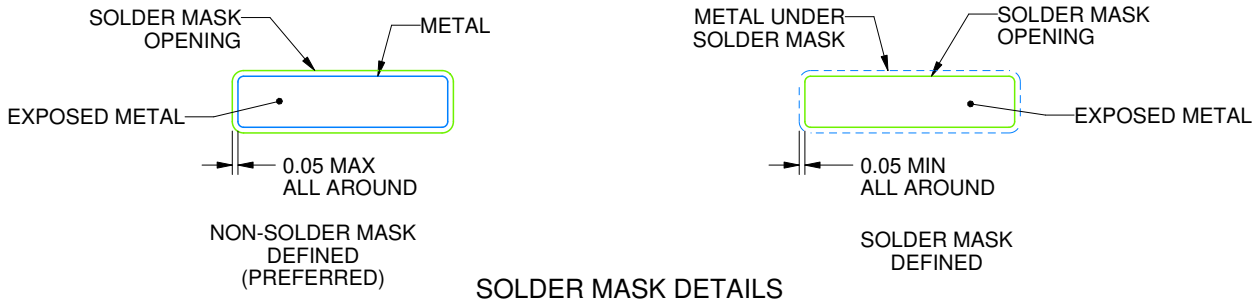



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

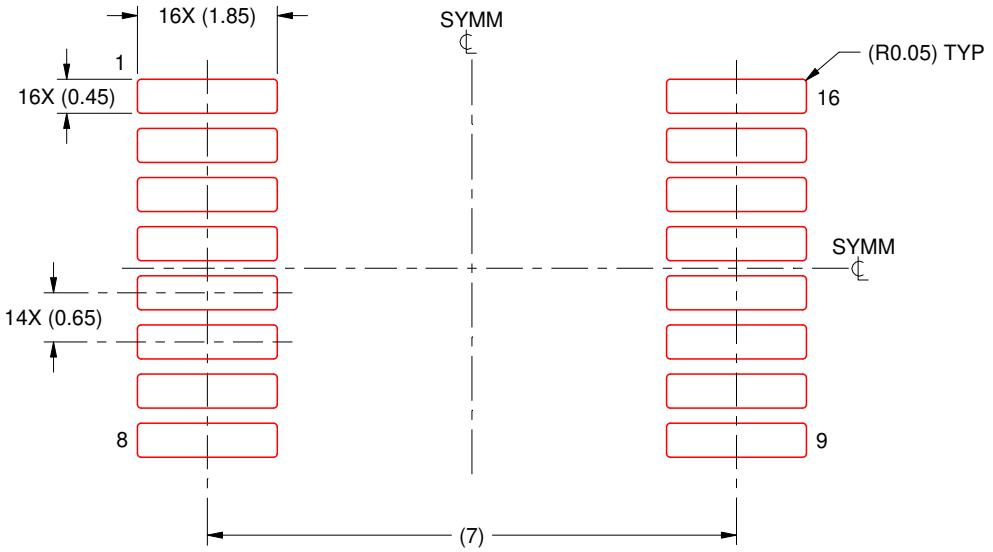



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

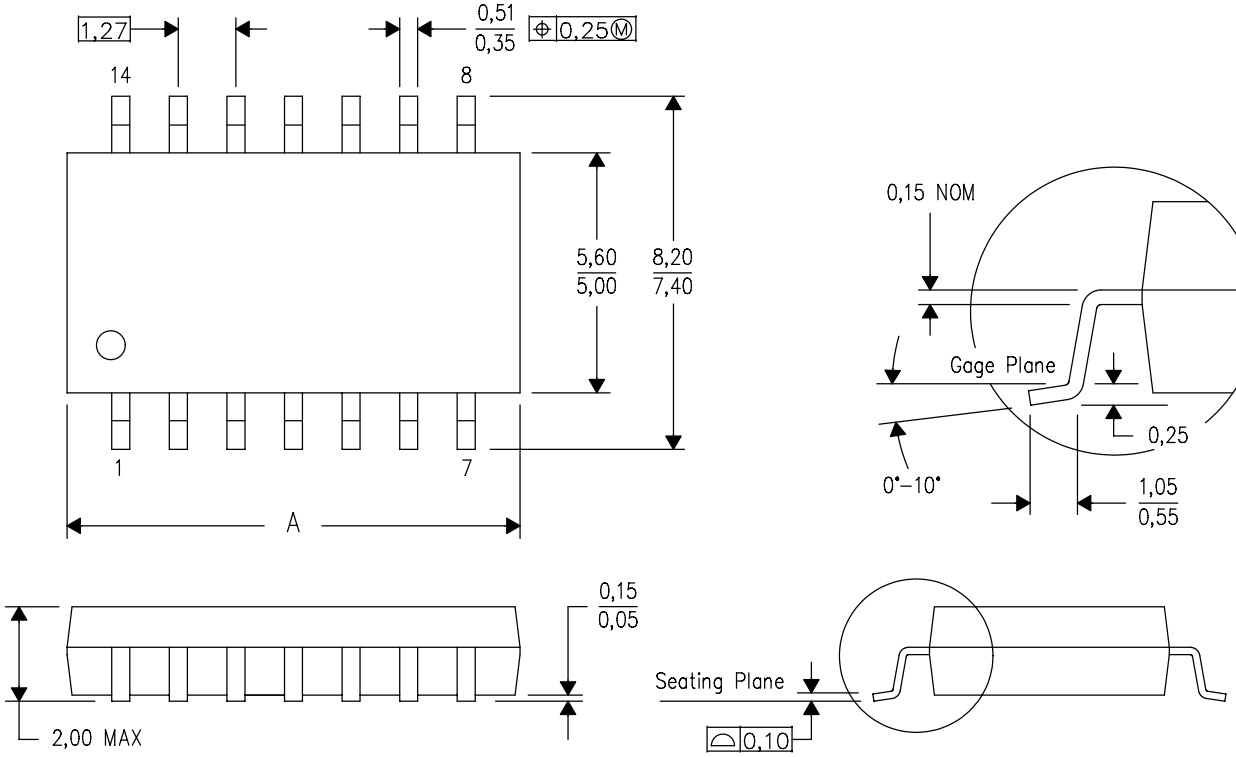
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

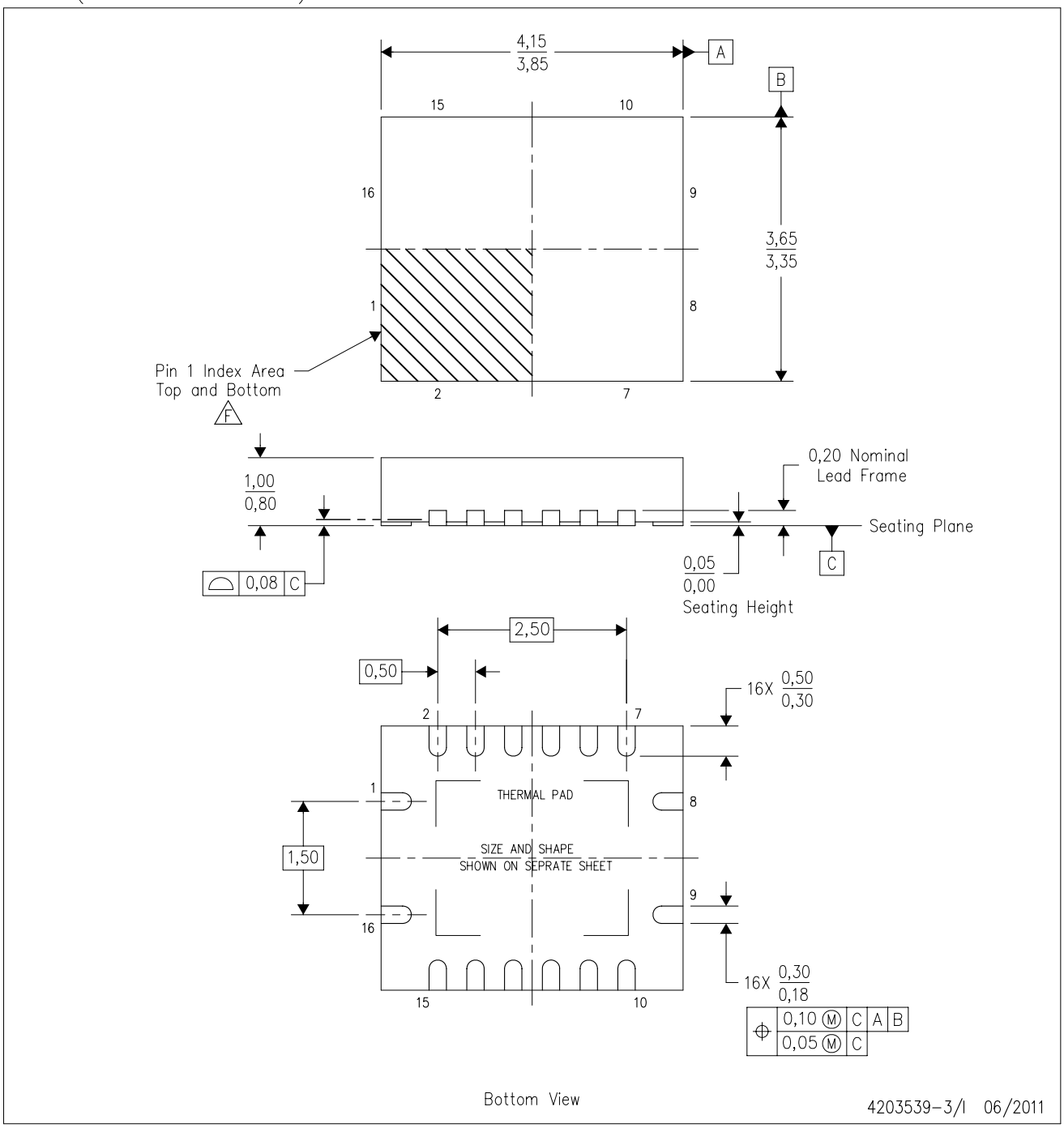



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

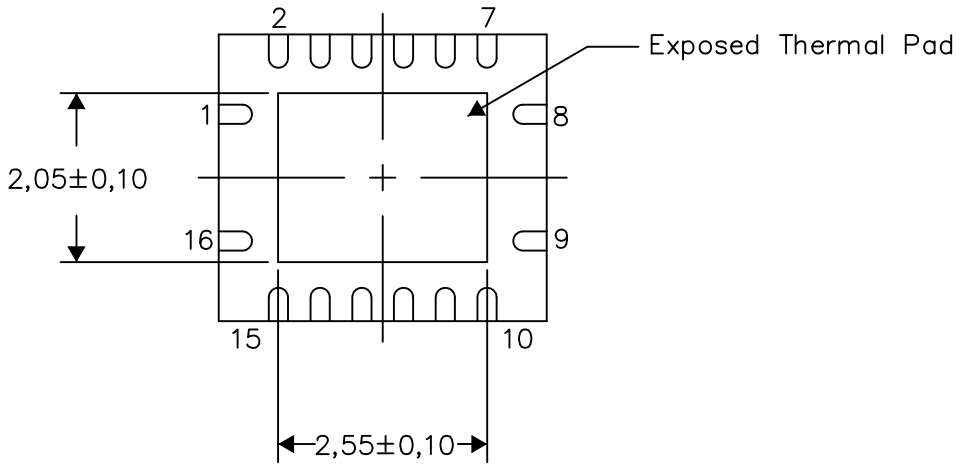
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



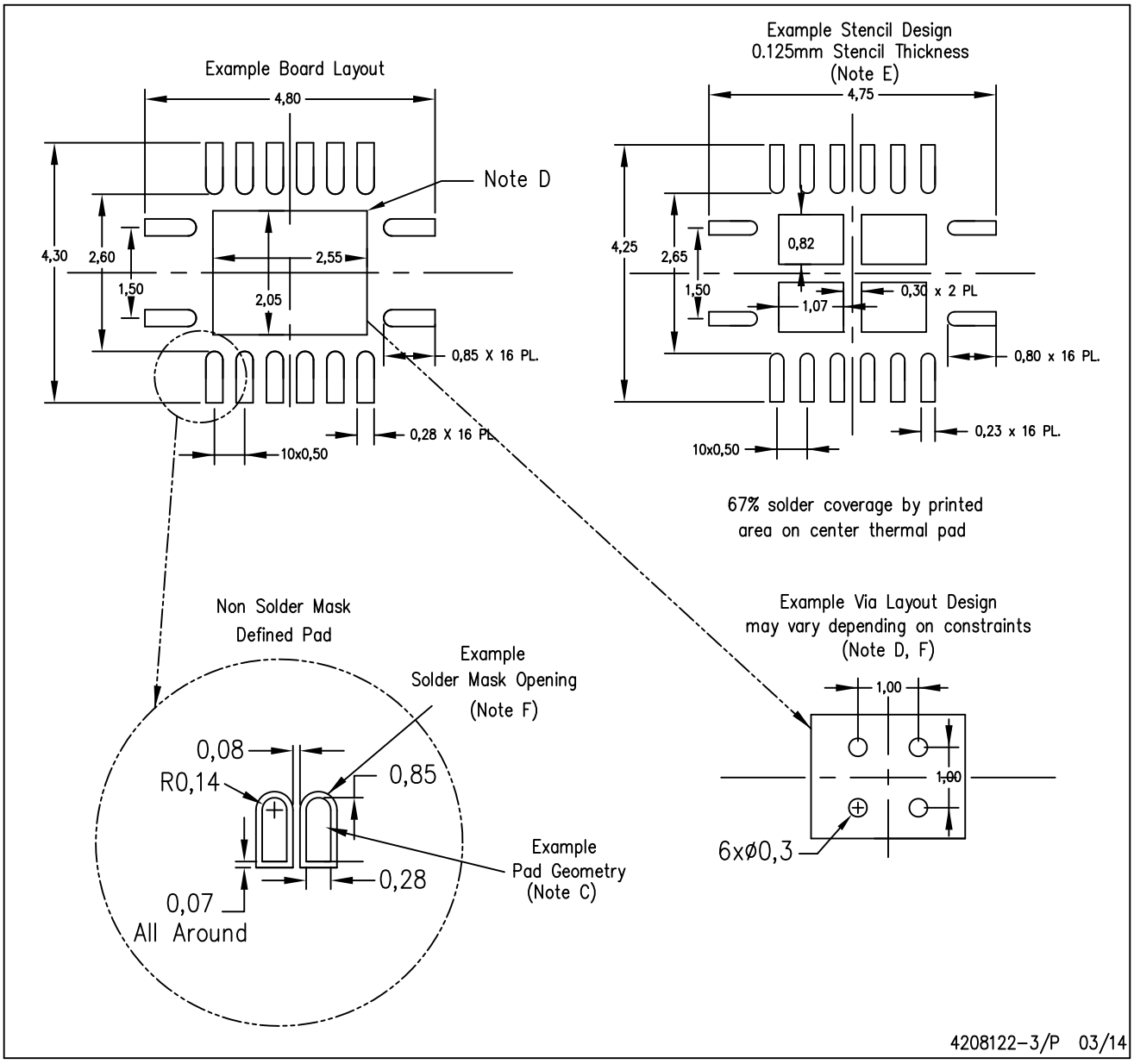

Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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