Default Configurations for Universal Frequency Translator Family of Devices

8T49N105

Code (ddd)	Mode	CONFIG	Input Frequency (MHz)		Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS	Output Frequency (MHz)
			CLK	XTAL_IN			Q	Q
-000	LoBW	0	25	40	Manual	Pin	P/on	125
		1	19.44	40			D/off	622.08
-001	LoBW	0	25	40	Manual	Pin	D/on	125
		1	25	40			D/off	125
-002	LoBW	0	61.44	40	Manual	Pin	D/on	61.44
		1	61.44	40			D/off	61.44
-006	LoBW	0	125	40	Manual	Pin	P/on	100
		1	125	40			D/off	100
-007	LoBW	0	76.92307692	40	Manual	Pin	D/on	76.92307692
		1	100	40			D/off	100
-999	LoBW	0	25	40	Manual	Pin	P/off	125
		1	19.44	40			D/off	622.08

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N183

Code (ddd)	Crystal Frequency (MHz)	PLL	Locked Loop Bandwidth (Hz)	Output Frequency (MHz)		GPIO Direction			
				Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State		GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
				Frequency Source					
				Phase Delay (steps)					
				Q0	Q1	GPIO0	GPIO1	GPIO2	GPIO3
-001	40	0	4 Hz	512	898	In	In	In	In
				D/+/on	D/+/on				
		1	4 Hz	PLL0	PLL1	GPI	GPI	GPI	GPI
				None	None				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N203

Code (ddd)	Mode	CONFIG	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
			CLK0	CLK1	XTAL_IN			Q0	Q1	Q0	Q1
-000	LoBW	0	25	25	40	Manual	Pin	P/on	P/on	125	125
		1	19.44	19.44	40			P/on	P/on	622.08	622.08
-001	LoBW	0	156.25	156.25	40	Manual	Pin	P/on	P/on	156.25	156.25
		1	1	1	40			P/on	P/on	156.25	156.25
-002	LoBW	0	30.72	30.72	40	Manual	Pin	P/on	P/on	122.88	122.88
		1	30.72	30.72	40			P/on	P/on	122.88	122.88
-003	LoBW	0	600	600	40	Manual	Pin	P/on	P/on	1200	1200
		1	605	605	40			P/on	P/on	1210	1210
-004	LoBW	0	91.7	91.7	40	Manual	Pin	P/on	P/on	165	165
		1	16.7	16.7	40			P/on	P/on	30	30
-005	LoBW	0	25	25	40	Manual	Pin	P/on	P/on	155.52	155.52
		1	25	25	40			P/on	P/on	155.52	155.52
-006	LoBW	0	156.25	156.25	40	Manual	Pin	P/on	P/on	156.255	156.255
		1	1	1	40			P/on	P/on	156.255	156.255
-007	LoBW	0	25	25	40	Manual	Pin	P/on	P/on	25	25
		1	25	25	40			P/on	P/on	25	25
-009	SYNTH / HiBW	0	n/a	n/a	40	Manual	Pin	D/on	D/on	156.25	156.25
		1	320	320	n/a			D/on	D/on	156.25	156.25
-010	HiBW	0	156.25	156.25	n/a	Manual	Pin	D/on	D/off	125	125
		1	320	320	n/a			D/on	D/off	125	125
-012	SYNTH	0	n/a	n/a	25	Manual	Pin	P/on	P/on	750	750
		1	n/a	n/a	25			P/on	P/on	450	450
-013	LoBW	0	156.25	156.25	40	Manual	Pin	D/on	D/on	156.25	156.25
		1	125	125	40			D/on	D/on	125	125
-014	LoBW	0	25	25	40	Manual	Pin	D/on	D/off	156.25	156.25
		1	25	25	40			D/on	D/off	125	125
-015	LoBW	0	156.25	156.25	38.88	Manual	Pin	D/on	D/on	156.25	156.25
		1	100	100	38.88			P/on	P/on	100	100
-016	HiBW	0	125	125	n/a	Manual	Pin	P/on	P/on	161.1328125	161.1328125
		1	156.25	156.25	n/a			P/on	P/on	161.1328125	161.1328125
-017	LoBW	0	161.1328125	161.1328125	40	Manual	Pin	P/on	P/on	25	25
		1	31.25	31.25	40			P/on	P/on	25	25
-018	LoBW	0	156.25	156.25	38.88	Manual	Pin	D/on	D/on	156.25	156.25
		1	100	100	38.88			D/on	D/on	100	100
-019	LoBW	0	125	125	40	Manual	Pin	P/on	P/on	161.1328125	161.1328125
		1	156.25	156.25	40			P/on	P/on	161.1328125	161.1328125
-023	SYNTH	0	n/a	n/a	40	Manual	Pin	D/on	D/on	187.512	187.512
		1	320	320	n/a			D/on	D/on	187.512	187.512
-024	HiBW	0	187.512	187.512	n/a	Manual	Pin	D/on	D/on	125	125
		1	125	187.512	40			D/on	D/on	156.25	156.25
-025	LoBW	0	644.53125	644.53125	40	Manual	Pin	P/on	P/on	644.53125	644.53125
		1	698.8123348	698.8123348	40			P/on	P/on	698.8123348	698.8123348
		1	10.24	10.24	25			P/on	P/off	10	10
-027	HiBW	0	26	26	n/a	Manual	Pin	D/on	D/on	644.53125	644.53125
		1	26	26	n/a			D/on	D/on	644.53125	644.53125
-028	LoBW	0	20	20	40	Manual	Pin	P/on	P/on	40	40
		1	10.24	10.24	25			P/on	P/on	10	10
-029	LoBW	0	125	125	40	Manual	Pin	P/on	P/on	156.25	156.25
		1	156.25	156.25	40			P/on	P/on	156.25	156.25
-999	LoBW	0	25	25	40	Manual	Pin	P/off	P/off	125	125
		1	19.44	19.44	40			P/off	P/off	622.08	622.08

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N205

Code (ddd)	Mode	CONFIG	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
			CLK0	CLK1	XTAL_IN			Q0	Q1	Q0	Q1
-000	LoBW	0	0.008	0.008	40	Manual	Pin	P/on	P/on	19.44	19.44
		1	10	10	40			P/on	P/on	155.52	155.52
-001	HiBW	0	100	100	n/a	Automatic	Non-Revertive	P/on	P/on	100	100
		1	133.3333333	133.3333333	n/a			P/on	P/on	133.3333333	133.3333333
-003	LoBW	0	19.44	19.44	25	Manual	Pin	D/on	D/on	155.52	155.52
		1	19.44	19.44	40			D/on	D/on	155.52	155.52
-004	LoBW	0	14.318	14.318	40	Automatic	Revertive	P/on	P/on	14.318	14.318
		1	14.318	14.318	40			P/on	P/on	14.318	14.318
-005	LoBW	0	10	10	40	Manual	Pin	P/on	P/on	10	10
		1	10	10	40			P/on	P/on	10	10
-006	LoBW	0	19.44	19.44	38.88	Manual	Pin	P/on	P/on	25	25
		1	19.44	19.44	38.88			P/on	P/on	125	125
-007	LoBW	0	19.44	19.44	38.88	Manual	Pin	P/on	P/on	25	25
		1	19.44	19.44	38.88			P/on	P/on	156.25	156.25
-009	LoBW	0	25	25	25	Automatic	Revertive	D/on	D/on	25	25
		1	25	25	40			D/on	D/on	25	25
-010	LoBW	0	103.125	103.125	25	Manual	Pin	P/on	P/on	25	25
		1	10.24	10.24	25			P/on	P/on	10	10
-999	LoBW	0	0.008	0.008	40	Manual	Pin	P/off	P/off	19.44	19.44
		1	10	10	40			P/off	P/off	155.52	155.52

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N222

Code (ddd)	Mode	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
		CLK0	CLK1	XTAL_IN			Q0	Q1	Q0	Q1
-000	LoBW	25	25	40	Manual	Pin	P/on	P/on	156.25	25
-001	LoBW	74.25	74.25	40	Manual	Pin	P/on	P/on	148.5	74.25
-002	LoBW	19.44	19.44	40	Manual	Pin	P/on	P/on	622.08	155.52
-003	LoBW	125	125	40	Manual	Pin	P/on	P/on	307.2	122.88
-004	LoBW	38.88	38.88	25	Manual	Pin	D/on	D/on	155.52	155.52
-100	HiBW	25	25	n/a	Manual	Pin	D/on	D/on	100	100
-101	HiBW	25	25	n/a	Manual	Pin	D/on	D/on	125	125
-108	LoBW	122.88	122.88	25	Manual	Pin	D/on	D/on	122.88	122.88
-109	SYNTH	n/a	n/a	25	Manual	Pin	D/on	D/on	125	156.25
-110	HiBW	25	25	n/a	Manual	Pin	D/on	D/on	156.25	100
-121	SYNTH	n/a	n/a	40	Manual	Pin	D/on	D/on	156.25	50
-122	LoBW	10	10	40	Manual	Pin	D/on	D/on	1000	100
-123	LoBW	25	25	40	Manual	Pin	D/on	D/on	125	156.25
-124	LoBW	10	10	40	Manual	Register	D/on	D/on	925	92.5
-125	LoBW	10	10	40	Manual	Register	D/on	D/on	1000	100
-126	LoBW	25	25	38.88	Manual	Pin	D/on	D/on	100	133.3333333
-127	LoBW	10	10	18.432	Manual	Register	D/on	D/on	1000	100
-999	LoBW	25	25	40	Manual	Pin	P/off	P/off	156.25	25

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N240

Code (ddd)	Serial Port Protocol	Boot Method	Crystal Frequency (MHz)	Input Frequency (MHz)		Locked Loop Bandwidth (Hz)	Output Frequency (MHz)				GPIO Direction			
							Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State				GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
	Device Address	EEPROM Addressing					Frequency Source							
							Phase Delay (steps)							
		Address		CLK0	CLK1		Q0	Q1	Q2	Q3	GPIO0	GPIO1	GPIO2	GPIO3
-984	I2C	OTP	49.152	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off				
	0b0110100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-990	I2C	OTP	49.152	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off				
	0b1110100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-991	I2C	EEPROM	49.152	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off				
	0b1101100	2-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-994	I2C	OTP	49.152	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-998	I2C	EEPROM	49.152	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N241

Code (ddd)	Serial Port Protocol	Boot Method	Crystal Frequency (MHz)	Input Frequency (MHz)		Locked Loop Bandwidth (Hz)	Output Frequency (MHz)				GPIO Direction			
							Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State				GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
	Device Address	EEPROM Addressing					Frequency Source							
							Phase Delay (steps)							
		Address		CLK0	CLK1		Q0	Q1	Q2	Q3	GPIO0	GPIO1	GPIO2	GPIO3
-993	I2C	EEPROM	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-994	I2C	OTP	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-997	I2C	EEPROM	38.88	DIS	DIS	25Hz	155.52	N/A	N/A	N/A	In	In	In	Out
							CN/+/on	P/+/off	P/+/off	P/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	GPI	GPI	GPI	LOL
		0b1010000					N/A	N/A	N/A	N/A				
-998	I2C	EEPROM	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1111100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-999	I2C	OTP	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1111100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N242

Code (ddd)	Serial Port Protocol	Boot Method	Crystal Frequency (MHz)	Input Frequency (MHz)		Locked Loop Bandwidth (Hz)	Output Frequency (MHz)				GPIO Direction			
							Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State				GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
	Device Address	EEPROM Addressing					Frequency Source							
							Phase Delay (steps)							
		Address		CLK0	CLK1		Q0	Q1	Q2	Q3	GPIO0	GPIO1	GPIO2	GPIO3
-006	I2C	EEPROM	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1111100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-993	I2C	EEPROM	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-997	I2C	EEPROM	38.88	DIS	DIS	25Hz	155.52	N/A	N/A	N/A	In	In	In	Out
							CN/+/on	P/+/off	P/+/off	P/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	GPI	GPI	GPI	LOL
		0b1010000					N/A	N/A	N/A	N/A				
-998	I2C	EEPROM	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1111100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				
-999	I2C	OTP	38.88	DIS	DIS	25Hz	N/A	N/A	N/A	N/A	In	In	In	In
							-/+/off	-/+/off	-/+/off	-/+/off				
	0b1101100	1-Byte					PLL	PLL	PLL	PLL	OE0	OE1	CSEL	GPI
		0b1010000					N/A	N/A	N/A	N/A				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

8T49N244

Code (ddd)	PLL-A	LoBW	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
			CLK0	CLK1	REF_IN			Q0	Q1	Q0	Q1
-000	PLL-A	LoBW	25	25	40	Manual	Pin	D/off	D/off	622.08	622.08
	PLL-B	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	644.53125	644.53125
-001	PLL-A	LoBW	2.048	2.048	40	Manual	Pin	D/off	D/off	125	125
	PLL-B	LoBW	77.76	77.76	40	Manual	Pin	D/off	D/off	125	125
-004	PLL-A	LoBW	120	120	40	Manual	Pin	D/off	D/off	120	120
	PLL-B	LoBW	40	40	40	Manual	Pin	D/off	D/off	180	180
-005	PLL-A	LoBW	40	40	40	Manual	Pin	D/off	D/off	180	180
	PLL-B	LoBW	120	120	40	Manual	Pin	D/off	D/off	120	120
-999	PLL-A	LoBW	25	25	40	Manual	Pin	D/off	D/off	622.08	622.08
	PLL-B	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	644.53125	644.53125

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N281

Code (ddd)	Serial Port Protocol	Boot Method	Crystal Frequency (MHz)	Input Frequency (MHz)		Locked Loop Bandwidth (Hz)	Output Frequency (MHz)								GPIO Direction			
							Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State								GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
	Device Address	EEPROM Addressing					Frequency Source											
							Phase Delay (steps)											
		Address		CLK0	CLK1		Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	GPIO0	GPIO1	GPIO2	GPIO3
-994	0b1101100	OTP	38.88	DIS	DIS	64 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte					None	None	None	None	None	None	None	None				
-998	0b1111100	EEPROM	38.88	DIS	DIS	64 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte					None	None	None	None	None	None	None	None				
-999	0b1111100	OTP	38.88	DIS	DIS	64 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte					None	None	None	None	None	None	None	None				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N282

Code (ddd)	Serial Port Protocol / Device Address	Boot Method / EEPROM Addressing / Address	Crystal Frequency (MHz)	PLL	Input Frequency (MHz) by PLL: PLL0 / PLL1 CLK0	CLK1	CLK2	CLK3	Locked Loop Bandwidth (Hz)	Output Frequency (MHz) — Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State / Frequency Source / Phase Delay (steps): Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	GPIO Direction — GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output: GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7
-997	0b1101100	EEPROM	38.88	0	DIS	DIS	DIS	DIS	64 Hz	155.52	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Out	In	In	In	In	In	In	In
										P/+/on	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	4 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	LOL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		1-Byte								None	None	None	None	None	None	None	None								
-998	0b1111100	EEPROM	38.88	0	DIS	DIS	DIS	DIS	64 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In	In	In	In	In
										P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	64 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		1-Byte								None	None	None	None	None	None	None	None								
-999	0b1111100	OTP	38.88	0	DIS	DIS	DIS	DIS	64 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In	In	In	In	In
										P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	64 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		1-Byte								None	None	None	None	None	None	None	None								

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N283

Code (ddd)	Serial Port Protocol	Boot Method	Crystal Frequency (MHz)	PLL	Input Frequency (MHz) by PLL		Locked Loop Bandwidth (Hz)	Output Frequency (MHz)								GPIO Direction			
								Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State								GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
	Device Address	EEPROM Addressing			PLL0			Frequency Source											
					PLL1			Phase Delay (steps)											
		Address			CLK0	CLK1		Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	GPIO0	GPIO1	GPIO2	GPIO3
-998	0b1111100	EEPROM	38.88	0	DIS	DIS	64Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	CN/+/off	P/+/off	P/+/off	P/+/off				
		0b1010000		1	DIS	DIS	64Hz	PLL0	PLL1	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	OE	OE	OE	OE
		1-Byte						None	None	None	None	None	None	None	None				
-999	0b1111100	Defaults	38.88	0	DIS	DIS	64Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	CN/+/off	P/+/off	P/+/off	P/+/off				
		0b1010000		1	DIS	DIS	64Hz	PLL0	PLL1	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	OE	OE	OE	OE
		-						None	None	None	None	None	None	None	None				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N285

Code (ddd)	Serial Port Protocol / Device Address	Boot Method / EEPROM Addressing / Address	Crystal Frequency (MHz)	Input Frequency (MHz) CLK0	Input Frequency (MHz) CLK1	Locked Loop Bandwidth (Hz)	Output Frequency (MHz) Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	GPIO Direction GPIO0	GPIO1	GPIO2	GPIO3
							Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State								GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
							Frequency Source											
							Phase Delay (steps)											
-991	0b1101100	EEPROM	38.88	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		2-Byte					None	None	None	None	None	None	None	None				
-993	0b1101100	EEPROM	38.88	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte					None	None	None	None	None	None	None	None				
-994	0b1101100	OTP	38.88	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte					None	None	None	None	None	None	None	None				
-996	0b1111100	EEPROM	38.88	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		2-Byte					None	None	None	None	None	None	None	None				
-998	0b1111100	EEPROM	38.88	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte					None	None	None	None	None	None	None	None				
-999	0b1111100	Defaults	38.88	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
							P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000					PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte					None	None	None	None	None	None	None	None				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N286

Code (ddd)	Serial Port Protocol / Device Address	Boot Method / EEPROM Addressing / Address	Crystal Frequency (MHz)	PLL	Input Frequency (MHz) by PLL: PLL0 / PLL1 CLK0	CLK1	CLK2	CLK3	Locked Loop Bandwidth (Hz)	Output Frequency (MHz) — Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State / Frequency Source / Phase Delay (steps): Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	GPIO Direction — GPIO Function (GPIO = General Purpose I/O, OE = Output Enable input, CSEL = Clock Select input, LOSn, LOLn, HOLDn = Alarm output): GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7
-991	0b1101100	EEPROM	38.88	0	DIS	DIS	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Out	In	In	In	In	In	In	In
										P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	LOL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		2-Byte								None	None	None	None	None	None	None	None								
-993	0b1101100	EEPROM	38.88	0	DIS	DIS	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In	In	In	In	In
										P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		1-Byte								None	None	None	None	None	None	None	None								
-994	0b1101100	OTP	38.88	0	DIS	DIS	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In	In	In	In	In
										P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		1-Byte								None	None	None	None	None	None	None	None								
-998	0b1111100	EEPROM	38.88	0	DIS	DIS	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In	In	In	In	In
										P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		1-Byte								None	None	None	None	None	None	None	None								
-999	0b1111100	OTP	38.88	0	DIS	DIS	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In	In	In	In	In
										P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off								
	I2C	0b1010000		1	DIS	DIS	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI	GPI	GPI	GPI	GPI
		1-Byte								None	None	None	None	None	None	None	None								

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N287

Code (ddd)	Serial Port Protocol	Boot Method	Crystal Frequency (MHz)	PLL	Input Frequency (MHz) by PLL		Locked Loop Bandwidth (Hz)	Output Frequency (MHz)								GPIO Direction			
								Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State								GPIO Function GPIO = General Purpose I/O OE = Output Enable input CSEL = Clock Select input LOSn, LOLn, HOLDn = Alarm output			
	Device Address	EEPROM Addressing			PLL0			Frequency Source											
					PLL1			Phase Delay (steps)											
		Address			CLK0	CLK1		Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	GPIO0	GPIO1	GPIO2	GPIO3
-991	0b1101100	EEPROM	38.88	0	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000		1	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		2-Byte						None	None	None	None	None	None	None	None				
-993	0b1101100	EEPROM	38.88	0	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000		1	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte						None	None	None	None	None	None	None	None				
-994	0b1101100	OTP	38.88	0	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000		1	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte						None	None	None	None	None	None	None	None				
-996	0b1111100	EEPROM	38.88	0	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000		1	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		2-Byte						None	None	None	None	None	None	None	None				
-998	0b1111100	EEPROM	38.88	0	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000		1	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte						None	None	None	None	None	None	None	None				
-999	0b1111100	Defaults	38.88	0	DIS	DIS	11.25 Hz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In	In
								P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off	P/+/off				
	I2C	0b1010000		1	DIS	DIS	11.2 Hz	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	PLL0	GPI	GPI	GPI	GPI
		1-Byte						None	None	None	None	None	None	None	None				

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N1012

Code (ddd)	Serial Port Protocol	Boot Method	Crystal Frequency (10M~40MHz)	CLK_SEL	PreScale	FB Divider	VCO Frequency (M)	Output Frequency (MHz)												
								Output Style (P = LVPECL, D=LVDS, CP = LVCMOS in-phase, CN = LVCMOS out-of-phase) Inversion (-) or non-inversion (+) Power-up State											
	Device Address	EEPROM Addressing						Frequency Source												
								Total Divide Ratio												
		Address						Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	REF
-991	0b1101100	EEPROM	40	Crystal	*2	43.5	3480	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
								P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	CP/+/Off
	I2C	0b1010000						DIVA	DIVB	DIVC	DIVD	DIVE	DIVF	DIVG	DIVH	DIVI	DIVI	DIVJ	DIVJ	XTAL
		2-Byte						N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1
-992	0b1101100	EEPROM	40	Crystal	*2	50	4000	125	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
								CN/+/On	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	CP/+/Off
	I2C	0b1010000						DIVA	DIVB	DIVC	DIVD	DIVE	DIVF	DIVG	DIVH	DIVI	DIVI	DIVJ	DIVJ	XTAL
		1-Byte						32	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1
-993	0b1101100	EEPROM	40	Crystal	*2	43.5	3480	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
								P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	CP/+/Off
	I2C	0b1010000						DIVA	DIVB	DIVC	DIVD	DIVE	DIVF	DIVG	DIVH	DIVI	DIVI	DIVJ	DIVJ	XTAL
		1-Byte						N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1
-994	0b1101100	OTP	40	Crystal	*2	43.5	3480	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
								P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	CP/+/Off
	I2C	0b1010000						DIVA	DIVB	DIVC	DIVD	DIVE	DIVF	DIVG	DIVH	DIVI	DIVI	DIVJ	DIVJ	XTAL
		1-Byte						N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1
-998	0b1101100	EEPROM	40	Crystal	*2	43.5	3480	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
								P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	P/+/Off	CP/+/Off
	I2C	0b1010000						DIVA	DIVB	DIVC	DIVD	DIVE	DIVF	DIVG	DIVH	DIVI	DIVI	DIVJ	DIVJ	XTAL
		1-Byte						N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N366

Code (ddd)	PLL	Mode	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
			CLK0	CLK1	REF_IN			Q0	Q1	Q0	Q1
-000	PLL-A	LoBW	25	25	40	Manual	Pin	D/off	D/off	622.08	622.08
	PLL-B	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	644.53125	644.53125
	PLL-C	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	156.25	156.25
-999	PLL-A	LoBW	25	25	40	Manual	Pin	D/off	D/off	622.08	622.08
	PLL-B	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	644.53125	644.53125
	PLL-C	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	156.25	156.25

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N445

Code (ddd)	PLL	Mode	Input Frequency (MHz)		Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS	Output Frequency (MHz)
			CLK	REF_IN			Q	Q
-000	PLL-A	LoBW	38.88	40	Manual	Pin	D/off	622.08
	PLL-B	LoBW	19.44	40	Manual	Pin	D/off	531.25
	PLL-C	LoBW	40	40	Manual	Pin	D/off	167.331645
	PLL-D	LoBW	25	40	Manual	Pin	D/off	164.3554688
-999	PLL-A	LoBW	38.88	40	Manual	Pin	D/off	622.08
	PLL-B	LoBW	19.44	40	Manual	Pin	D/off	531.25
	PLL-C	LoBW	40	40	Manual	Pin	D/off	167.331645
	PLL-D	LoBW	38.88	40	Manual	Pin	D/off	622.08

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

8T49N488

Code (ddd)	PLL	Mode	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
			CLK0	CLK1	REF_IN			Q0	Q1	Q0	Q1
-000	PLL-A	LoBW	25	25	40	Manual	Pin	D/off	D/off	622.08	622.08
	PLL-B	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	644.53125	644.53125
	PLL-C	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	156.25	156.25
	PLL-D	LoBW	25	25	40	Manual	Pin	D/off	D/off	161.1328125	161.1328125
-999	PLL-A	LoBW	25	25	40	Manual	Pin	D/off	D/off	622.08	622.08
	PLL-B	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	644.53125	644.53125
	PLL-C	LoBW	19.44	19.44	40	Manual	Pin	D/off	D/off	156.25	156.25
	PLL-D	LoBW	25	25	40	Manual	Pin	D/off	D/off	161.1328125	161.1328125

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

840N202

Code (ddd)	Mode	CONFIG	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Power-up State		Output Frequency (MHz)	
			CLK0	CLK1	XTAL_IN			Q0	Q1	Q0	Q1
-000	LoBW	0	25	25	40	Manual	Pin	on	on	125	125
		1	25	25	40			on	on	156.25	156.25
-001	LoBW	0	19.44	19.44	27	Manual	Pin	on	on	125	125
		1	19.44	19.44	27			on	on	25	25
-999	LoBW	0	25	25	40	Manual	Pin	off	off	125	125
		1	25	25	40			off	off	156.25	156.25

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

849N202

Code (ddd)	Mode	CONFIG	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
			CLK0	CLK1	XTAL_IN			Q0	Q1	Q0	Q1
-000	LoBW	0	25	25	40	Manual	Pin	P/on	P/on	25	25
		1	25	25	40			P/on	P/on	156.25	156.25
-001	HiBW	0	133.333	133.333	n/a	Manual	Pin	P/on	P/on	400	400
		1	133.333	133.333	n/a			P/on	P/on	533.333	533.333
-006	LoBW	0	156.25	156.25	25	Manual	Pin	P/on	P/on	156.25	156.25
		1	155.52	155.52	25			P/on	P/on	155.52	155.52
-008	SYNTH	0	n/a	n/a	25	Manual	Pin	P/on	P/on	100	100
		1	n/a	n/a	25			P/on	P/on	125	125
-009	LoBW	0	77.76	77.76	38.88	Manual	Pin	P/on	P/off	155.52	155.52
		1	77.76	77.76	38.88			P/on	P/off	155.52	155.52
-010	LoBW	0	156.25	156.25	25	Manual	Pin	P/on	P/on	644.53125	644.53125
		1	156.25	156.25	25			P/on	P/on	322.265625	322.265625
-011	LoBW	0	155.52	155.52	26	Manual	Pin	P/on	P/off	100	100
		1	155.52	155.52	26			P/on	P/off	155.52	155.52
-012	LoBW	0	40.08	40.08	25	Manual	Pin	D/on	D/on	320.64	320.64
		1	40.08	40.08	25			D/on	D/on	240.48	240.48
-013	SYNTH	0	n/a	n/a	25	Manual	Pin	D/on	D/on	40.08	40.08
		1	n/a	n/a	25			D/on	D/on	40.08	40.08
-014	LoBW	0	0.25	0.25	40	Manual	Pin	P/on	P/on	12	12
		1	0.25	0.25	40			P/on	P/on	12	12
-015	LoBW	0	0.008	0.008	40	Manual	Pin	D/on	D/on	155.52	155.52
		1	0.008	0.008	19.44			D/on	D/on	155.52	155.52
-016	SYNTH	0	n/a	n/a	25	Manual	Pin	D/on	D/on	133.33	133.33
		1	n/a	n/a	25			D/on	D/on	125	125
-017	HiBW	0	156.25	156.25	n/a	Manual	Pin	D/on	D/on	644.53125	644.53125
		1	156.25	156.25	n/a			D/on	D/on	322.265625	322.265625
-018	LoBW	0	100	100	27	Manual	Pin	D/on	D/on	100	100
		1	100	100	27			P/on	P/on	50	50
-019	SYNTH	0	n/a	n/a	25	Manual	Pin	D/on	D/on	156.25	156.25
		1	n/a	n/a	25			D/on	D/on	100	100
-020	LoBW	0	25	25	40	Manual	Pin	D/on	D/on	156.25	156.25
		1	74.25	74.25	40			D/on	D/on	148.5	148.5
-021	LoBW	0	644.53125	644.53125	25	Manual	Pin	P/on	P/on	161.13	161.13
		1	8.0565	8.0565	25			P/on	P/on	161.13	161.13
-022	LoBW	0	698.8	698.8	25	Manual	Pin	P/on	P/on	174.7	174.7
		1	8.735	8.735	25			P/on	P/on	174.7	174.7
-024	LoBW	0	644.53125	644.53125	40	Manual	Pin	D/on	D/on	161.1328125	161.1328125
		1	644.53125	644.53125	40			D/on	D/on	161.1328125	161.1328125
-025	LoBW	0	644.53125	644.53125	25	Manual	Pin	D/on	D/on	161.1328125	161.1328125
		1	n/a	644.53125	25			D/on	D/on	161.1328125	161.1328125
-999	LoBW	0	25	25	40	Manual	Pin	P/off	P/off	25	25
		1	25	25	40			P/off	P/off	156.25	156.25

NOTE: Please contact IDT (see last page) if a different configuration is desired.

Default Configurations for Universal Frequency Translator Family of Devices

849N212

Code (ddd)	Mode	CONFIG	Input Frequency (MHz)			Switchover Type	Switchover Mode	Output Style / Power-up State P = LVPECL, D = LVDS		Output Frequency (MHz)	
			CLK0	CLK1	XTAL_IN			Q0	Q1	Q0	Q1
-000	LoBW	0	25	25	40	Manual	Pin	P/on	D/on	25	25
		1	25	25	40			P/on	D/on	156.25	156.25
-001	LoBW	0	2.048	2.048	25	Manual	Pin	P/on	D/on	25	25
		1	25	25	25			P/on	D/on	2.048	2.048
-004	LoBW	0	2.048	2.048	25	Manual	Pin	P/on	D/on	125	125
		1	156.25	156.25	25			P/on	D/on	125	125
-005	LoBW	0	0.03125	0.03125	27	Manual	Pin	D/on	D/off	74.25	74.25
		1	0.03125	0.03125	27			D/on	D/off	74.25	74.25
-006	LoBW	0	0.0675	0.0675	27	Manual	Pin	D/on	D/off	74.25	74.25
		1	0.0675	0.0675	27			D/on	D/off	74.25	74.25
-007	LoBW	0	0.135	0.135	27	Manual	Pin	D/on	D/off	172	172
		1	0.135	0.135	27			P/on	D/off	172	172
-008	LoBW	0	10	10	25	Manual	Pin	P/on	D/on	100	100
		1	10.24	10.24	25			P/on	D/on	10	10
-009	LoBW	0	25	25	25	Manual	Pin	P/on	D/on	125	125
		1	2.048	2.048	25			P/on	D/on	125	125
-010	LoBW	0	2.048	2.048	25	Manual	Pin	P/on	D/on	125	125
		1	156.25	156.25	25			P/on	D/on	125	125
-999	LoBW	0	25	25	40	Manual	Pin	P/off	D/off	25	25
		1	25	25	40			P/off	D/off	156.25	156.25

NOTE: Please contact IDT (see last page) if a different configuration is desired.

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